Practice midterm exam

ECE 203

Initially given on 25 October 2004

Prepared by Robert Dick

You may not use books, notes, or calculators when completing this exam.

Please show your work.

Please look over all the problems now and ask questions if any of them are not clear.

(*n* pts.) Means the problem is worth *n* points.

I have included some challenging problems. However, they're worth very few points. Treat them like extra credit problems (solve them last, after all the high-weight problems are done). If you know the basic material, that's enough to get an A on the exam.

Good luck!

1. **(25 pts.)** Minimization

   (a) **(10 pts.)** Use the Quine-McCluskey method to find a minimal SOP expression for the following function:

   $$f(a,b,c) = \sum(0,1,2,5,6) + d(7)$$

   (b) **(2 pts.)** How many literals does your SOP expression have?

   (c) **(6 pts.)** Use a Karnaugh map to find a minimal POS expression for $f(a,b,c)$.

   (d) **(2 pts.)** How many literals does the POS expression have?

   (e) **(5 pts., challenging)** Would it have been possible to start from the SOP expression and convert to the POS expression using only algebraic manipulation? Why or why not?

2. **(10 pts.)** TTL: You have two SPST switches (like the ones in your lab kit) with which you need to control the inputs to a two-input TTL NAND gate. Unfortunately, you don't have any resistors. Draw the schematic of a working circuit. Note that this technique is a bit of a hack, and should be avoided when possible.

3. **(10 pts.)** Base conversion

   (a) **(5 pts.)** Convert each of the following hex numbers to binary numbers: 0x00, 0x18, 0x24, 0x5a, and 0xa5. For this problem, showing your work is optional.

   (b) **(5 pts.)** Convert the 647 to octal (base 8). Show your work.

4. **(20 pts.)** CMOS: Draw the schematic of a minimal transistor count CMOS implementation of the following function using only wires, NMOS transistors, and PMOS transistors:

$$h(a,b,c) = ab + c$$

You may assume access to complemented and uncomplemented input literals. You may choose to do some graphical or algebraic manipulation before starting the schematic.

5. **(20 pts.)** Building blocks: Using only multiplexers, design an encoder with four input lines, for which exactly one input line will be active at all times. You may assume access to complemented and uncomplemented input literals. Area efficiency counts.

6. **(15 pts.)** Combinational logic

   (a) **(4 pts.)** How many unique functions of three Boolean variables exist?

   (b) **(3 pts.)** Write an expression for the number of unique function of n variables, for some arbitrary integer n given that $n \geq 0$.

   (c) **(2 pts.)** How many unique functions of three (or fewer) variables may be implemented using one-level logic?

   (d) **(2 pts.)** How many unique functions of three (or fewer) variables may be implemented using two-level logic?

   (e) **(2 pts.)** How many unique functions of three (or fewer) variables may be implemented using multi-level logic?

   (f) **(2 pts., challenging)** Write an expression for the number of unique functions of n variables that may be implemented using only one-level logic.