Midterm exam
EECS 203
2 May 2007
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You may not use books, notes, or calculators when completing this exam.

Please show your work.

Please look over all the problems now and ask questions if any of them are not clear before starting.

(n pts.) Means the problem is worth n points.

Plan your time carefully. It is better to have all the answers right and nearly-optimal than to have one answer optimal, but no other answers.

Good luck!

1. **(10 pts.)** Find a minimal PoS form expression for the following function using a Karnaugh Map.

$$f(a,b,c,d) = \sum(0,2,3,4,12,14) + d(7,8)$$

2. **(10 pts.)** Minimize the following function using algebraic transformations or the Quine–McCluskey method.

$$f(a,b,c) = \overline{a}\,\overline{b} + \overline{b}\,c + a\overline{b}\,\overline{c} + \overline{a}\,b\overline{c}$$

3. **(10 pts.)** Show a CMOS transistor-level diagram for the carry output of a full-adder. You do not need to show the sum output. Correctness is of greatest importance but efficiency also counts. You may use hierarchy.

4. **(10 pts.)** Derive the minimal-two level formulas for a special encoder with the following properties. The encoder has three inputs and a minimal number of outputs. The output of the encoder will be observed only when exactly two of the input bits are on. In other words, if zero, one, or three input bits are on we do not care about the encoder output.

5. **(4 pts.)** Is it possible to devise a 3-bit binary encoding for the numbers 0–7 in which each pair of numbers that differ by one have encodings that differ in exactly two bits? Prove that your answer is correct.

6. **(3 pts.)** Why are PMOS transistors often wider than NMOS transistors? Use no more than three sentences.

7. **(3 pts.)** If a ripple-carry adder has a delay of d and multiplexer delay is negligible compared to full-adder delay, express (as a function of d) the approximate delay of a cary select adder implementing the same functions.