Homework four
ECE 203
Due 9 May
Prepared by Robert Dick and Russ Joseph

"Mano" is M. Morris Mano and Charles R. Kime. *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, fourth edition, 2008.

Please note that the assigned homework may not be enough for some people. If the concepts are still a little fuzzy after doing the homework, please take advantage of the other problems in Mano and/or see me for more problems.

When you can verify an answer, do so.

Show your work.

1. **(0 pts.)** Do Mano 5.7, 5.11, 5.13, 5.18, 5.31, and 5.37

2. **(0 pts.)** If you didn't ace the midterm Karnaugh map questions, you need some more practice: do these and hand them in. I want you to do well on the final.

$$f(a,b,c) = \sum(4,5,7) + DC(1)$$
$$f(a,b,c) = \prod(0,4) + DC(6,7)$$
$$f(a,b,c,d) = \sum(0,4,7) + DC(2,5,8,9,12,14,15)$$
$$f(a,b,c,d) = \prod(0,2,7,8,10,12,13,14) + DC(1,3,4,11,15)$$

3. **(5 pts.)** For each of the following base-10 numbers, find the representation in base-16 (hexadecimal).
   (a) 39
   (b) 21
   (c) 126
   (d) 119

4. **(5 pts.)** For each of the following base-10 numbers, find the sign-magnitude and two's-complement base-2 forms.
   (a) -12
   (b) 34
   (c) -6
   (d) 7

5. These questions will take some work. Please start discussing this on the mailing list. I'll give help and hints if people go astray in the design process. You need to start from basic logic gates (including XORs). However, you can use hierarchy. For example, you may show how to build a FA from basic gates and then use the FA block repeatedly. You may use MUXs without showing their contents.
   (a) **(10 pts.)** Draw a gate-level schematic of a three-bit (one bit sign, two bit magnitude) ripple-carry sign-magnitude adder-subtracter.
   (b) **(5 pts.)** Draw a gate-level schematic of a three-bit ripple-carry two's-complement adder-subtracter.

Table 1: Truth table

a	b	old Q	new Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	(ignore)
1	0	1	(ignore)
1	1	0	
1	1	1	

6. **(15 pts.)** Draw the schematic of a device that will multiply two three-bit sign-magnitude numbers to produce a 5-bit sign-magnitude number. You may use basic gates, half adders, full adders, and MUXs.

7. **(10 pts.)** Design two different three-bit Gray codes. Consider 0 to be adjacent to 7, e.g.,

decimal	code
0	000
1	010
2	011
3	001
4	101
5	111
6	110
7	100

8. **(10 pts.)** Use MUXs and/or DMUXs to design a device that accepts a three-bit unsigned number, a, and a two-bit unsigned number d. The device should output a three-bit unsigned number, b, that is equal to $\lfloor a/2^d \rfloor$.

9. **(10 pts.)** For the circuit in Figure 1, fill in Table 1 to represent how the value of Q changes based on inputs a and b, as well as the previous value of Q.

10. **(10 pts.)** Given the input and clock transitions in Figure 2, indicate the output of a D device assuming:

    (a) It is a negative edge-triggered flip-flop.

    (b) It is a positive edge-triggered flip-flop.

    (c) It is a clocked latch.

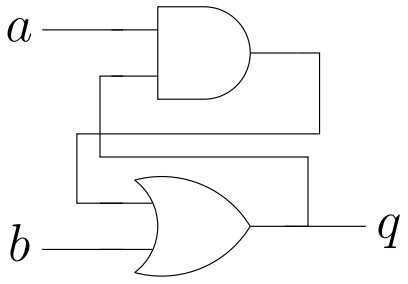

Figure 1: A strange latch

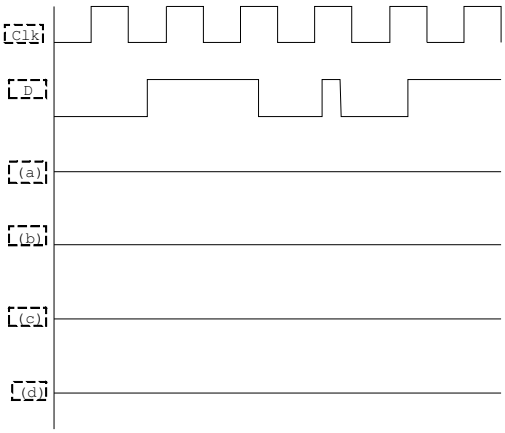

Figure 2: Timing diagram

You may assume 0 setup, hold and propagation times.

11. **(10 pts.)** Use basic gates to design a clocked Set-Reset latch with active-low s and r inputs, and an active-high clock.

12. **(10 pts.)** Using one full-adder, one rising edge-triggered D flip-flop with an asynchronous reset, and other basic gates as needed, design a *unsigned* serial adder. In other words, design a device that will accept a new pair of input values (a_i, b_i) every clock cycle and output the appropriate sum bit, s_i, and store the carry bit for use in the next clock cycle.

13. **(0 pts.)** Were there any problems that were mostly busy-work? In other words, were there any problems that required a lot of time without helping you to learn new concepts? If so, which ones.

14. **(0 pts.)** Were there any problems for which the lectures, book, and handouts didn't give you enough background information? If so, which ones?