Laboratory assignment three
Error detection in digital communication lines
EECS 203

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Lab report due during your lab check slot on 23 April

Please keep track of how long you spend doing this laboratory assignment. Specifically, how much time is needed to do the problems after studying enough to understand the concepts?

Please carefully review lecture four before starting this assignment. If you make catastrophic wiring mistakes, this could result in be exploding integrated circuits sending chunks of plastic into your forehead.

In this laboratory assignment, you will be modifying a circuit so that it will tolerate errors on (encoded signal) communication wires between a control panel and remote outputs. Although this lab assignment isn't more difficult than lab two, it does require more independent thinking. I'll try to guide you through the necessary steps in the Theory section of this handout.

Please show your work in your lab report.

1 Original design

You have been hired by a space flight company to improve their rocket design. An *actuator* is a device that performs a mechanical action in response to an input signal. In the original design, most actuator signals were generated by error-tolerant primary control computers located very near the actuators. However, a few signals came from the pilot control panel. In the original design, the pilot could push buttons to generate any of the signals indicated in the following table.

1. no action
2. open hatch (H)
3. decompress cabin (C)
4. eject pilot (P)
5. release safety harness (S)
6. self-destruct (D)

The actuators and control panel are both highly reliable. They were connected by a shielded cable containing four wires, one of which is presently unused. The original design called for the transmission of four unencoded signals. The project's prior engineer decided to add a signal, and made due with the same cable by encoding and decoding the signal. You were able to learn this information by reading the excellent technical reports produced by the engineer who formerly held your position.

2 A small design flaw

Unfortunately, the control panel to actuator signal cable is routed near other electrical devices, e.g., motors, that can interfere with the transmission of digital signals. Despite the signal cable's shielding, there was a problem when the first designer was testing it in orbit. Although nobody is certain exactly what happened, it appears that a spurious "decompress cabin" signal appeared at the actuators while the orbital rocket was in a vacuum and the designer was not wearing a pressurized suit. Your job is to make the communication of control signals error-resistant.

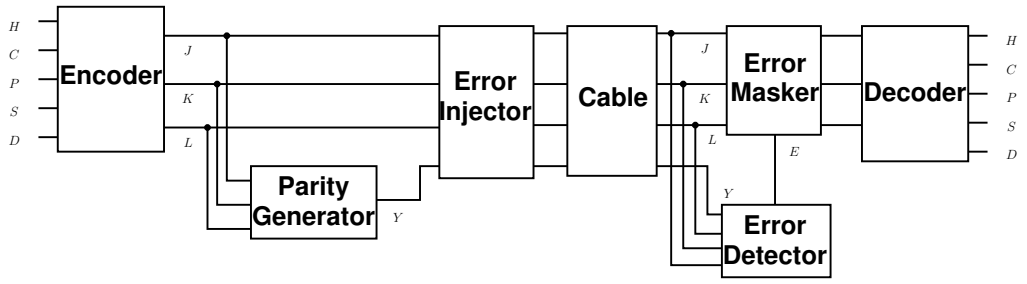

Figure 1: Pre-decoder error masking block diagram

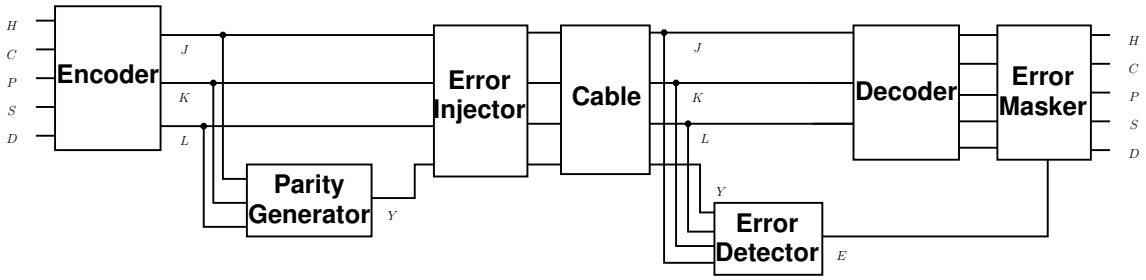

Figure 2: Post-decoder error masking block diagram

3 Resource background

Your predecessor had already selected a cable with excellent shielding to prevent interference. However, laboratory tests indicate that there is still a 0.1 probability that an error on a single wire will occur during a day. The probability of errors on two wires occurring at the same time is extremely low. Your cable contains four wires. Three must be used for (encoded) signals. The fourth can be used to assist you in detecting errors.

4 Design guidelines

Please design circuits that will allow the detection of, and detect, errors occurring in the cable. When an error is detected, ensure that no action will be taken, i.e., ensure that no output LED will be lit. When an error is not detected, please allow the circuit to function normally.

A more experienced engineer recommends building four subcircuits, organized either as shown in Figure 1 or Figure 2. Please do not share gates between the portions of the system on the panel side of the cable and the actuator side of the cable.

1. The Parity Generator will be inserted between the encoder and the cable. It will generate an additional parity signal for later use in error detection. Its output is Y. **Please use an LED to display Y.**

2. The Error Injector will be inserted between the Parity Generator and the cable. Although it won't be used during normal operation, the Error Injector will allow you to simulate errors on the encoded signal wires.

3. The Error Detector will be inserted between the cable and the decoder. It will use the three encoded signal wires, along with the parity wire, to determine whether a transmission error occurred, i.e., whether the signals received at the one end of the cable differ from those produced at the other end. Its output is E. **Please use an LED to display E.**

4. The position of the Error Masker is a bit more complicated. It will use E to prevent any output signal from being activated when any cable errors have occurred. It could be implemented by using five two-input AND gates. Each will have $\overline{E}$ and one of the button pressed signals (H, C, P, S, and D) as inputs. It is also be possible to use gates on the encoded signals, to ensure that the *no action* signal is present on the inputs of the decoder if an error occurs. For example, if the *no action* signal were encoded as $\overline{J}\,\overline{K}\,\overline{L}$, then ANDing L, K, and L with $\overline{E}$ would ensure that no output signal will be generated if a cable error has occurred.

5 Theory

The following exercises must be completed and handed in with the laboratory report.

Consider a digital bus composed of n one-bit communication wires, $i_1 \cdots i_n$. If you add an additional communication wire, Y that is set to 1 if an odd number of other wires are 1, and 0 if an even number of other wires are 1, then when you consider all wires, $i_1 \cdots i_n, Y$, the total number of wires set to 1 will always be even.

1. Prove that the number of active wires will always be even for $n = 3$ (four wires total, including Y).
2. Write a formula for $Y(i_1, i_2)$.
3. What gate may be used to implement $Y(i_1, i_2)$?
4. Show how to build $Y(i_1, i_2, i_3)$ using only two-input Ys.
5. Prove that adding Y makes a single error detectable, i.e., prove that, if the signal on exactly one wire (including Y) is inverted after the generation of Y, then the number of wires that are active will not be even.
6. Prove that adding Y does not make double errors detectable, i.e., prove that, if the signals on exactly two wires (including Y) are inverted after the generation of Y, then the number of wires that are active may be even.
7. Error Injector: $W(j_1, j_2)$ outputs j_1 if $j_2 = 0$ and $\overline{j_1}$ if $j_2 = 1$. You'll need four of these (along with input switches and pull-down resistors) to be able to inject errors in four wires.
8. Error Detector: Design a circuit that will detect a single error for $n = 3$, i.e., design $Y(k_1, k_2, k_3, k_4)$.

6 Notes

In addition to the parts used to implement Lab Two, my design required 2 LEDs, 2 330 Ω resistors, and four integrated circuit packages. We're far enough along, now, that I think you can figure out which packages will do the job. Please use in-class questions, office hours, and the mailing list if you need more guidance. Starting from lab two, wiring up this lab is likely to take between 1.5 and 2 hours.

7 Requirements

Prepare a laboratory report. This report should contain the following information.

- A problem statement or objective for the laboratory assignment
- Anything you used in achieving this objective, e.g., truth tables or algebraic simplification, etc.
- A list of the parts required for the circuits you implemented

- Schematic diagrams of the circuits you implemented
- A brief discussion of how you verified that the implementation meets the requirements
- Comments and observations
- You are encouraged to do a floorplan diagram before starting

In addition, please give short answers to the following questions (ungraded)

1. How long did you spend on design
2. How long did you spend on implementation
3. How true are the following statements on a scale of 1 to 5? If any related comments spring to mind, please make them. Your answers won't have any impact on your grade. I'm just trying to figure out whether the labs are good or not.

   (a) I can see where I might some day use the the types of design skills developed in this lab in my work

   (b) This lab gave me a chance to think through portions of the design process on my own instead of handing me all the solutions

   (c) This lab required me to figure out too much on my own – it didn't give enough guidance

   (d) The balance of between theory and implementation was good (if not, what should be stressed more next time around?)

The lab will be graded as follows:

Component	Weight
Circuit quality	5
Report clarity	2
Derivation and schematic	1
Layout style and neatness	1
Correct LED and switch use (resistors, etc.)	1