Laboratory assignment four
Two's-complement arithmetic
EECS 203

Lab due on 7 May
Updated by Robert Dick (based on an existing lab)

Please carefully review lecture four before starting this assignment. If you make catastrophic wiring mistakes, this could result in be exploding integrated circuits sending chunks of plastic into your forehead.

In this laboratory assignment, you will be building a device capable of adding and subtracting three-bit two's-complement numbers.

Please show your work in your lab report.

1 Assignment

In lab two and three, I told stories to illustrate why encoding, decoding, and error correction are useful. I hope those stories were useful. However, I assume everybody already knows why adding and subtracting are useful. In this assignment, you'll be building a device to do arithmetic. Similar devices are found in calculators and microprocessors. I'll get right to the point. Build a device with the following inputs

1. a: a three-bit (a_2, a_1, a_0) two's complement number
2. b: another three-bit (b_2, b_1, b_0) two's complement number
3. s: a one-bit input indicating whether to add (0) or subtract (1)

and the output j, a four-bit (j_3, j_2, j_1, j_0) two's complement number.

$$j = \begin{cases} a + b & \text{if } \overline{s}\,, \\ a - b & \text{if } s. \end{cases}$$

Please put switches and LED displays on all the input lines, and put LED displays on all the output lines. I strongly recommend using a ripple-carry (cascaded carry-chain) design style. Check your design carefully. Subtle errors are common for this problem.

2 Theory

1. What happens when you use your design to subtract 1 from 0? If your answer is 7, then you have a bit more work to do.
2. How do you convert the three-bit two's complement number 010 (2) to a four-bit two's complement number?
3. How do you convert the three-bit two's complement number 110 (-2) to a four-bit two's complement number?
4. How do you convert any three-bit two's complement number to a four-bit two's-complement number?
5. If no overflow/underflow occurred, then you should generate j_3 using the method you found in (4).
6. If an overflow/underflow occurred, you already have a four-bit two's-complement number, with the j_4 being the carry-out of the three-bit adder/subtracter.

3 Requirements

Prepare a laboratory report. This report should contain the following information.

- A problem statement or objective for the laboratory assignment
- Anything you used in achieving this objective, e.g., truth tables or algebraic simplification, etc.
- A list of the parts required for the circuits you implemented
- Schematic diagrams of the circuits you implemented
- A brief discussion of how you verified that the implementation meets the requirements
- Comments and observations
- A circuit floorplan (optional)

The lab will be graded as follows:

Component	Weight
Circuit quality	5
Report clarity	2
Derivation and schematic	1
Layout style and neatness	1
Correct LED and switch use (resistors, etc.)	1