Introduction to Computer Engineering – EECS 203

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Outline

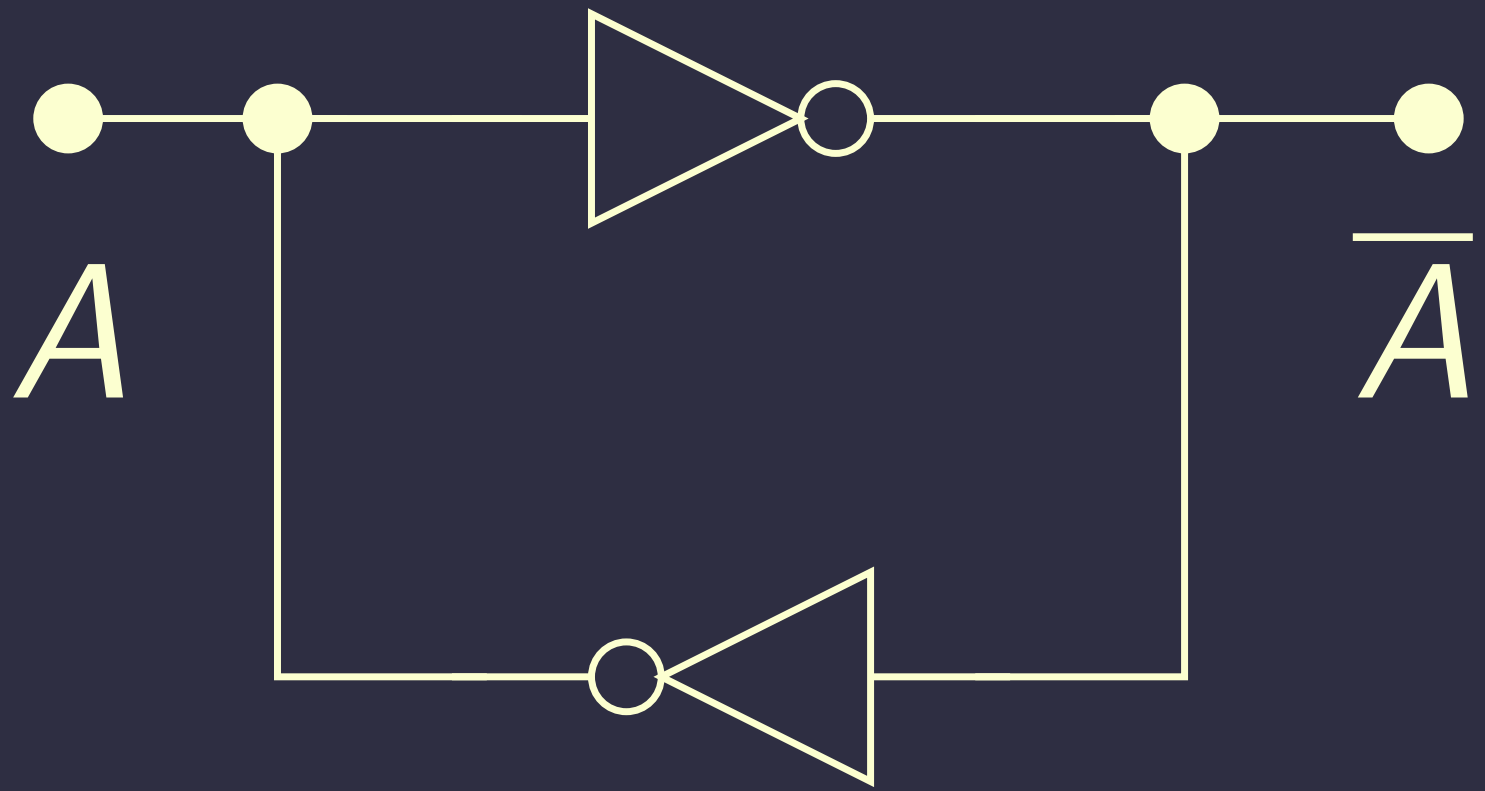
Memory

- Combinational logic outputs a function of inputs, only
- Sequential logic outputs a function of inputs and *state*
- State is remembered
- Consider a sequential vending machine

Flip-flop introduction

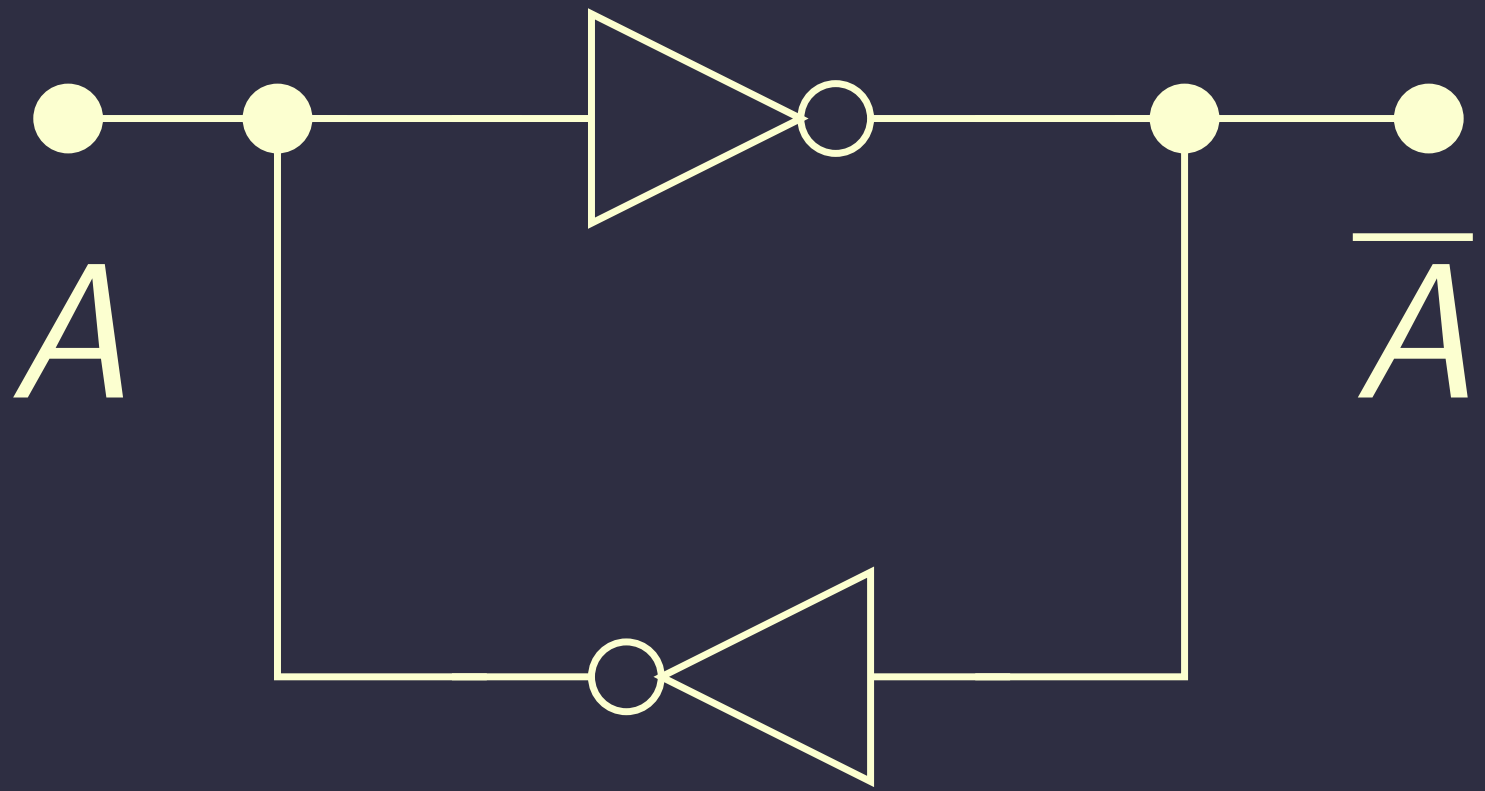
- Stores, and outputs, a value
- Puts a special clock signal in charge of timing
- Allows output to change in response to clock transition
- More on this later
  - Timing and sequential circuits

Feedback and memory



- Feedback is the root of memory
- Can compose a simple loop from NOT gates

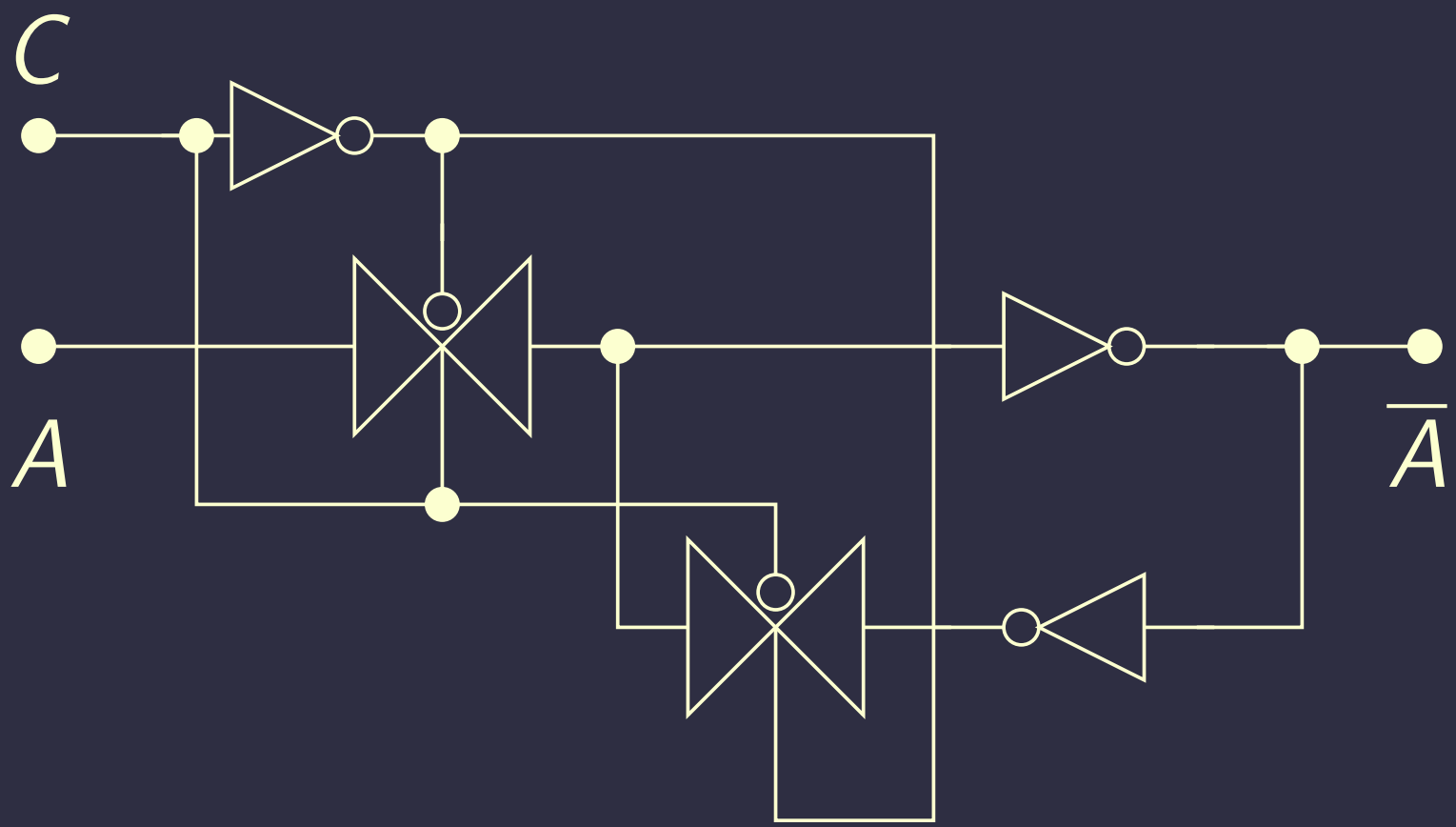
Feedback and memory



- Feedback is the root of memory
- Can compose a simple loop from NOT gates
- However, there is no way to switch the value

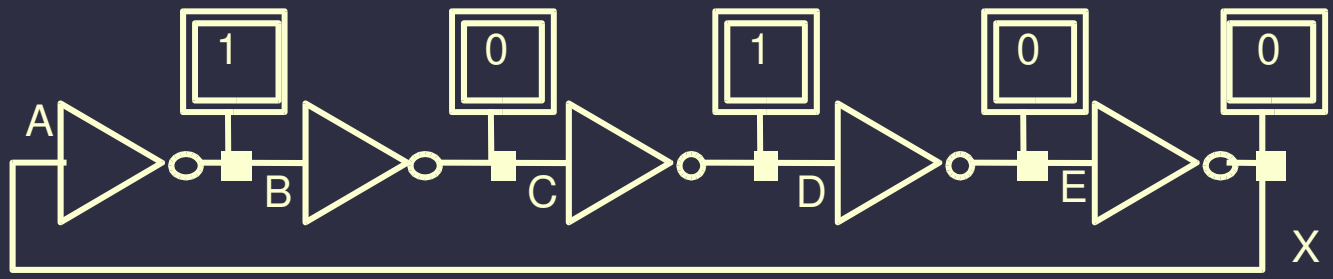
Outline

TG and NOT-based memory



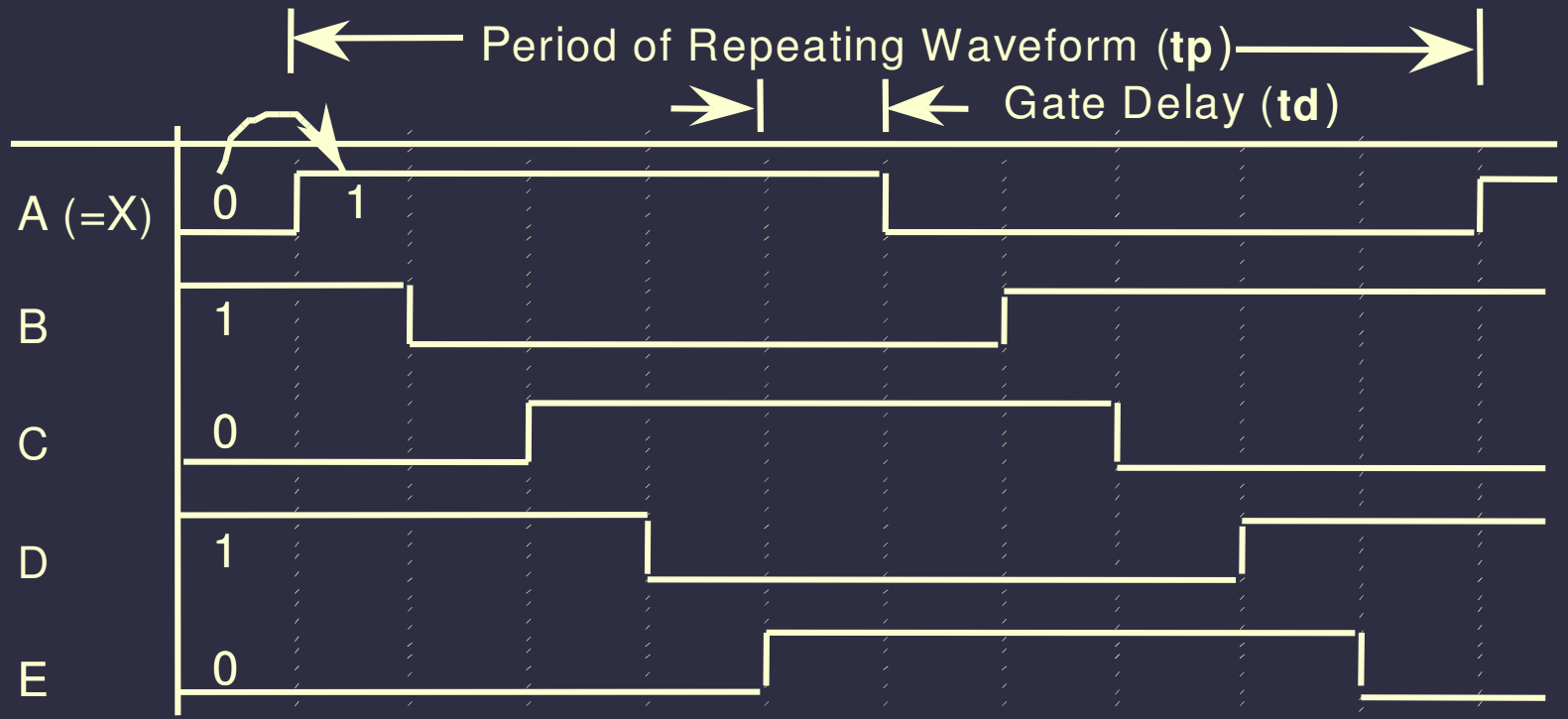
- Can break feedback path to load new value
- However, potential for timing problems

Ring oscillators

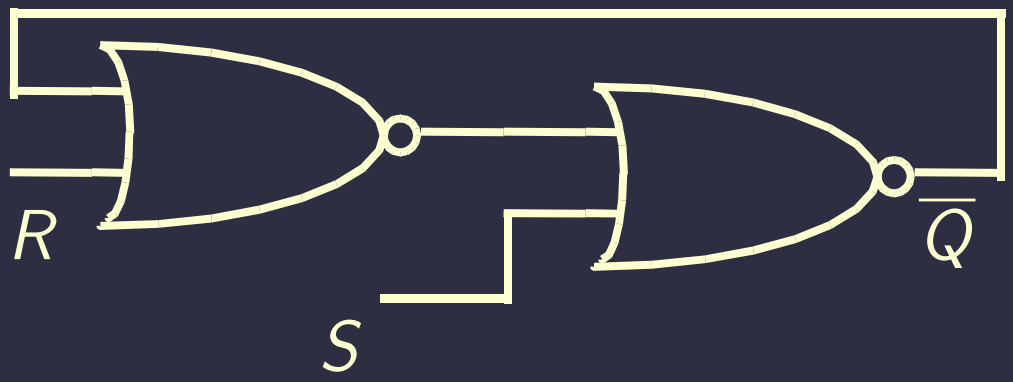


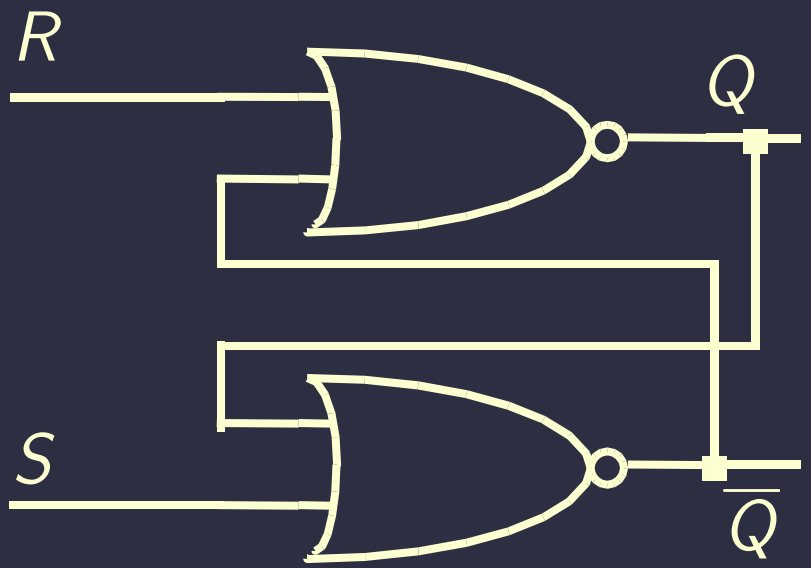
Like pulse shaping circuits with memory

Ring oscillators

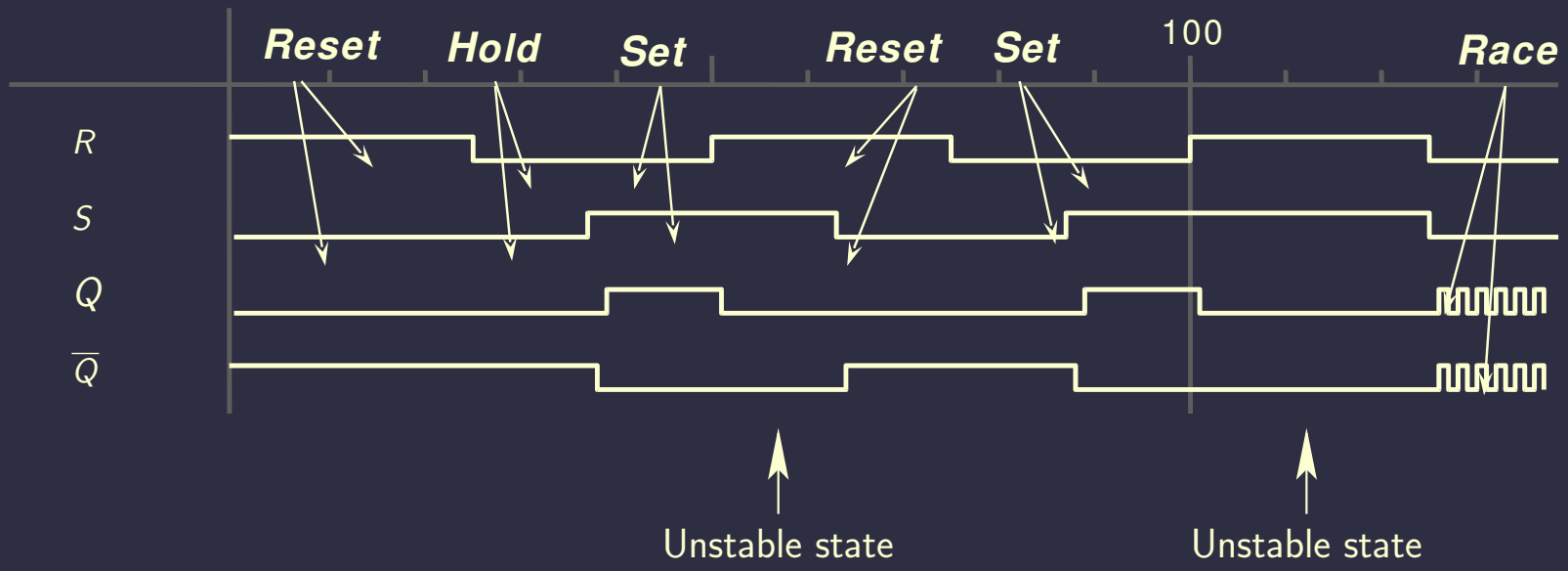


Reset/set latch



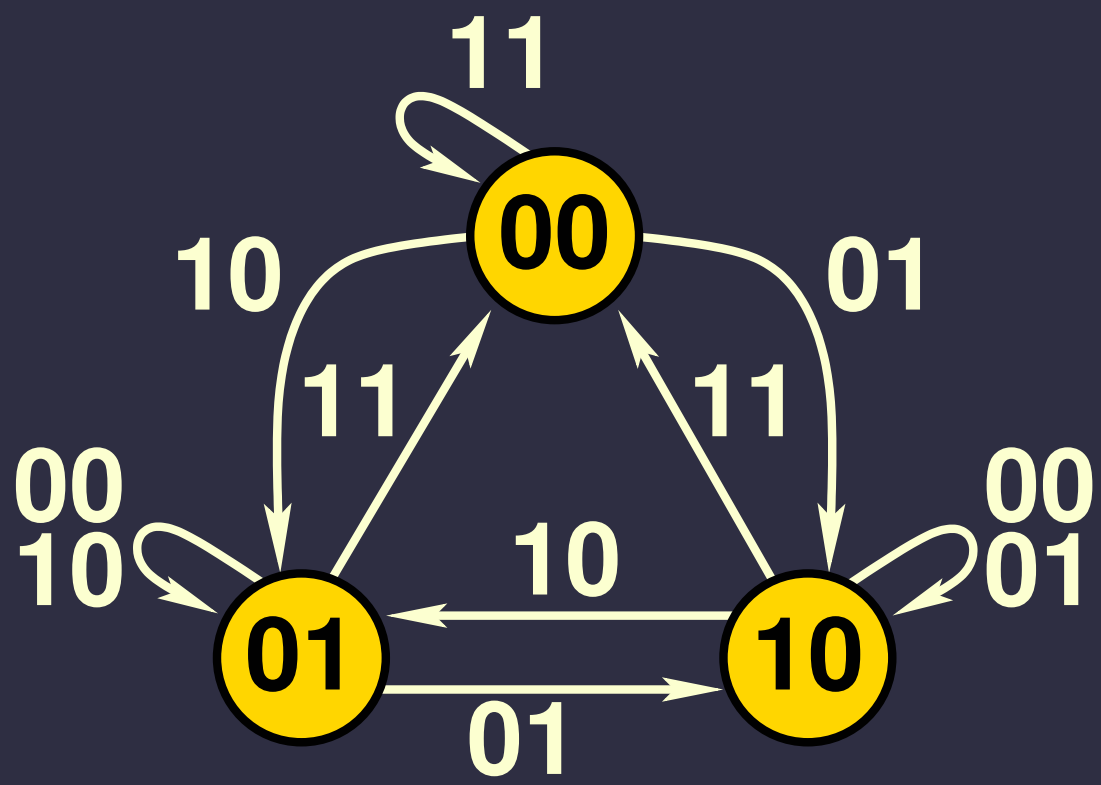


Reset/set timing



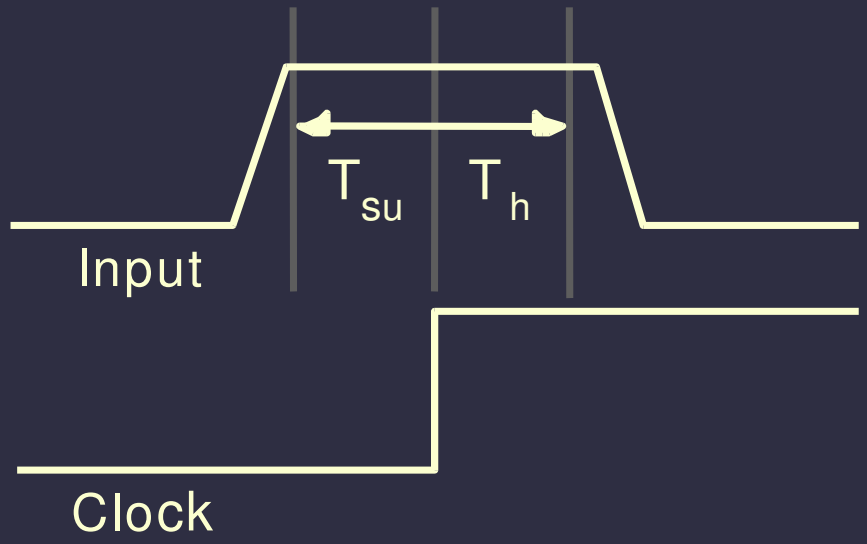
RS latch state diagram

output$=Q\ \overline{Q}$
input$=R\ S$



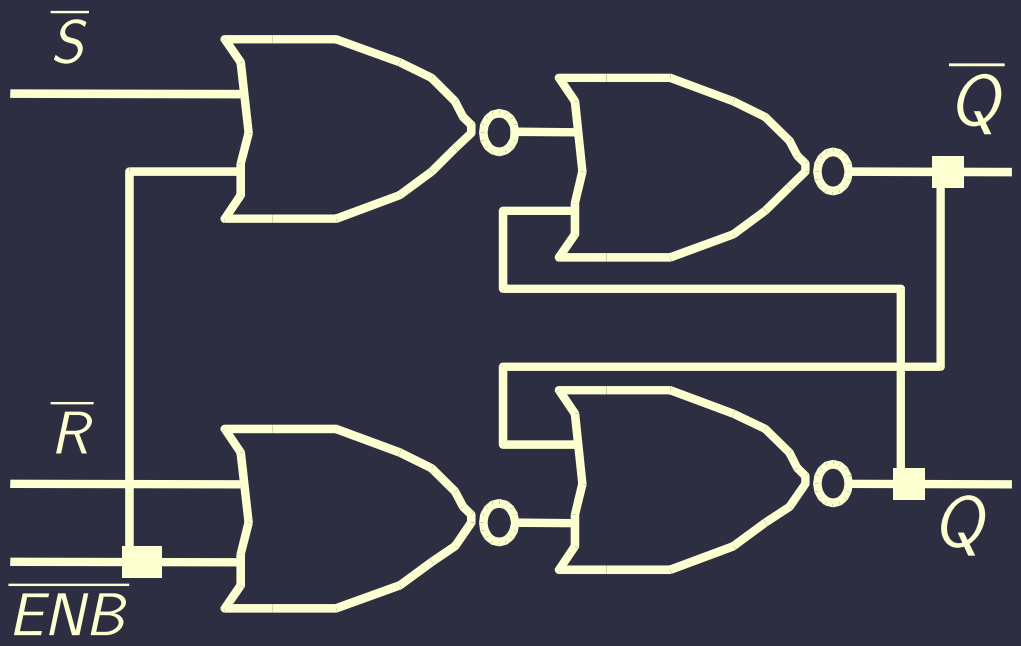
Outline

Clocking terms

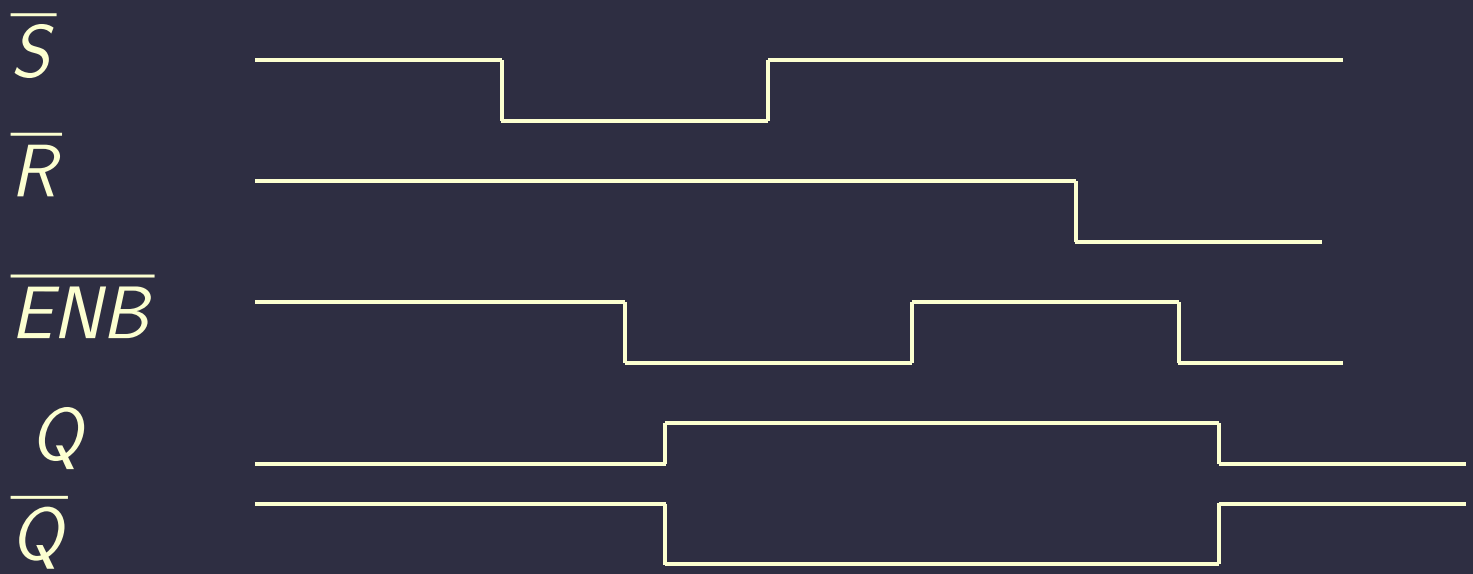


- Clock – Rising edge, falling edge, high level, low level, period
- Setup time: Minimum time before clocking event by which input must be stable (T_{SU})
- Hold time: Minimum time after clocking event for which input must remain stable (T_H)
- Window: From setup time to hold time

Gated RS latch



Gated RS latch

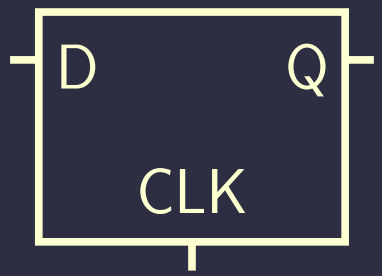


Memory element properties

Type	Inputs sampled	Outputs valid
Unclocked latch	Always	LFT
Level-sensitive latch	Clock high (T_{SU} to T_H) around falling clock edge	LFT
Edge-triggered flip-flop	Clock low-to-high transition (T_{SU} to T_H) around rising clock edge	Delay from rising edge

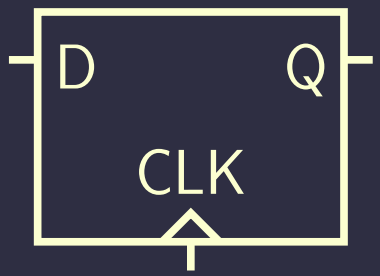
Clocking conventions

Active-high transparent



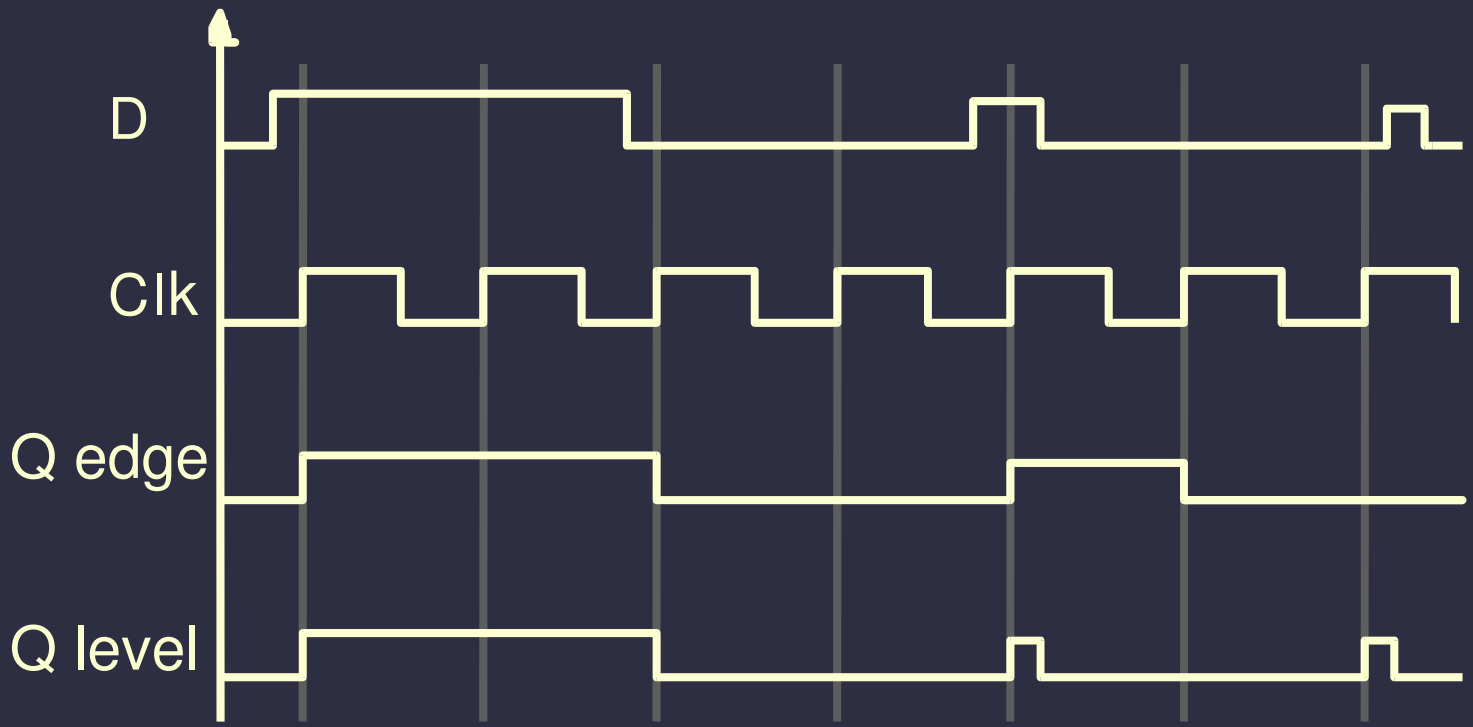
Active-low transparent

Positive (rising) edge



Negative (falling) edge

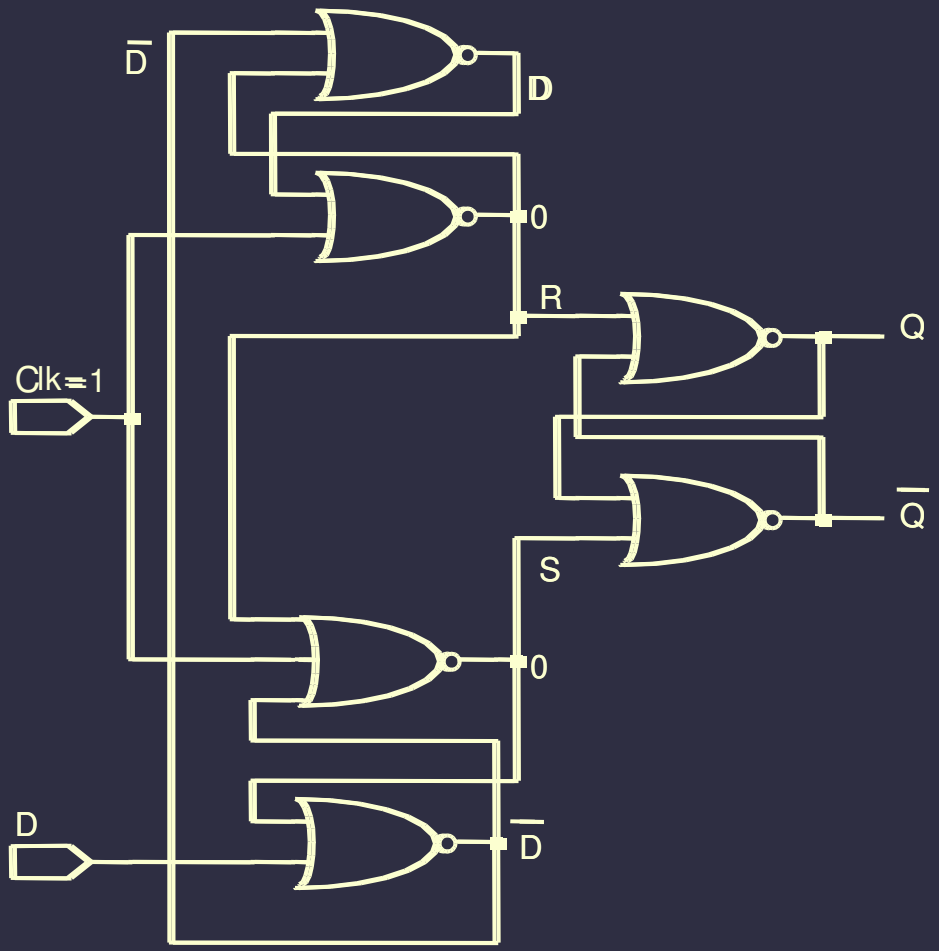
Timing for edge and level-sensitive latches



Falling edge-triggered D flip-flop

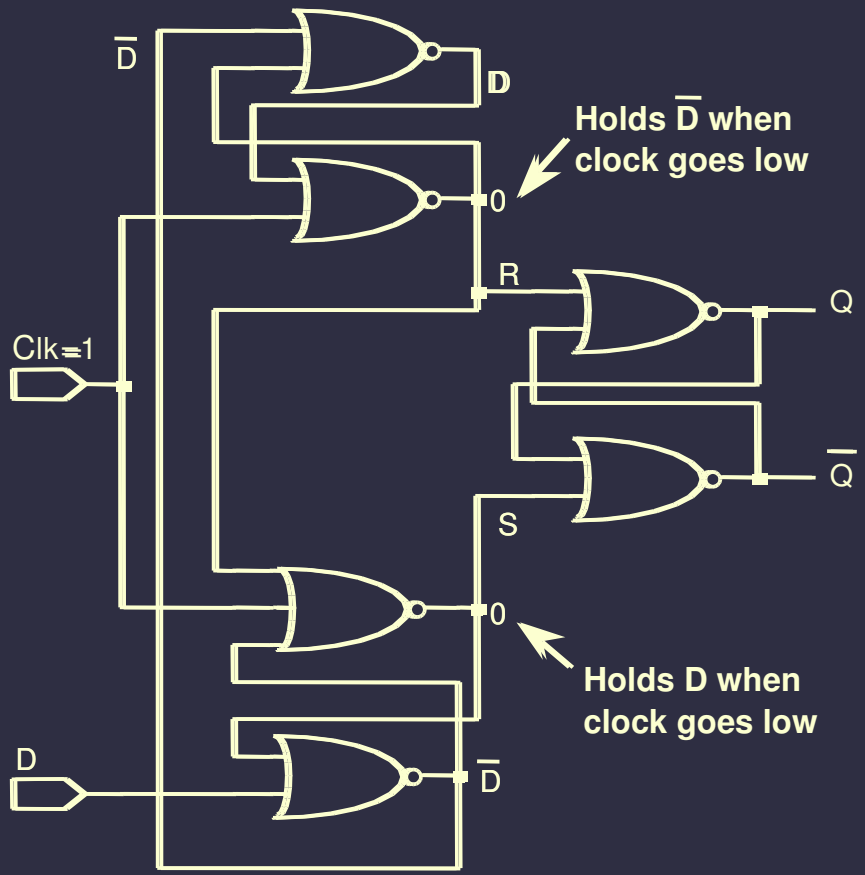
- Use two stages of latches
- When clock is high
  - First stage samples input w.o. changing second stage
  - Second stage holds value
- When clock goes low
  - First stage holds value and sets or resets second stage
  - Second stage transmits first stage
- $Q^+ = D$
- One of the most commonly used flip-flops

Falling edge-triggered D flip-flop



Clock high

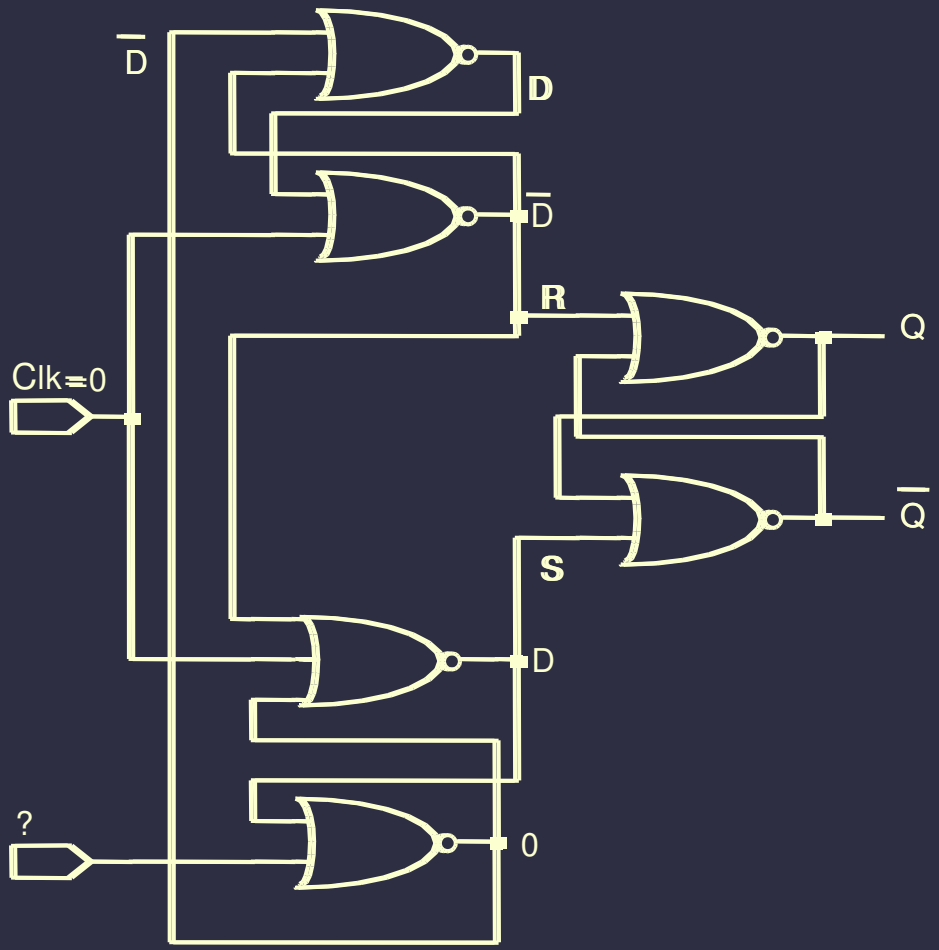
Falling edge-triggered D flip-flop



Clock switching

Inputs sampled on falling edge, outputs change after falling edge

Falling edge-triggered D flip-flop



Clock low

Summary

- Memory
- Latches
- Flip-flops (more on these later)

Outline

Reading assignment

- M. Morris Mano and Charles R. Kime. *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, fourth edition, 2008
- Sections 5.1–5.7
- Sections 6.1–6.4

Computer geek culture reference

Computer security

- PGP
- (Open)SSH
- (Type II) remailers
- Wireshark
- Crack