Introduction to Computer Engineering – EECS 203

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Pace, lab expectations

- Anybody falling behind?
- If something isn't making sense, stop me and I'll elaborate using the chalkboard
  - I'm glad to do it!
- Lab expectations (lab two and above)
  - Complete schematics
  - Easy to debug, color-coded wiring
  - Terse but clear description

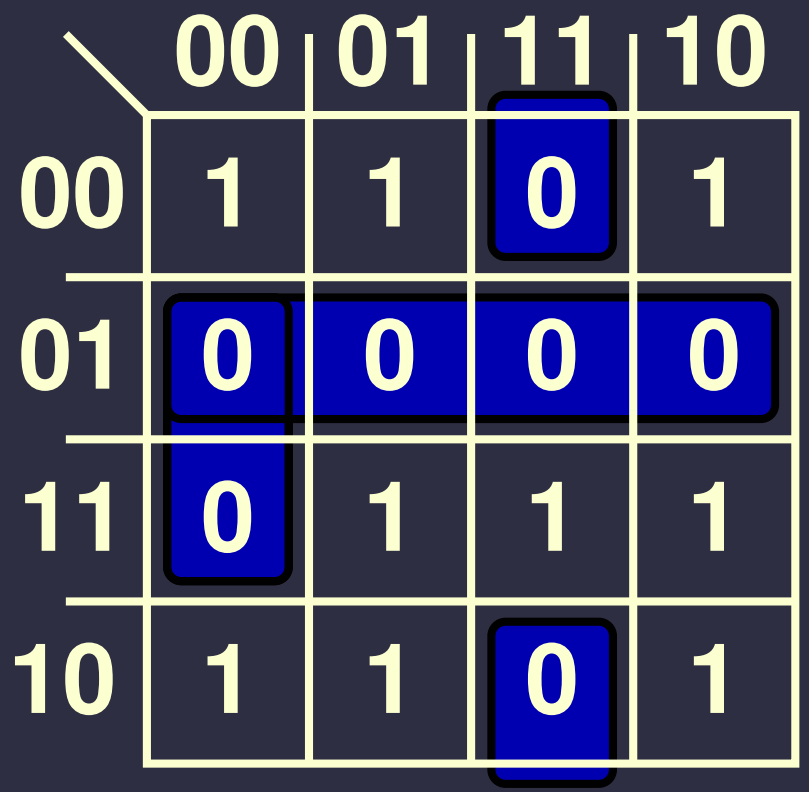
Outline

Review: Minimization techniques

Advantages and disadvantages?

- Algebraic manipulation
- Karnaugh maps
- Quine–McCluskey
- Advanced topic: Kernel extraction
- Advanced topic: Heuristic minimization, e.g., Espresso

Deriving POS



Find SOP form for zeros:

$$\overline{f} = ab\overline{z} + \overline{c}\,d + \overline{a}\,\overline{b}\,d$$

Deriving POS

Apply De Morgan's theorem

$$\overline{f} = ab\overline{d} + \overline{c}\,d + \overline{a}\,\overline{b}\,d \quad (1)$$

$$\overline{\overline{f}} = \overline{ab\overline{d} + \overline{c}\,d + \overline{a}\,\overline{b}\,d} \quad (2)$$

$$f = \overline{\left(ab\overline{d}\right)} \cdot \overline{\left(\overline{c}\,d\right)} \cdot \overline{\left(\overline{a}\,\overline{b}\,d\right)} \quad (3)$$

$$f = \left(\overline{a} + \overline{b} + d\right)\left(c + \overline{d}\right)\left(a + b + \overline{d}\right) \quad (4)$$

- Advanced topic: Read the POS expression directly from the Karnaugh map
  - More difficult

Quine–McCluskey two-level logic minimization

- Compute prime implicants with a well-defined algorithm
  - Start from minterms
  - Merge adjacent implicants until further merging impossible
- Select minimal cover from prime implicants
  - Unate covering problem
- What is happening?
  - $ab + a\overline{b} = a$

Computing prime implicants

$\Sigma = 0$	**0000**
$\Sigma = 1$	**0001** **0010** **1000**
$\Sigma = 2$	**1001** **1010**
$\Sigma = 3$	**1101** **1110**
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Computing prime implicants

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Summary

- Review: Minimization overview
- Review: Karnaugh map SOP minimization
- POS using SOP K-map trick
- Quine-McCluskey optimal two-level minimization method

Next lecture – More advanced building blocks

- Encoders and decoders
- MUXs
- Advanced TG techniques

Outline

Reading assignment

- M. Morris Mano and Charles R. Kime. *Logic and Computer Design Fundamentals*. Prentice-Hall, NJ, third edition, 2004
- Sections 2.7–2.10
- Sections 4.1–4.5
- Section 4.6 (decoders and multiplexers only)

Additional references

- If QM doesn't click, please also see the following references
- Randy H. Katz. *Contemporary Logic Design*. The Benjamin/Cummings Publishing Company, Inc., 1994: pp. 85–88
- John P. Hayes. *Introduction to Digital Logic Design*. Addison-Wesley, MA, 1993 pp. 320, 321
- You can get these from me or the library

Computer geek culture reference

http://www.deepchip.com/