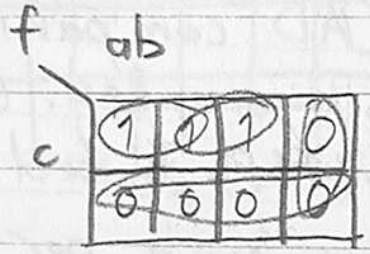
ECE 303 Fall 2003 Final Exam Solutions

1) Unate covering: Use Espresso heuristics instead of optimal Quine-McCluskey approach.
Binate covering: Use dynamic programming for tech. mapping after converting DAGs to trees instead of binate covering formulation.

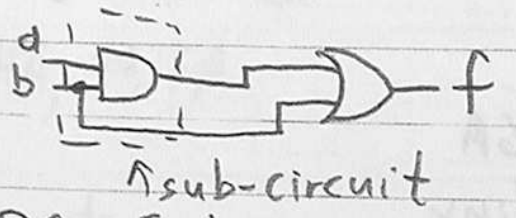
2)



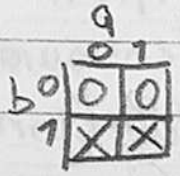
$f = \bar{a}\bar{c} + b\bar{c}$

$f = (\bar{a} + b) \cdot (\bar{c})$

3)



DC if b.



4) VHDL: Supports system-level design (A).
Hard to learn (D).

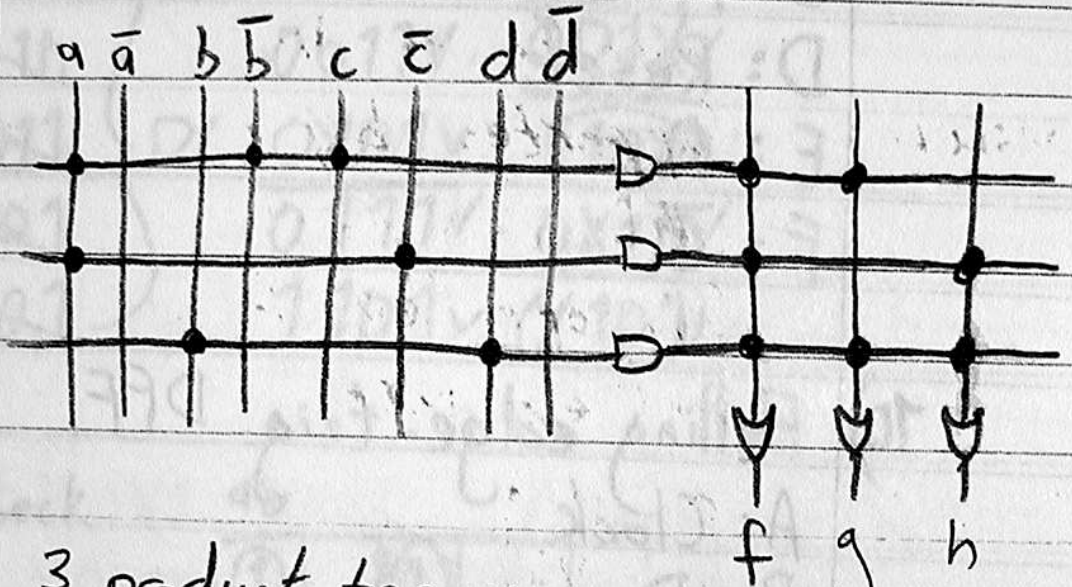
Verilog: Easy to learn (A).
Doesn't support system-level design very well (D).
(However, System Verilog does.)

SystemC: Supported by numerous CAD companies (A).
SW-oriented. Generally not expected to yield as high performance as VHDL (D).

5) a) FPGA
b) Xilinx
c) Configurable logic blocks (CLBs)
d) Functions of about 4 or 5 variables. However, can vary by family.
e) Heterogeneous.
f) Reconfigurable through switches.

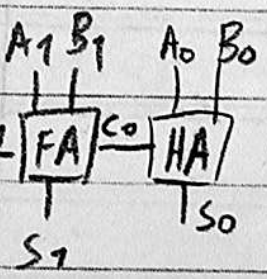
6) f: ab / cd

$f = a\bar{b}c + a\bar{c} + bd$



3 product terms

7) 1 HA, 13 FA



8) Decoder

I: Control input

O: Output

9) JK flip-flop w. active-high asynchronous reset, rising edge trig.

A: Clock
B: J
C: K
D: Reset
E: Q
F: $\overline{Q}$

10) Falling edge-trig DFF.

A: Clock
B: D
C: Q

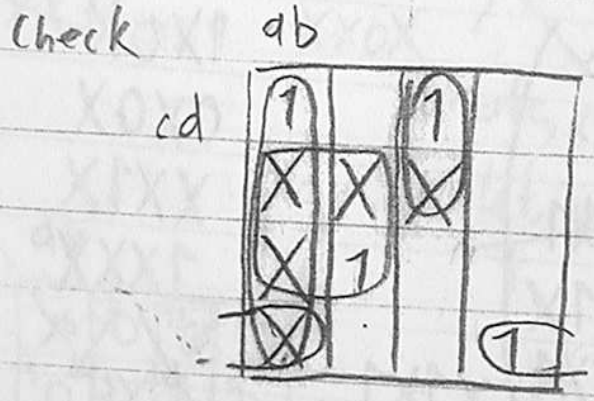
11)

0000	0000 ✓	000X ✓	(00XX)
0111	0001 ✓	00X0 ✓	(0XX1)
1010	0010 ✓	00X1 ✓	
1100	1010 ✓	0X01 ✓	
	1100 ✓	(X010)	
0001	0011 ✓	001X ✓	
0010	0101 ✓	(10X)	
0011	0111 ✓	0X11 ✓	
0101	1101 ✓	(X101)	
1101			

on

DC

check



11)

	X010	110X	X101	00XX	0XX1
0000				1	
0111					1
1010	1				
1100		1			

$$f = \bar{b}c\bar{d} + ab\bar{c} + \bar{a}\bar{b} + \bar{a}d$$

12) a)

1X0X
0X01
~~X1X1~~
X11X
1XX1

X1X1

$$1X0X = 0X0X = XX1X = 1XXX$$

$\bar{a}$ / a

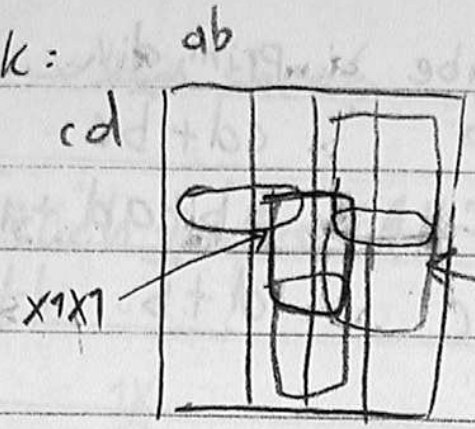
not relatively essential

XX0X XX0X
XX1X XX1X
$\bar{c}$ / c XX1X

XXXX XXXX XXXX
taut. taut $\bar{c}$ / c

XXXX XXXX
XXXX XXXX
taut. taut.

12) a) check:



$a\bar{c}$

$\bar{a}\bar{c}d$

bd

bc

ad

12) b) $(1X0X)$ $(0X01)$ $(X1X1)$ $(X11X)$ ~~$(1XX1)$~~ $1XX1$

$(XX0X)$ $(X1XX)$ $(X11X)$ unate in b

$\bar{b}$ ↙ ~~b~~ ✗ $XX0X$

unate, not taut., relatively essential

13) a)

f

cd \ ab	00	01	11	10
00	X (8)	0 (9)	0 (11)	0 (10)
01	0 (4)	X (5)	0 (13)	0 (12)
11	0 (3)	X (7)	1 (15)	X (14)
10	0 (2)	1 (6)	0 (14)	1 (16)

$f = \bar{a}bc + acd + a\bar{b}c$

13)b)

cube	prim. div.	kernel?
a	$cd + \bar{b}c$	no
c	$\bar{a}b + ad + a\bar{b}$	yes
ac	$d + \bar{b}$	yes

If we use $\bar{a}b + ad + a\bar{b}$:

$c(\bar{a}b + ad + a\bar{b})$: 7 lit.

If we use $d + \bar{b}$:

$(d + \bar{b})ac + \bar{a}bc$: 7 lit.

$f = c(\bar{a}b + ad + a\bar{b})$

↑recurse

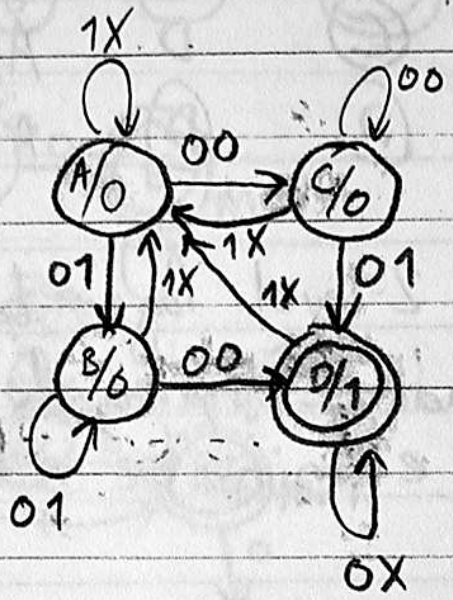
cube	prim. div.	kernel?
a	$d + \bar{b}$	yes

$f = c(a(d + \bar{b}) + \bar{a}b)$: 6 lit.

14)a) See exam sheet.

14)b) No such nodes. All nodes on critical path.

15)a)



15)b) 3 adj. to A → at least 3 state var.

pq

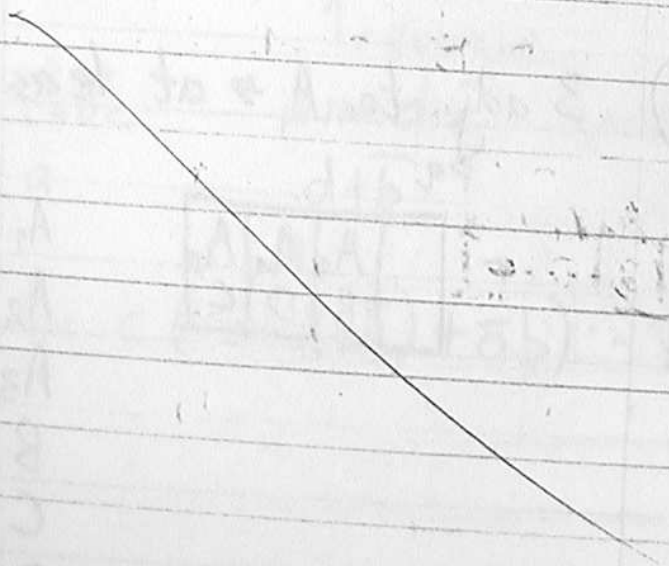
r		A_1	A_2	A_3
		B	D	C

A_1: 010
A_2: 110
A_3: 100
B: 011
C: 101
D: 111

15)b)

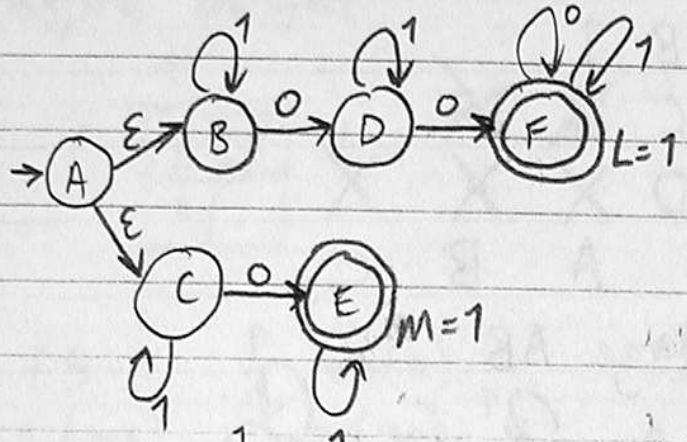
CS	NS 00	01	10	11	Out
A_1	A_2	B	A_1	A_1	0
A_2	A_3	A_1	A_2	A_2	0
A_3	C	A_2	A_3	A_3	0
B	D	B	A_1	A_1	0
C	C	D	A_3	A_3	0
D	D	D	A_2	A_2	1

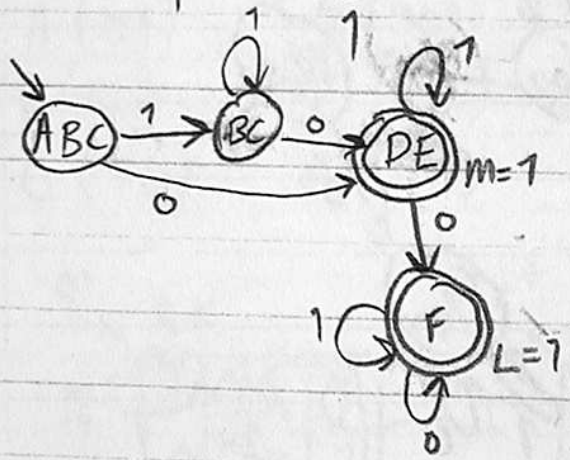
15)c) Use 2-level logic to eliminate dynamic hazards. Cover all transitions to eliminate static hazards.

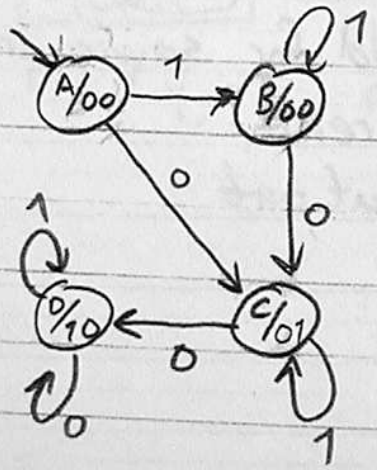


16)a) $1^*01^*0(0+1)^* \leftarrow L$

$1^*01^* \leftarrow M$







CS	0	1	out
A	C	B	0
B	C	B	0
C	D	C	0
D	D	D	1

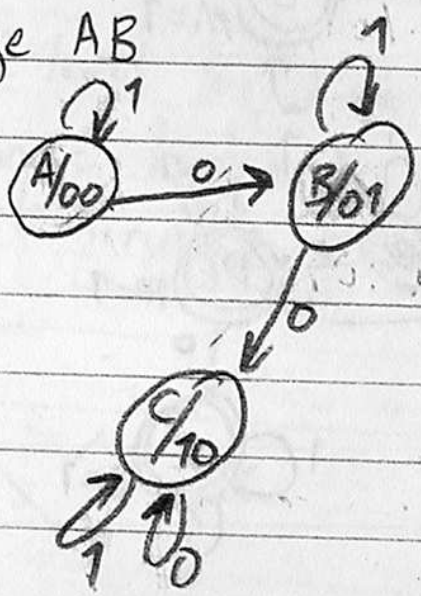
NS

16)b) No. Completely specified FSM.

16)c)

	1		
B	~~BC~~	~~AC~~	
C	~~CD~~	~~AC~~	
D	X	X	X
	A	B	C

Merge AB



16)d) Same child for same input
Same parent
Same output

16)e) BC children, AB, BC parent
AB, AC output

r \ q	B	C
A		

16)f)

CS	NS(0)	NS(1)	
A (01)	B (00)	A (01)	00
B (00)	C (10)	B (00)	01
C (10)	C (10)	C (10)	10

q^+

I \ qr	00	01	11	10
1	0	X	1	
0	0	X	1	

$q^+ = \bar{r}\bar{I} + q$

r^+

I \ qr	00	01	11	10
0	0	X	0	
1	0	X	0	

$r^+ = rI$

L

r \ q	0	1
0		X

$L = q$

M

r \ q	1	0
0	X	

$M = \bar{q}\bar{r}$

16)a)