EECS 303: Advanced Digital Logic Design
Midterm Exam

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Show your work. Derivations are required for credit; end results are insufficient.

1. **(10 pts.)** Mind the minimal two-level **Product of Sums** representation for the following function using a Karnaugh Map

$$f(a,b,c,d) = \sum(0,2,7,10) + d(4,5,6,13)$$

2. **(5 pts.)** Using no more than two sentences, state a primary reason to use a multi-level, i.e., greater than two-level, implementation of a function instead of using a two-level implementation?

3. **(10 pts.)** Assume that you have a computer program exactly implementing the Quine-McCluskey method, and that you supply an n-input parity function to the program. Also assume that the computer program has the (perhaps magical) ability to solve instances of the unate covering problem in time polynomial in the input size. Is the run time of the program polynomial or exponential in the number of function inputs? Think carefully about this and explain your answer using no more than three sentences.

4. **(10 pts.)** Consider the following set of cubes:

$$\{\overline{a}\,\overline{c}, a\overline{c}, \overline{c}d, a\overline{d}, c\overline{d}\}$$

   Given that $\overline{c}d$, $a\overline{c}$, and $a\overline{d}$ are redundant, use a method based on fast tautology checking to determine which cubes are *totally redundant* and which are *partially redundant*. Show your work.

5. **(5 pts.)** Using three or fewer sentences, explain the special useful property of unate covers for tautology checking and explain why this property holds.

6. **(5 pts.)** Would a floating gate based memory technology be non-volatile if the floating gate were separated from the substrate by only three atoms of silicon dioxide? Explain why using no more than two sentences.

7. **(5 pts.)** Approximately how many inputs may a function have, while still being implementable in the most basic logic unit of an FPGA, e.g., a configurable logic block?

8. **(10 pts.)** Using only a few words or, at most, a sentence each, indicate an advantage and disadvantage for each of the following implementation technologies/styles:

   (a) FPGA

   (b) PLA

   (c) EEPROM

   (d) CMOS logic gates

   (e) CMOS transmission gates

9. **(5 pts.)** Show a table for a three-bit Gray code. The table should have two columns: "Number" and "Encoding".

10. **(10 pts.)** Consider the following coding scheme:

Number	Encoding
0	000
1	001
2	010
3	011
4	110
5	111
6	100
7	101

    If a circuit uses this coding scheme on a bus with high-capacitance wires, and increments the value once per cycle upward (wrapping around from 7 back to 0) what is the average energy consumption per cycle? Neglect leakage power consumption and assume that the energy for switching one wire in the bus is e.

11. **(10 pts.)** Using no more than three sentences, explain what the following circuit is and why it might be useful.