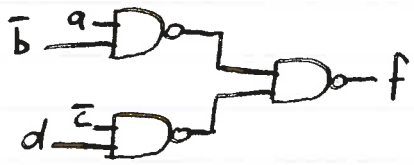
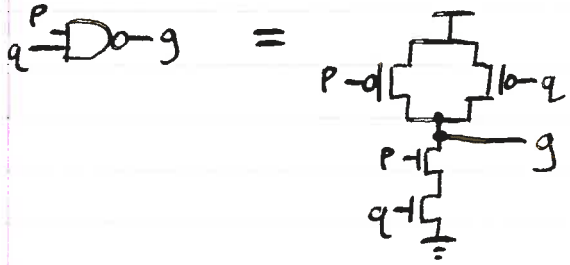
Robert Dick, Fall '08 midterm, EECS 303

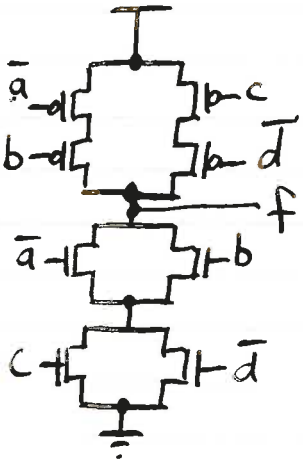
1) $f = a\bar{b} + \bar{c}d = \overline{\overline{a\bar{b} + \bar{c}d}} = \overline{\overline{a\bar{b}} \cdot \overline{\bar{c}d}}$





First, consider pull-up network.
1 iff $a\bar{b} + \bar{c}d$. Inverted control for pull-up.
$\bar{a}b + c\bar{d}$

Pull-down $\overline{a\bar{b} + \bar{c}d}$
$\overline{a\bar{b}} \cdot \overline{\bar{c}d}$
$(\bar{a} + b)(c + \bar{d})$



2) $f = \sum(0,1,5,6) + dc(3,4)$
$\bar{f} = \sum(2,7) + dc(3,4)$

010	Σ_1	010✓	01X
111		100	X11
011	Σ_2	011✓	
100	Σ_3	111✓	

	100	01X	X11
010		1	
111			1

$\bar{f} = \bar{a}b + bc$
$f = \overline{\bar{a}b + bc}$
$f = \overline{\bar{a}b} \cdot \overline{bc}$
$f = (a + \bar{b})(\bar{b} + \bar{c})$

3) The second phase of the Quine-McCluskey method is Unate covering. The DAG-based technology mapping problem is Binate covering. Although both are NP-complete, Binate covering problem instances tend to be harder to solve in practice.

4) In some cases further expansion of a cube is not possible without first reducing the cube.

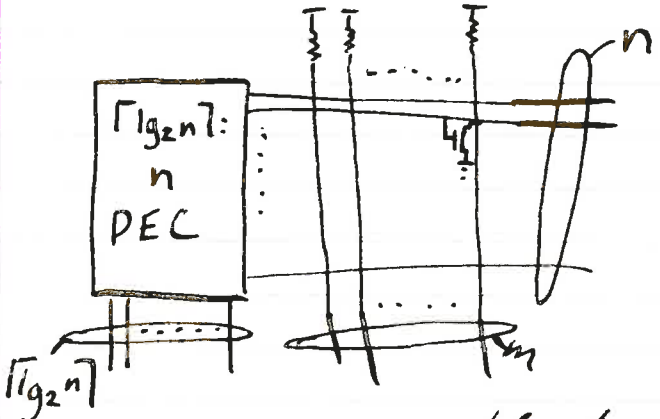
5) Programming would be slower or require higher voltage because tunneling would be reduced.

6)

	a	b	c	d
i	0	1		
j		0	1	
k			0	1
l	1			1

Only column d need be used.

7)



m×n floating gate transistors.

Each output of the decoder is a $\lceil \lg_2 n \rceil$-input AND, or a $\lceil \lg_2 n \rceil$-input NOR. There are n such outputs. We may use up to $\lceil \lg_2 n \rceil$ inverters to get complemented input literals.

$\lceil \lg_2 n \rceil$ inverters $= \lceil \lg_2 n \rceil$ PMOS + $\lceil \lg_2 n \rceil$ NMOS
$n \times \lceil \lg_2 n \rceil$-input NORs $= n \cdot \lceil \lg_2 n \rceil$ PMOS + $n \lceil \lg_2 n \rceil$ NMOS

Result:

$m \times n$ floating gate
$(n+1)\lceil \lg_2 n \rceil$ each of NMOS and PMOS

It is good if you used minimized decoders. That would further reduce transistor count.