EECS 303: Advanced Digital Logic Design
Midterm Exam

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Robert Dick

Show your work. Derivations are required for credit; end results are insufficient. Closed book. No electronic aids.

1. **(10 pts.)** Consider the following function:

$$f(x, y, z) = a\bar{b} + \bar{c}\,d$$

   - Show a gate-level two-level diagram for an implementation of the function composed of NAND and NOR gates.
   - Show the transistor-level CMOS diagram for each type of gate used in the previous diagram.
   - Show a transistor-level diagram for a single CMOS logic gate implementing the function.

2. **(10 pts.)** Use the Quine–McCluskey method to find a minimal POS-form implementation of the following function. An expression is sufficient: you need not show a schematic.

$$f(a, b, c) = \sum(0, 1, 5, 6) + dc(3, 4)$$

3. **(10 pts.)** Is the covering problem formulation of the DAG technology mapping problem harder than, easier than, or the same difficulty as the second phase of the Quine–McCluskey method? Using no more than three sentences, explain why.

4. **(10 pts.)** Using three or fewer sentences, explain why an Espresso-like algorithm that uses only *Irredundant Cover* and *Expand* would be inferior compared to Espresso.

5. **(10 pts.)** If high-κ gate dielectric were used in non-volatile storage floating-gate technology and the gates were thickened to preserve identical MOSFET performance, what impact would this have on programming the device? Use two or fewer sentences.

6. **(10 pts.)** Given that each column has an equal cost, solve the following binate covering problem.

	a	b	c	d
i	0	1		
j		0	1	
k			0	1
l	1			1

7. **(10 pts.)** Consider an m-bit wide ROM with n addresses. How many floating-gate transistors, NMOS, and PMOS transistors will the ROM have as a function of m and n? You may ignore resistors but should consider transistors in the decoder. You may support your argument with expressions and/or diagrams.