

ECE 303 Spring 2003 Final Exam Solutions

1)a) Two-level ensures that dynamic hazards won't occur. It also allows one to eliminate static hazards by covering all 1-1 transitions in SOP or all 0-0 transitions in POS.

1)b) A combination of input values for which the output is irrelevant because the input combination can never occur.

1)c) A PLA has fully general product term selection for its OR array. A PAL only allows a subset of product terms to be used by each OR gate.

1)d) Calculating EFT and LFT.

1)e) Partially specified FSM state minimization
Technology mapping
Phase II of Quine-McCluskey

2) a)

ab

	⁰ X	⁴ 1	¹² 1	⁸ 0
¹ 1	⁵ 1	¹³ 0	⁹ 1	
³ X	⁷ 0	¹⁵ 0	¹¹ 0	
⁶ X	¹⁴ X	¹⁰ X	¹⁶ 0	

$$f = \bar{c}(\bar{a} + \bar{b} + \bar{d})(b + d)$$

2) b) List

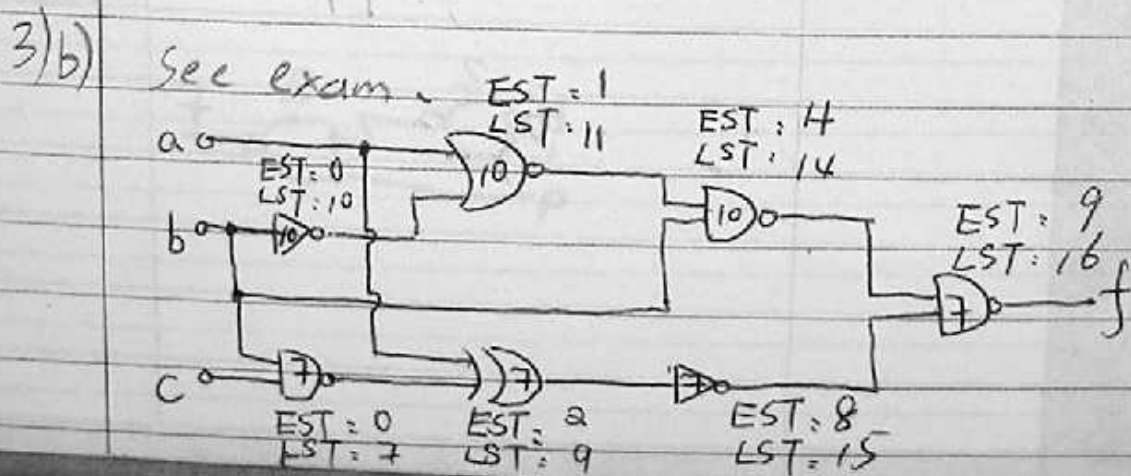
0000v	<u>0000v</u>	000Xv	<u>0X0X</u>
0001v	0001v	<u>0X00v</u>	0X0X
0100v	<u>0100v</u>	X001v	<u>X0X1</u>
0111v	1001v	00X1v	X0X1
1001v	1010v	0X01v	<u>0XX1</u>
1010v	0011v	<u>010Xv</u>	0XX1
0011v	<u>0101v</u>	10X1v	
0101v	0111v	<u>101X</u>	
1011v	1011v	0X11v	
		X011v	
		01X1v	

	101X	0X0X	X0X1	0XX1
0000		1		
0001		1	1	1
0100		1		
0111				1
1001			1	
1010	1			

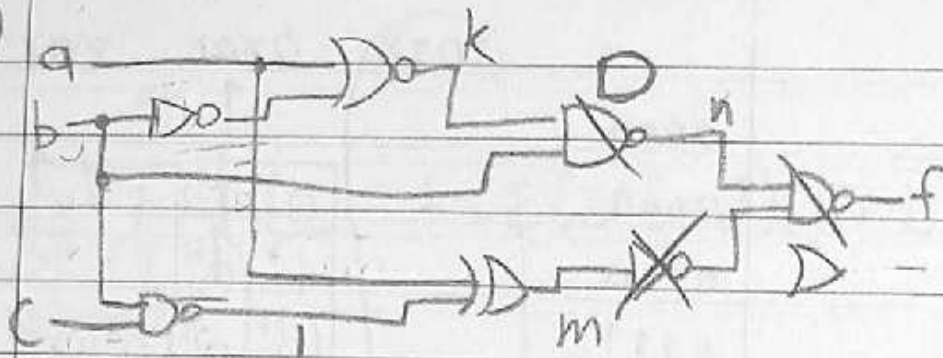
All required

$$f = a\bar{b}c + \bar{a}\bar{c} + \bar{b}d + \bar{a}d$$

3)a) Top path has 10 units of slack
 Bottom has 7 units of slack
 See exam.



3)c)



$$k = \overline{a} + \overline{b} = \overline{a}b$$

$$l = \overline{bc} = \overline{b} + \overline{c}$$

$$m = \overline{a}(\overline{b} + \overline{c}) + a(\overline{b} + \overline{c}) = abc + \overline{a}\overline{b} + \overline{a}\overline{c}$$

$$n = \overline{a}bb = \overline{a}b$$

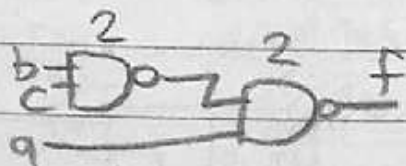
$$f = abc + \overline{a}\overline{b} + \overline{a}\overline{c} + \overline{a}b = abc + \overline{a}$$



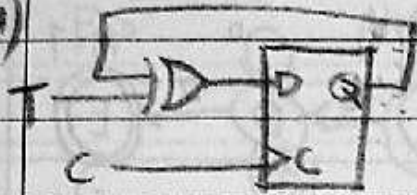
$$= \overline{a} + bc$$

$$= \overline{\overline{\overline{a} + bc}}$$

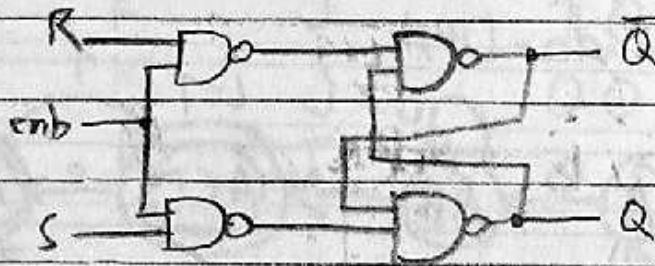
$$= a(\overline{bc})$$



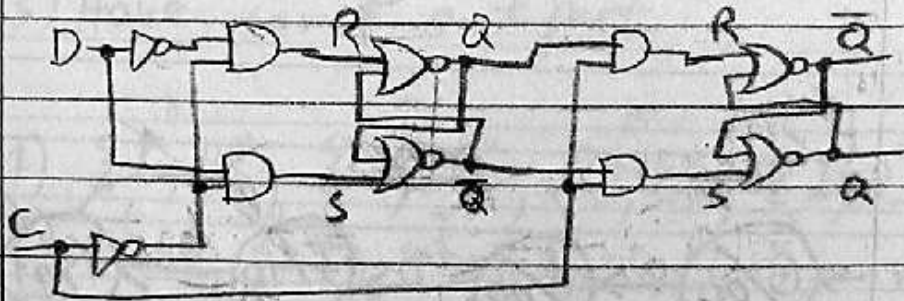
4)a)



4)b)

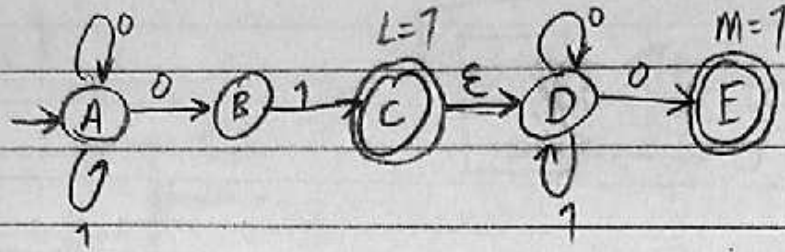


4)c)

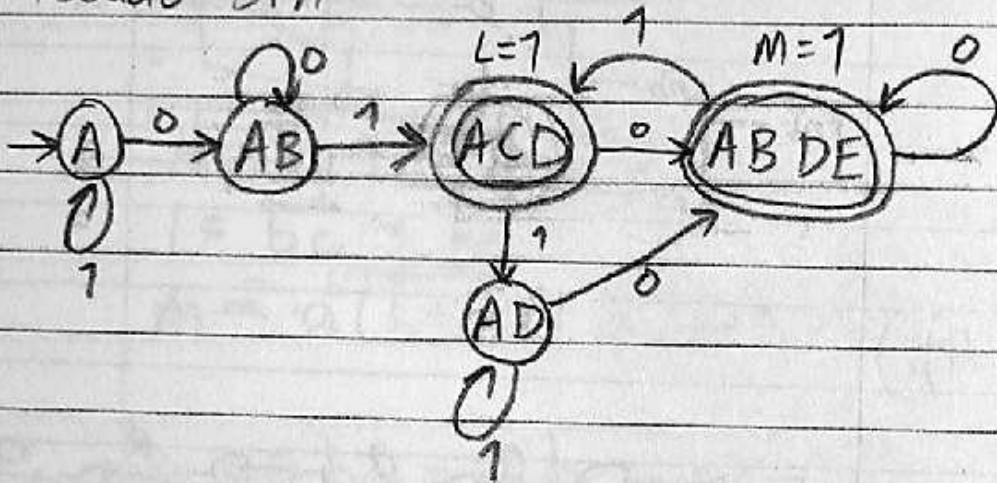


5) a)

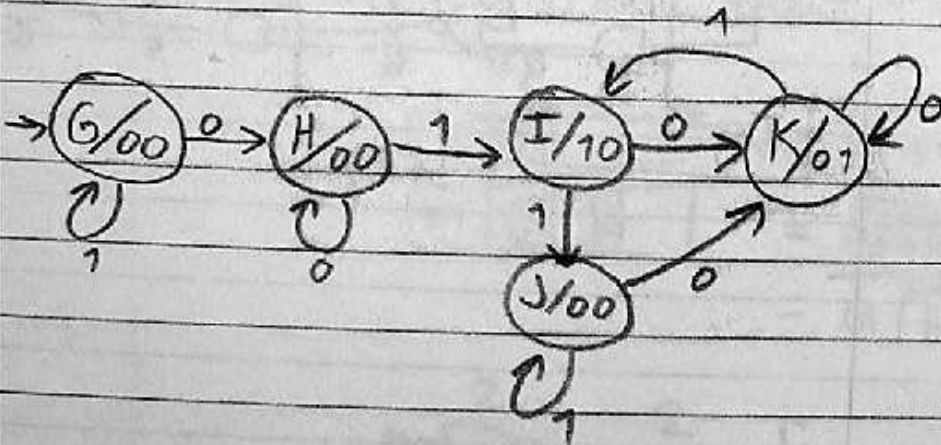
Pseudo-NFA



Pseudo-DFA



FSM



5)b)	PS	NS		LM
		i=0	i=1	
	G	H	G	00
	H	H	I	00
	I	K	J	10
	J	K	J	00
	K	K	I	01

- 5)c)
- 1) Share same child (input)
 - 2) Share same parent
 - 3) Have same output

- 5)d)
- 1) ~~{G, H}~~, ~~{H, K}~~, ~~{J, K}~~, ~~{I, J}~~
 - 2) ~~{G, H}~~, ~~{H, I}~~, ~~{J, K}~~, ~~{K, J}~~, ~~{I, K}~~ cant
 - 3) ~~{G, H, J}~~ decent. can't do output w.o. splitting

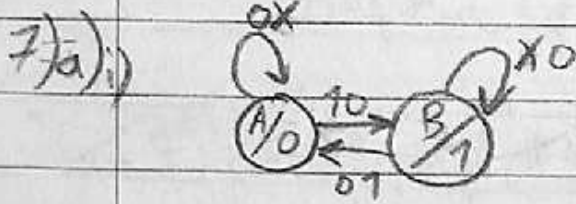
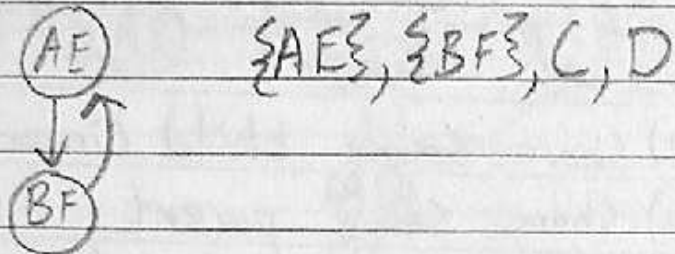


5)e)



6)

B	X				
C	X	A=D			
D	B	X	X		
E	B=F	X	X	A=E	
F	X	A=E	X	X	X
	A	B	C	D	E



7) a) ii) $A=0, B=1$

7) a) iii)

PS	NS(a,b)				Z
	00	01	10	11	
0	0	0	1	X	0
1	1	0	1	X	1

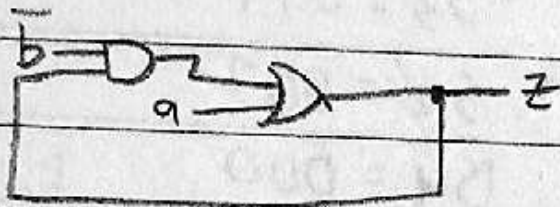
7) a) iv)

q	ab		
	00	01	11
0	0	0	1
1	1	0	1

$$q^+ = a + \bar{b}q$$

$$z = q$$

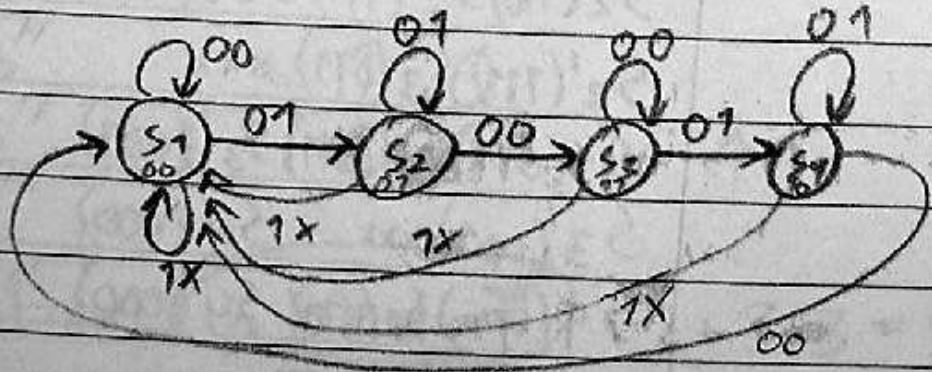
7) a) v)



7) a) vi) SR latch

7) b) i) Moore

7) b) ii)



7) b) iii)

		ab			
		00	01	11	10
0	S_4	S_1	S_2		
1	S_3'	S_3	S_2'		

$$S_1 = 010$$

$$S_2 = 110$$

$$S_2' = 111$$

$$S_3 = 011$$

$$S_3' = 001$$

$$S_4 = 000$$

7) b) iv)

PS	NS (ca)				$Z_1 Z_2$
	00	01	10	11	
$S_1(010)$	$S_1(010)$	$S_2(110)$	$S_1(010)$	"	00
$S_2(110)$	$S_2'(111)$	$S_2(110)$	"	"	01
$S_2'(111)$	$S_3(011)$	xxx	"	"	01
$S_3(011)$	$S_3(011)$	$S_3'(001)$	"	"	11
$S_3'(001)$	xxx	$S_4(000)$	"	"	11
$S_4(000)$	$S_1(010)$	$S_4(000)$	"	"	10

8) see exam

	a	b	c	d	e	f	
IO				1		1	
					1	1	
		1				1	
gates	i			1		1	
	j			1		1	
	k				1	1	
	l				1	1	
	m	1			1		1
	n			1		1	1
	o		1				1
$\bar{d}+b$		1		0			
$\bar{e}+b$		1			0		
$\bar{a}+b$	0	1					
$\bar{c}+b$		1	0				
$\bar{b}+a+d+ce$	1	0	1	1	1		

options $\bar{a}b\bar{c}de\bar{f}$ $2+3+3=8$
 $\bar{a}\bar{b}\bar{c}\bar{d}\bar{e}f$ 9

9)a) design = 2:1 MUX
a = I_0
b = I_1
c = select
d = output

9)b) design = rising edge T flip-flop
a = preset ($A\bar{H}$)
b = clear (AH)
c = clock
d = toggle