ECE 303: Advanced Digital Logic Design
Midterm Exam

3 May 2005

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1. **(25 pts.)** Multilevel minimization

   (a) **(12 pts.)** Use kernel extraction to minimize the following function:

   $$f(a,b,c,d) = \sum(0,3,5,6,10,11,12,13)$$

   You may first use two-level minimization. However, you may not use algebraic manipulation for multi-level minimization.

   Starting from your result for the previous sub-problem, use decomposition to further reduce the literal count.

   (b) **(2 pts.)** How many literals does your kernel extraction result have? How many literals does your kernel extraction and decomposition result have?

   (c) **(3 pts.)** Draw a diagram of your implementation, assuming access to ANDs, ORs, and NOTs. Assume access to complemented and uncomplemented input literals.

   (d) **(3 pts.)** Draw a diagram of your implementation, assuming access to XORs, XNORs, ANDs, ORs, and NOTs. Assume access to complemented and uncomplemented input literals.

2. **(20 pts.)** CMOS implementation

   (a) **(4 pts.)** Use up to three sentences or phrases to explain the impact of reducing sequential circuit frequency upon power consumption, performance, and energy consumption.

   (b) **(4 pts.)** Use up to three sentences or phrases to explain the impact of reducing sequential circuit voltage (V_{DD}) upon power consumption, performance, and energy consumption.

   (c) **(4 pts.)** Use up to three sentences or phrases to describe the difference between leakage (static) power consumption and switching (dynamic) power consumption.

   (d) **(8 pts.)** Show a transistor-level diagram for a minimal transistor count, two-level implementation of the following function:

   $$f(a,b,c) = \sum(0,1,6) + d(5)$$

   You may take advantage of hierarchy by showing how to construct a logic gate and reusing the gate.

Exam continues on reverse side.

3. **(20 pts.)** Complexity

   (a) **(5 pts.)** Use up to three sentences to define the *unate covering problem*.

   (b) **(5 pts.)** Use up to three sentences to define *NP-complete*.

   (c) **(5 pts.)** Assume that you have discovered a polynomial-time solutions to the unate covering problem. Use up to three sentences to explain the implications of your discovery for logic minimization.

   (d) **(5 pts.)** Use up to three sentences to explain the implications of your discovery for all other NP-complete problems.

4. **(20 pts.)** Combinational design

   (a) **(6 pts.)** Use the Quine–McCluskey method to find a minimal SOP expression for the following function:

$$f(a,b,c) = \sum(0,1,5,7) + d(3)$$

   (b) **(4 pts.)** Would a Karnaugh map also have been guaranteed to yield an optimal result for this problem? Use up to three sentences to justify your answer and explain why two-level minimization is, in general, hard.

   (c) **(6 pts.)** Show an implementation of f using a minimal number of 2:1 multiplexors.

   (d) **(2 pts.)** Show an implementation of a 2:1 multiplexor with transmission gates and an inverter.

   (e) **(2 pts.)** Show an implementation of a transmission gate with NMOS and PMOS transistors. Assume access to complemented and uncomplemented input literals.

5. **(15 pts.)** Implementation technologies

   (a) **(10 pts.)** Use a sentence or phrase, each, to describe the following groups of implementation technologies.

   - PALs and PLAs
   - ROMs, PROMs, and EPROMs
   - Flash memory
   - FPGAs
   - Full-custom CMOS implementation

   (b) **(5 pts.)** Use one sentence to describe a ROM. For the technologies following ROM, use one sentence or phrase, each, to indicate how the technology differs from the preceeding one.

   - ROM
   - PROM
   - EPROM
   - EEPROM
   - Flash memory