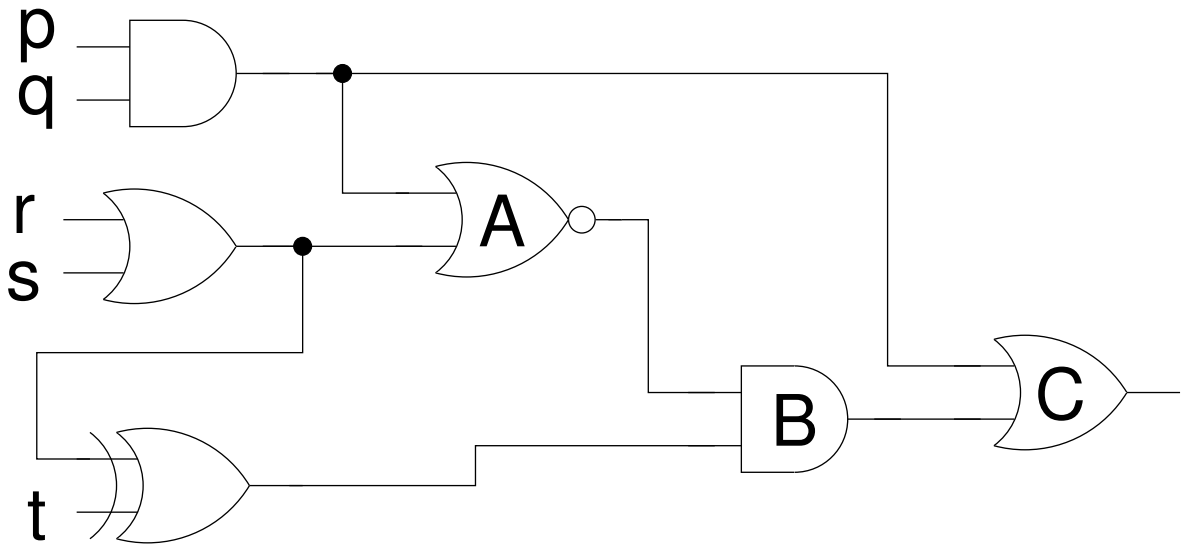
Homework on $\mathcal{D}$ Algorithm

EECS 303: Advanced Digital Logic Design
Assigned 2 December
Due 6 December

You may discuss the assignment with your classmates. However, you need to write down your solutions independently. Please make sure your answers are legible. You can manually produce the circuit diagrams or use a graphics package with a logic gate library, e.g., `xfig`.

1. **(10 pts)** Consider the following circuit:



   (a) Find a set of test vectors capable of testing for a s-a-0 and s-a-1 fault at the output of gate A.

   (b) If gate C were changed to an AND gate, attempt to find a set of test vectors capable of testing for a s-a-0 and s-a-1 fault at the output of gate A. If this is not possible, explain why.

2. **(10 pts)** Find a minimal two-level implementation of the function implemented by the circuit in the preceeding question. Devise test vectors for every s-a-0 and s-a-1 fault that can occur on a gate output. Is it possible to test for all such faults? Why?