Homework two

EECS 303: Advanced Digital Logic Design
Assigned 9 October 2008
Due 16 October 2008

You may discuss the assignment with your classmates.
However, you need to understand and write the solutions independently.

1. **(10 points)** Consider the following functions

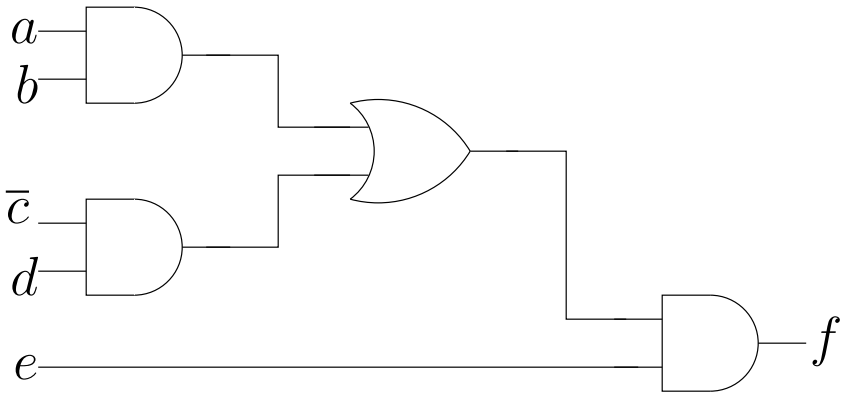
$$f(a,b,c,d) = \overline{a}\,b\overline{c} + \overline{b}\,c + ac + \overline{a}\,\overline{b}\,c\overline{d}$$
$$g(a,b,c,d) = ab + \overline{a}\,bc\overline{d}$$
$$h(a,b,c,d) = \overline{a}\,\overline{b}\,c\overline{d} + \overline{a}\,bc\overline{d}$$

   (a) Draw a diagram for an implementation using a single PLA using a minimal number of AND gates. How many AND gates are required?

   (b) If you were to implement it with a PAL, how many AND gates would be required?

2. **(10 points)** Implement $f(a,b,c) = \sum(0,3,4) + d(2,5,7)$ using a $n:1$ multiplexor where n is minimal. Draw the circuit diagram. What is n?

3. **(10 points)** Reimplement the following network using only NANDs and NORs. Assume there is no cost to invert inputs. You need not globally reorganize the network: local transformation is sufficient. Show a series of three or so circuit diagrams indicating your steps.



4. **(5 points)** Implement an exclusive or gate using steering logic. Assume access to complimented and uncomplimented input literals. Draw a diagram composed only of transmission gates. How many transmission gates are required?

5. **(5 points)** Implement an exclusive or using transmission gates. Assume access to complimented and uncomplimented input literals. Draw a diagram composed only of transmission gates. How many transmission gates are required?