EECS 312: Digital Integrated Circuits
Midterm Exam

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Closed book. Closed notes. Calculators permitted for the purpose of computation, but not storage of notes. I put reference material at the end of the exam.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

Print name:

Show your work. Derivations are required for credit; end results are insufficient. When answers have length limits, these are upper bounds. Shorter correct answers will receive full credit. In fact, shorter answers that are correct and have no errors will receive more credit than longer answers containing flaws.

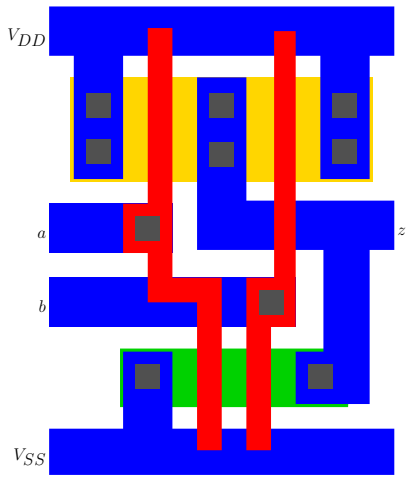
# 1 Knowledge

1. **(5 pts.)** What problem can the inductance in the PCB and package power delivery network cause? When does this problem occur? Use at most four sentences.

2. **(10 pts.)** Why was there a recent transition from using polysilicon gates to using metal gates? Use at most three sentences.

3. **(10 pts.)** Show the side view of the basic memory element used in an EPROM. Using at most two sentences, explain the process of programming it. Using at most two sentences, explain the process of erasing it.

4. **(10 pts.)** What does this layout show? What is its greatest performance irregularity or flaw? In other words, if you were to implement the same function, how would your solution differ? Use at most four sentences.



5. **(10 pts.)** List one problem caused by hot carriers and one profitable use of them. Use at most four sentences.

6. **(5 pts.)** What controls whether carbon nanotubes are metallic or semi-conducting? Use at most one sentence.

## 2 Analysis and Design

7. **(10 pts.)** You designed a CMOS inverter to have a $V_M = V_{DD}/2$. However, its fabrication was not perfect. Impurities mixed in with the acceptor ions introduced strain in the NMOSFET, increasing its carrier mobility by 50%. What is the impact on $V_M$?

8. **(10 pts.)** Generalize the concept of carry-select addition to multiplication. Show the diagram of a carry-select combinational multiplier for two 3-bit numbers. Indicate the impact on performance, assuming that the MUX overhead is negligible. You may use boxes labeled HA, FA, and MUX without showing their transistor-level designs.

9. **(15 pts.)** Draw a diagram of an SRAM with 16 addresses, each of which stores one bit. Take your design down to transistor level, but use hierarchy. Focus on correctness, not efficiency for this question. Your inputs are the four address lines. Implementing the read functionality is sufficient.

10. **(15 pts.)** Determine the period of oscillation for a ring of three balanced inverters with minimal-width NMOSFETs. Explicitly state any simplifying assumptions you make. The diffusion region lengths are all 0.5 µm, but don't assume that my stating this requires that you use it.

**Question 10 was the last question. You are done. Have a good break.**

# 3 Reference material

| | $C_{OX}$ (fF/µm$^2$) | $C_O$ (fF/µm) | $C_j$ (fF/µm$^2$) | $m_j$ | $\phi_b$ (V) | $C_{jsw}$ (fF/µm) | $m_{jsw}$ | $\phi_{bsw}$ (V) |
|---|---|---|---|---|---|---|---|---|
| NMOS | 6 | 0.31 | 2 | 0.5 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 6 | 0.27 | 1.9 | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

# MODELS FOR CMOS DEVICES

**CMOS (0.25 µm) – Unified Model.**

| | $V_{T0}$ (V) | $\gamma$ ($V^{0.5}$) | $V_{DSAT}$ (V) | $k'$ ($A/V^2$) | $\lambda$ ($V^{-1}$) |
|---|---|---|---|---|---|
| NMOS | 0.43 | 0.4 | 0.63 | $115 \times 10^{-6}$ | 0.06 |
| PMOS | –0.4 | –0.4 | –1 | $-30 \times 10^{-6}$ | –0.1 |

**CMOS (0.25 µm) – Switch Model ($R_{eq}$)**

| $V_{DD}$ (V) | 1 | 1.5 | 2 | 2.5 |
|---|---|---|---|---|
| NMOS (kΩ) | 35 | 19 | 15 | 13 |
| PMOS (kΩ) | 115 | 55 | 38 | 31 |

**CMOS (0.25 µm) – BSIM Model**

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

| Name | Value |
|---|---|
| $kT/q$ | 25.875 mJ/C |
| NMOSFET $I_S$ | 21.0 pA |
| PMOSFET $I_S$ | 41.8 pA |
| $n$ (for $I_D$ calculation) | 1.5 |

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\nu_{satp} W_p}{\nu_{satn} W_n}$$

# VALUES OF MATERIAL AND PHYSICAL CONSTANTS

| Name | Symbol | Value | Units |
|---|---|---|---|
| Room temperature | $T$ | 300 (= 27°C) | K |
| Boltzman constant | $k$ | $1.38 \times 10^{-23}$ | J/K |
| Electron charge | $q$ | $1.6 \times 10^{-19}$ | C |
| Thermal voltage | $\phi_t = kT/q$ | 26 | mV (at 300 K) |
| Intrinsic Carrier Concentration (Silicon) | $n_i$ | $1.5 \times 10^{10}$ | $cm^{-3}$ (at 300 K) |
| Permittivity of Si | $\epsilon_{si}$ | $1.05 \times 10^{-12}$ | F/cm |
| Permittivity of $SiO_2$ | $\epsilon_{ox}$ | $3.5 \times 10^{-13}$ | F/cm |
| Resistivity of Al | $\rho_{Al}$ | $2.7 \times 10^{-8}$ | Ω-m |
| Resistivity of Cu | $\rho_{Cu}$ | $1.7 \times 10^{-8}$ | Ω-m |
| Magnetic permeability of vacuum (similar for $SiO_2$) | $\mu_0$ | $12.6 \times 10^{-7}$ | Wb/Am |
| Speed of light (in vacuum) | $c_0$ | 30 | cm/nsec |
| Speed of light (in $SiO_2$) | $c_{ox}$ | 15 | cm/nsec |

**Definitions useful in gate sizing**

| | |
|---|---|
| $g_i$ | Gate logical effort. Ratio of input capacitor to equal on-resistance inverter. |
| $G = \prod_{i=1}^{n} g_i$ | Path logical effort. |
| $H = \frac{C_{out}}{C_{in}}$ | Path electrical effort. |
| $b = \frac{C_{total}}{C_{useful}}$ | Stage branching effort. |
| $B = \prod_{i=1}^{n} b_i$ | path branching effort. |
| $F = GBH$ | path effort. |
| $\hat{f} = g_i h_i = \sqrt[n]{F}$ | Optimal stage effort. |
| $\hat{h_i} = \frac{\hat{f}}{g_i} = \frac{C_{i,out}}{C_{i,in}}$ | Optimal stage electrical effort. |
| $D_i = G_i h_i + p_i$: | Stage delay. |

For sizing inverters, $\forall_{i=1}^{n} b = g = 1$.

# FORMULAS AND EQUATIONS

### Diode

$$I_D = I_S(e^{V_D/\Phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

### MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

### Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

### MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

### Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

### Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$\text{with } g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

### Interconnect

Lumped *RC*: $t_p = 0.69\,RC$

Distributed *RC*: $t_p = 0.38\,RC$

*RC*-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

# CMOS COMBINATIONAL LOGIC

### Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$