EECS 312: Digital Integrated Circuits
Midterm Exam Solutions

12 March 2009

Robert Dick

Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

1. **(5 pts.)** $k_n = \frac{W\mu_n\epsilon_{ox}}{Lt_{ox}}$ When the move from $SiO_2$ to high-$\kappa$ gate dielectric occurred, what qualitative changes were made to the variables upon which $k_n$ depends? Use only a few sentence fragments for your answer.

   $\epsilon_{ox} \uparrow, t_{ox} \uparrow$.

   **Note: If you didn't get this one, please read the Spectrum article. It is a very fun article!**

2. **(10 pts.)** Consider a static CMOS gate implementing the following function:

   $$f(a, b, c) = ab + \bar{b}c$$

   This gate is subjected to the following transition $a = 1, b = 0, c = 1 \rightarrow a = 1, b = 1, c = 1$. Will the gate's dynamic energy consumption be greater if its inputs come from other standard static CMOS gates and inverters, or from DCVSL gates? Use one sentence to explain why. You may also use a schematic if that makes your answer clearer.
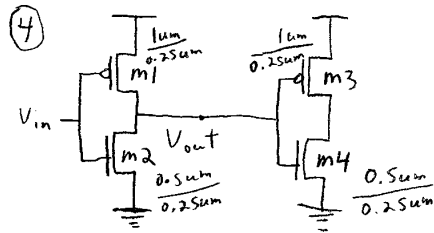
   **Any answer expressing the possible relationship between different transition times for $b$ and $\bar{b}$ when implemented using standard static CMOS gates and inverters, but not for DCVSL, and output glitching for $f$ received credit. With DCVSL, the two will change at approximately the same time. With standard static CMOS gates and inverters, one will switch significantly before the other (plus the delay of an inverter). If $b$ switches before $\bar{b}$, this will cause the output of $f$ to briefly glitch to 0.**

   **Note: Do not be very concerned if you did not have this answer: few did. In retrospect, I believe I wrote this question badly. I will give more details on such potentially-ambiguous questions in future exams.**

3. **(10 pts.)** Given process variation resulting in a Gaussian distribution of threshold voltage around its nominal value, will total integrated circuit sub-threshold leakage power consumption be higher, the same, or lower than that of an integrated circuit in which all transistors have nominal threshold voltages? Use at most two sentences to explain why.

> **Total leakage is likely to be higher. Leakage power is proportional to $e^{\frac{-\Delta V_T}{nkT/q}}$. Thus a given decrease in $V_T$ results in a big increase in leakage power while the same increase in $V_T$ results in a small decrease in leakage power.**

4. **(10 pts.)** Determine the high-to-low propagation delay for an inverter with a $500\,\text{nm}$ wide NMOSFET and a $1\,\mu\text{m}$ wide PMOSFET with its output connected to another identical inverter. Assume the default $250\,\text{nm}$ process. Do consider overlap capacitance. Recall that it is necessary to consider both bottom and sidewall capacitance. You may neglect the resistance and capacitance of the wire connecting the two inverters. Note that the switch model reference table gives values for $W/L =$ transistors. Show your work.

④



Find $t_p HL$ for $V_{out}$

$V_{dd} = 2.5V$

$t_p HL = R_n C_L$

$R_n$ is $R_{eq}$ of m2

For nmos $W = L = 0.25 um$, $R_{eq} = 13 k\Omega$

For $W = 0.5um$, $R_{eq} = 6.5 k\Omega$

$C_L$ is composed of gate-channel and overlap cap for the second inverter (m3 and m4) and drain-junction and gate-drain cap for the second inverter (m1 and m2).

$C_{gcm3} = C_{ox_p} WL = 6 \cdot 1 \cdot 0.25 = 1.5 fF$

$C_{overlap m3} = C_{aso} + C_{abo} = 2 \cdot C_{o_p} W = 2 \cdot 0.27 \cdot 1 = 0.54 fF$

$C_{gcm4} = C_{ox_n} WL = 6 \cdot 0.5 \cdot 0.25 = 0.75 fF$

$C_{overlap m4} = C_{aso} + C_{soo} = 2 \cdot C_{o_n} W = 2 \cdot 0.31 \cdot 0.5 = 0.31 fF$

$C_{gd m1} = C_{o_p} W = 0.27 \cdot 1 = 0.27 fF$

  Miller effect; Convert to cap to ground

$C_{gd_1} = 2 \cdot C_{gd m1}$
$= 0.54 fF$

$C_{gd m2} = C_{o_n} W = 0.31 \cdot 0.5 = 0.155 fF$

  miller Effect

$C_{gd_2} = 2 \cdot C_{gd m2}$
$= 0.31 fF$

$$C_{dm1} = C_{jbot} + C_{sidewall}$$
$$= C_j(W \cdot L_{diff}) + C_{jsw}(2L_{diff} + W)$$

Note that we forgot to specify $L_{diff}$ (length of the drain diffusion regi
If you used 0.25um (channel length) we did not take off points, even
though it is incorrect.
An appropriate value for $L_{diff}$ is $3L_{chan}$ or 0.75um.

$$= 1.9(1 \cdot 0.75) + 0.22(2 \cdot 0.75 + 1)$$
$$= 1.975 \, fF$$

$$C_{dm2} = C_j(W \cdot L_{diff}) + C_{jsw}(2L_{diff} + W)$$
$$= 2 \cdot (0.5 \cdot 0.75) + 0.28(2 \cdot 0.75 + 0.5)$$
$$= 1.31 \, fF$$

$$C_L = C_{gcm3} + C_{gcm4} + C_{overlapm3} + C_{overlapm4} + C_{gd1} + C_{gd2} + C_{dm1} + C_{dm2}$$
$$= 1.5 + 0.75 + 0.54 + 0.31 + 0.54 + 0.31 + 1.975 + 1.31 \, fF$$
$$= 7.235 \, fF$$

$$t_{pHL} = 0.69 \cdot R_n \cdot C_L$$
$$= 0.69 \cdot 6.5 \, k\Omega \cdot 7.235 \, fF$$
$$= 32.5 \, ps$$

Note about drain-junction caps:
In this solution, we use the pessimistic junction cap equation
$$C_j(W \cdot L) + C_{jsw}(2L + W)$$
As the junction diode reverse bias increases, this capacitance
actually decreases. Page 195 in the textbook presents a
linear model for this effect, where the junction cap is
scaled by a $K_{eq}$ value. $K_{eq}$ ranges from ~0.6 to ~0.8.
See example 5.3 for an explanation of how to use this to
more accurately determine $C_L$ for this problem.

5. **(10 pts.)** Assuming the default 250 nm process, determine the minimum and maximum percentage change in subthreshold leakage current of a minimal-width NMOSFET given that the threshold voltage may deviate by 0.1 V from the nominal in either direction. You may assume that $n = 1.5$.

$$\text{Let } \sigma = 1 - e^{-\frac{V_{DS}}{kT/q}} \tag{1}$$

$$I_D^{nominal} = I_S e^{\frac{V_{GS}}{nkT/q}} \sigma \tag{2}$$

$$I_D^{nominal} = I_S e^{\frac{0\,\text{V}}{1.5 \cdot 26\,\text{mV}}} \sigma \qquad \textbf{(from table)} \tag{3}$$

$$I_D^{nominal} = I_S e^{25.6 \cdot 0} \sigma \tag{4}$$

$$I_D^{nominal} = I_S \sigma \tag{5}$$

$$I_D^{low} = I_S e^{25.6 \cdot -0.1} \sigma \tag{6}$$

$$I_D^{low} = I_S e^{-2.56} \sigma \tag{7}$$

$$I_D^{low} = I_S \cdot 0.0773 \cdot \sigma \qquad \textbf{(from plot)} \tag{8}$$

$$I_D^{high} = I_S e^{25.6 \cdot 0.1} \sigma \tag{9}$$

$$I_D^{high} = I_S e^{2.56} \sigma \tag{10}$$

$$I_D^{high} = I_S \cdot 12.9 \cdot \sigma \qquad \textbf{(from plot)} \tag{11}$$

$$\Delta I_D^{low} = \frac{I_D^{low} - I_D^{nominal}}{I_D^{nominal}} \tag{12}$$

$$\Delta I_D^{low} = \frac{I_S \cdot 0.0773 \cdot \sigma - I_S \sigma}{I_S \sigma} \tag{13}$$
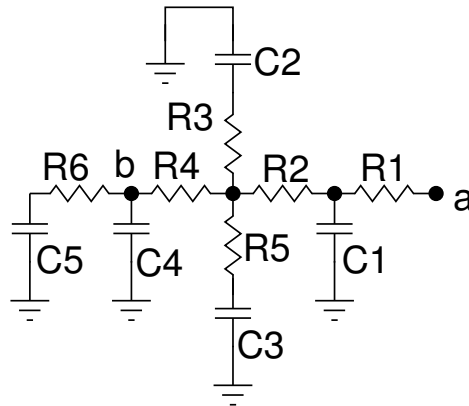
$$\Delta I_D^{low} = 0.0773 - 1 = -0.923 = -92.3\% \tag{14}$$

$$\Delta I_D^{high} = \frac{I_D^{high} - I_D^{nominal}}{I_D^{nominal}} \tag{15}$$

$$\Delta I_D^{high} = \frac{I_S \cdot 12.9 \cdot \sigma - I_S \sigma}{I_S \sigma} \tag{16}$$

$$\Delta I_D^{high} = 12.9 - 1 = 11.9 = 1190\% \tag{17}$$

6. **(10 pts.)** Determine the Elmore delay from Node a to Node b in the following circuit.
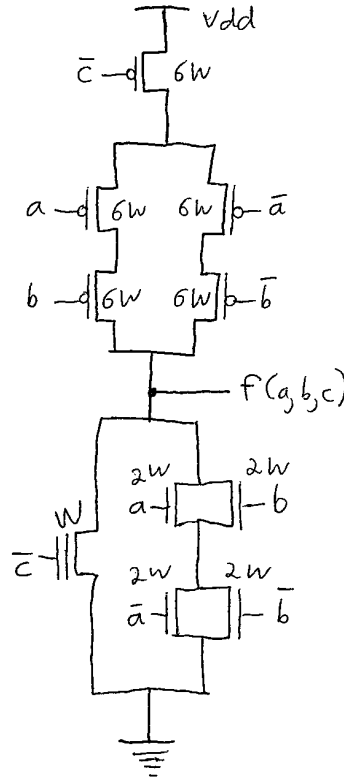


$$\tau_{ab} = R1(C1 + C2 + C3 + C4 + C5) + R2(C2 + C3 + C4 + C5) + R4(C4 + C5) \tag{18}$$

7. **(10 pts.)** Show the circuit diagram for a static CMOS implementation of the following function sized to have the same resistance to ground and $V_{DD}$ as an inverter with a $W$ wide NMOSFET and an $2W$ wide PMOSFET. You may assume access to complemented and uncomplemented input literals, i.e., $a$ and $\bar{a}$.
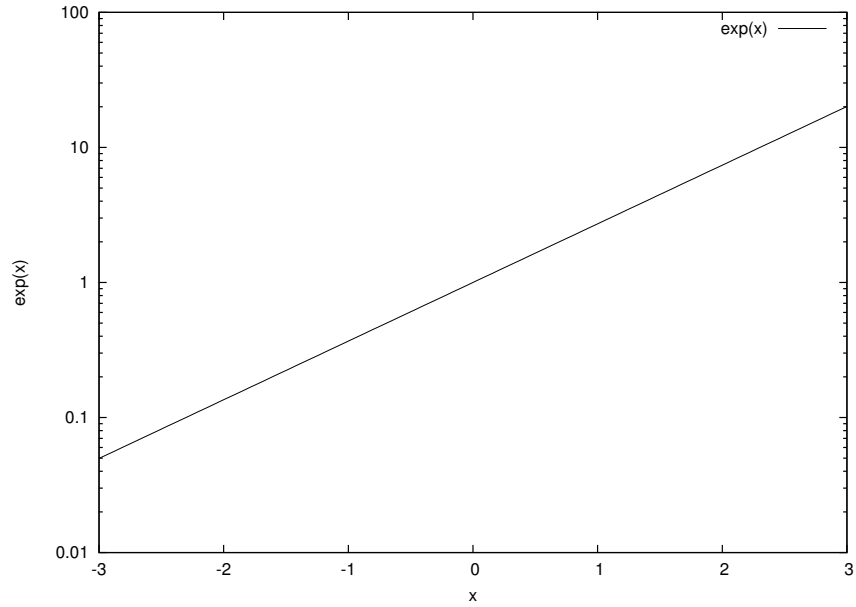
$$f(a, b, c) = (ab + \bar{a}\bar{b})c$$



8. **(0 pts.)** Was this exam □ tricky and surprising or did it □ fairly closely follow the material we focused on in class?

> **Note: Problem 2 was trickier than I intended it to be, and I intend to be clearer in the future. Problem 4 was somewhat tedious, but you shouldn't be surprised to see a tedious problem again in the future.**

| | $C_{OX}$ $(fF/\mu m^2)$ | $C_O$ $(fF/\mu m)$ | $C_j$ $(fF/\mu m^2)$ | $m_j$ | $\phi_b$ $(V)$ | $C_{jsw}$ $(fF/\mu m)$ | $m_{jsw}$ | $\phi_{bsw}$ $(V)$ |
|---|---|---|---|---|---|---|---|---|
| NMOS | 6 | 0.31 | 2 | 0.5 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 6 | 0.27 | 1.9 | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

# MODELS FOR CMOS DEVICES

### CMOS (0.25 μm) – Unified Model.

|  | $V_{T0}$ (V) | $\gamma$ (V$^{0.5}$) | $V_{DSAT}$ (V) | $k'$ (A/V$^2$) | $\lambda$ (V$^{-1}$) |
|---|---|---|---|---|---|
| NMOS | 0.43 | 0.4 | 0.63 | $115 \times 10^{-6}$ | 0.06 |
| PMOS | −0.4 | −0.4 | −1 | $−30 \times 10^{-6}$ | −0.1 |

### CMOS (0.25 μm) – Switch Model ($R_{eq}$)

| $V_{DD}$ (V) | 1 | 1.5 | 2 | 2.5 |
|---|---|---|---|---|
| NMOS (kΩ) | 35 | 19 | 15 | 13 |
| PMOS (kΩ) | 115 | 55 | 38 | 31 |

### CMOS (0.25 μm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

# VALUES OF MATERIAL AND PHYSICAL CONSTANTS

| Name | Symbol | Value | Units |
|---|---|---|---|
| Room temperature | $T$ | 300 ($= 27°C$) | K |
| Boltzman constant | $k$ | $1.38 \times 10^{-23}$ | J/K |
| Electron charge | $q$ | $1.6 \times 10^{-19}$ | C |
| Thermal voltage | $\phi_T = kT/q$ | 26 | mV (at 300 K) |
| Intrinsic Carrier Concentration (Silicon) | $n_i$ | $1.5 \times 10^{10}$ | $cm^{-3}$ (at 300 K) |
| Permittivity of Si | $\epsilon_{si}$ | $1.05 \times 10^{-12}$ | F/cm |
| Permittivity of $SiO_2$ | $\epsilon_{ox}$ | $3.5 \times 10^{-13}$ | F/cm |
| Resistivity of Al | $\rho_{Al}$ | $2.7 \times 10^{-8}$ | $\Omega$-m |
| Resistivity of Cu | $\rho_{Cu}$ | $1.7 \times 10^{-8}$ | $\Omega$-m |
| Magnetic permeability of vacuum (similar for $SiO_2$) | $\mu_0$ | $12.6 \times 10^{-7}$ | Wb/Am |
| Speed of light (in vacuum) | $c_0$ | 30 | cm/nsec |
| Speed of light (in $SiO_2$) | $c_{ox}$ | 15 | cm/nsec |

# FORMULAS AND EQUATIONS

### Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times$$
$$[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

### MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat}C_{ox}W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS})$$
$$\text{(velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

### Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

### MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right)$$

$$\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

### Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69R_{eq}C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

### Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \text{ with } r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \dfrac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

### Interconnect

Lumped $RC$: $t_p = 0.69\,RC$

Distributed $RC$: $t_p = 0.38\,RC$

$RC$-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$


# CMOS COMBINATIONAL LOGIC

### Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^N\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^N p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$