EECS 312: Digital Integrated Circuits
Midterm Exam Solutions

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Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids.

Signature:

1 Qualitative questions

1. **(10 pts.)** Indicate whether each of the following has been increasing (↑) or decreasing (↓) with process scaling for synchronous integrated circuits. If you feel the need to qualify your answer, limit the qualification to three words at most.

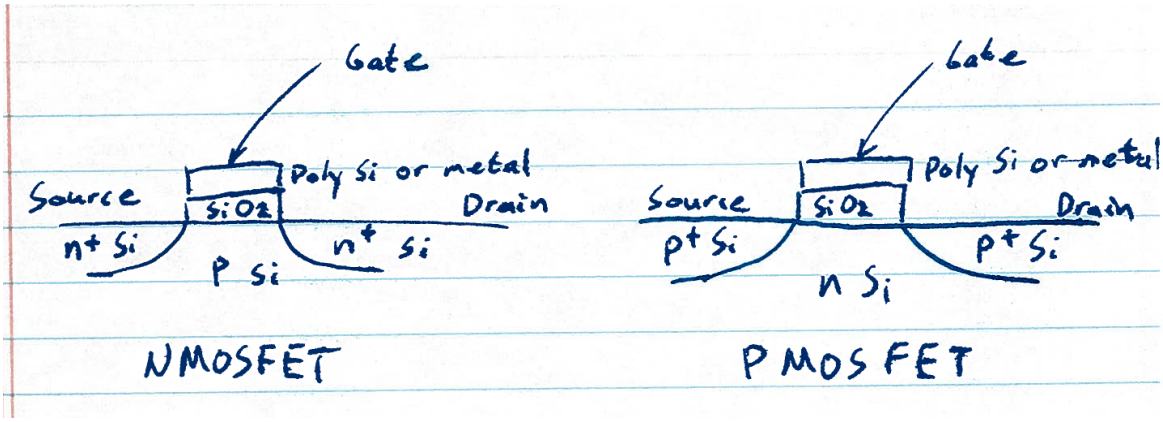
   (a) Clock frequency: ↑

   (b) Power consumption per device per switching event: ↓

   (c) Dynamic power consumption as a proportion of total power consumption: ↓

   (d) t_{ox}: ↓, except high-k dielectric

2. **(10 pts.)** Draw the side view of both an NMOSFET and a PMOSFET, showing the locations for source, drain, and gate, and indicating the type(s) of material used in each portion of the structure. Indicate class and concentration of dopants using the standard notation.



3. **(10 pts.)** Using no more than three sentences, each, explain why

   (a) Threshold voltage decreases for very short NMOSFETs and
   A portion of the region under the gate is already partially depleted by the source and drain fields. For short transistors, this region is no smaller and therefore has more relative effect.

   (b) Threshold voltage increases for narrow NMOSFETs.
   In the middle of the transistor, the field effect is similar to that for infinite parallel plates. Near the edges, the fringing effect results in a higher required voltage difference to achieve inversion. For narrow transistors, the appropriate model moves from infinite parallel plates to a line and plate.

4. **(10 pts.)** Use one sentence, each, to answer the following questions:

   (a) Give one reason why the switch from Al to Cu interconnect required moving to the dual Damascene process.

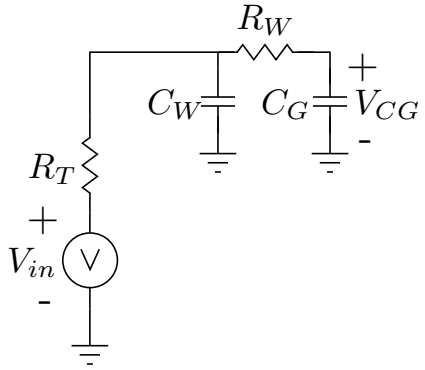
   i. **Etching copper to form easily-removed volatile compounds is harder than similarly etching aluminum.**
   ii. **Copper diffuses into silicon, requiring silicon to be protected by another substance before deposition. Although this is now part of the standard dual Damascene process, and is therefore an acceptable answer, it was not the source of the name of the process.**

   (b) Give one reason for an increase in the complexity of individual design rules with process scaling.
   As feature sizes reduce relative to exposure light wavelength, the radius of interaction increases in terms of lambda, requiring more rules.

   (c) Indicate one important use of CMP during the fabrication process.
   Planarization between fabrication of metal layers.

2 Quantitative questions

5. **(10 pts.)** Consider the circuit shown in the following figure.



Given that V_{in} has been 0 V for a very long time, and changes instantly to 2.5 V at $t = 0$, derive the expression for $V_{CG}(t)$. It is fine to simplify the problem by converting the resistances and capacitances to lump sum values. Please simplify your expression as much as possible. **Gross simplifications were accepted for this question. In fact, any answer providing a complete voltage function with approximately the right form, and constants that don't introduce extreme error, was accepted. However, we will soon learn the concept of Elmore delay, after which time a more refined approximation will be possible, and expected. The following answers were accepted.**

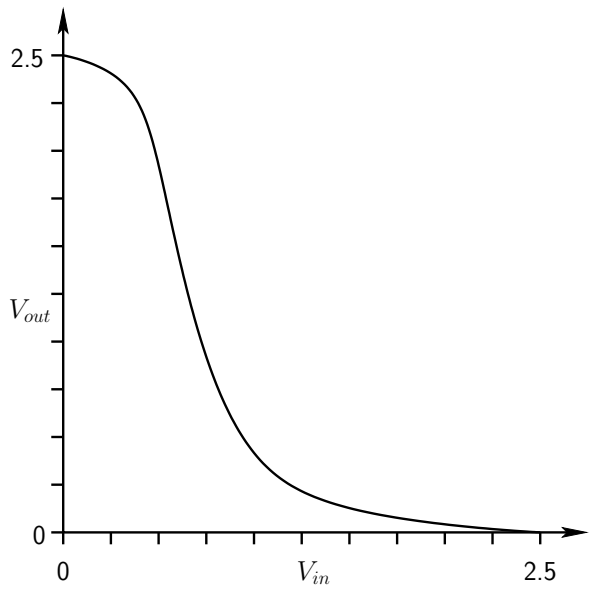
$$V_{CG}(t) \approx 2.5\,\text{V}\left(1 - e^{\frac{-t}{\textbf{anything not crazy}}}\right)$$

The preferred answer is

$$V_{CG}(T) \approx 2.5\,\text{V}\left(1 - e^{\frac{-t}{R_T C_W + (R_T + R_W) C_G}}\right).$$

Again, note that this answer was not required for full credit on this exam.

6. **(10 pts.)** Consider the transfer function shown in the following figure.



Report NM_L and NM_H for this technology. I understand that you are estimating these values from the plot so answers within 5% of the right value will be considered correct.

$$NM_L = 0.375\,\mathrm{V}$$
$$NM_H = 1.375\,\mathrm{V}$$

7. **(20 pts.)** Determine the steady-state current through a floating-output inverter built from minimal-width (i.e., it is an unbalanced inverter) and minimal-length FETs in the default process for each of the following values of V_{GS}: 0 V and 0.2 V. Show your work.

In both cases, NMOSFET is in the sub-threshold region. The PMOSFET resistance is negligible compared to that of the NMOSFET. We can simplify the problem and derive an approximate solution by assuming that the PMOSFET has no resistance and concentrating on the NMOSFET. More precise solutions were also accepted. Those who wrote the correct expression but did not solve for the numerical values of the exponentials were not penalized.

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}} \left(1 - e^{\frac{-V_{DS}}{kT/q}}\right)$$
$$I_D(0\,\mathrm{V}) = 21.0\,\mathrm{pA} e^{\frac{0\,\mathrm{V}}{1.5 \cdot 25.875^{-3}}} \left(1 - e^{\frac{-2.5\,\mathrm{V}}{25.875 \times 10^{-3}}}\right)$$
$$I_D(0\,\mathrm{V}) = 21.0\,\mathrm{pA} \left(1 - e^{\frac{-2.5\,\mathrm{V}}{25.875 \times 10^{-3}}}\right)$$
$$I_D(0\,\mathrm{V}) = 21\,\mathrm{pA}$$
$$I_D(0.2\,\mathrm{V}) = 21.0\,\mathrm{pA} e^{\frac{0.2\,\mathrm{V}}{1.5 \cdot 25.875 \times 10^{-3}}} \left(1 - e^{\frac{-2.5\,\mathrm{V}}{25.875 \times 10^{-3}}}\right)$$
$$I_D(0.2\,\mathrm{V}) = 3.63\,\mathrm{nA}$$

A solution using the subthreshold swing expression is also fine.

3 Reference material

	C_{OX} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MODELS FOR CMOS DEVICES

CMOS (0.25 µm) – Unified Model.

	V_{T0} (V)	γ (V$^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	–0.4	–1	-30×10^{-6}	–0.1

CMOS (0.25 µm) – Switch Model (R_{eq})

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

CMOS (0.25 µm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

Name	Value
kT/q	25.875 mJ/C
NMOSFET I_S	21.0 pA
PMOSFET I_S	41.8 pA
n (for I_D calculation)	1.5

VALUES OF MATERIAL AND PHYSICAL CONSTANTS

Name	Symbol	Value	Units
Room temperature	T	300 (= 27°C)	K
Boltzman constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Thermal voltage	$\phi_T = kT/q$	26	mV (at 300 K)
Intrinsic Carrier Concentration (Silicon)	n_i	1.5×10^{10}	cm^{-3} (at 300 K)
Permittivity of Si	ε_{si}	1.05×10^{-12}	F/cm
Permittivity of SiO_2	ε_{ox}	3.5×10^{-13}	F/cm
Resistivity of Al	ρ_{Al}	2.7×10^{-8}	Ω-m
Resistivity of Cu	ρ_{Cu}	1.7×10^{-8}	Ω-m
Magnetic permeability of vacuum (similar for SiO_2)	μ_0	12.6×10^{-7}	Wb/Am
Speed of light (in vacuum)	c_0	30	cm/nsec
Speed of light (in SiO_2)	c_{ox}	15	cm/nsec

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$I_D = 0$ for $V_{GT} \le 0$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\,RC$

Distributed *RC*: $t_p = 0.38\,RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$