EECS 312: Digital Integrated Circuits
Midterm Exam

26 October 2010

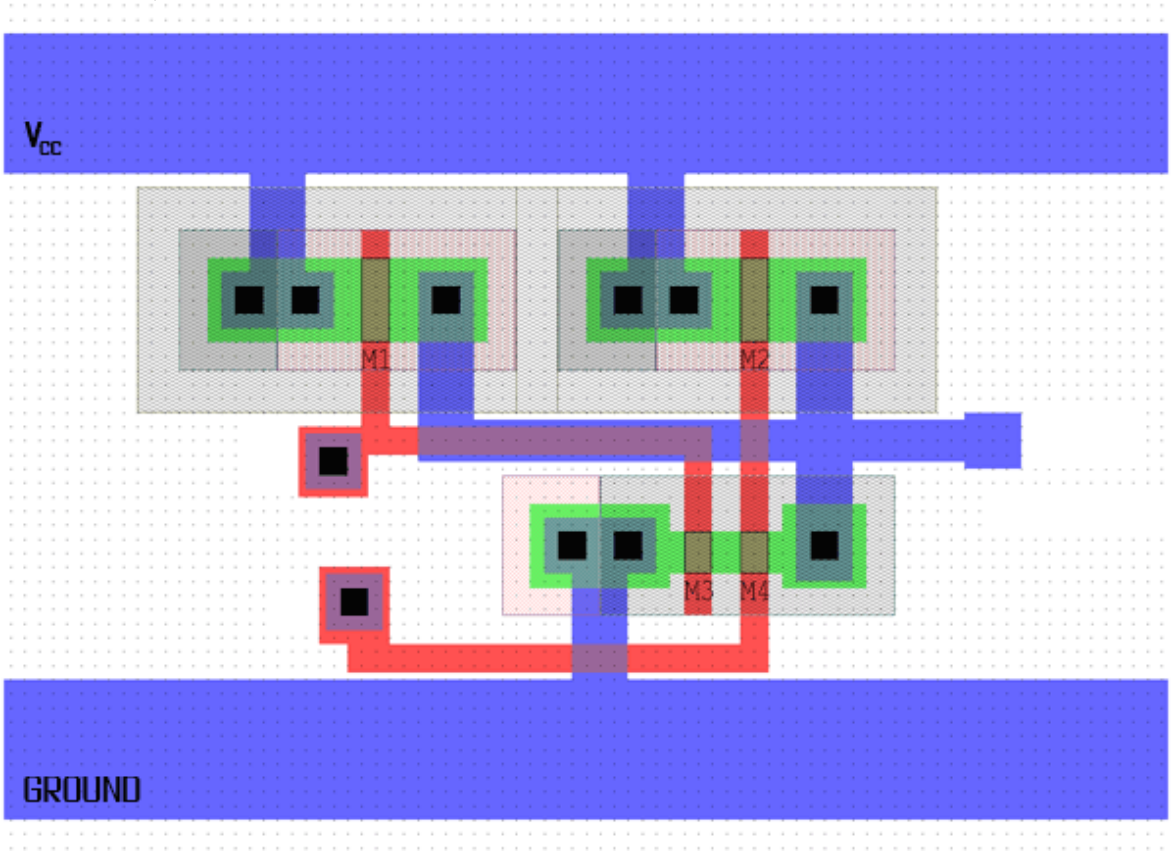
Robert Dick

Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids, e.g., calculators.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

1. **(15 total pts.)** Consider the following figure.



(a) **(5 pts.)** What type of logic gate is this?

NAND2. The pull-up network has two PMOSFETs in parallel and the pull-down network has two NMOSFETs in series. Interestingly, we can see that the designer didn't balance t_{phl} and t_{plh}.

(b) **(10 pts.)** Write an expression for the total gate output node drain capacitance as a function of λ and constants that can be found in Section 1. Note that the transistors are all minimal-length, i.e., $L = 2\lambda$. You needn't do numerical calculation. You just need to write the expression in terms of the relevant variables. Note, V_{CC} is the system's high voltage. To those of you who already know about the Miller effect, you need not consider it in this problem. Unless you are very good at measuring, you had better show your work, e.g., by indicating your length estimates before computing capacitances based on them.

We will need to consider the drain capacitances of two PMOSFETs and one NMOSFET.

$$\begin{aligned} C_{total} =& A_{drain,total,p} \cdot C_{j,p} + A_{drain,total,n} \cdot C_{j,n} + \\ & P_{drain,total,p} \cdot C_{jsw,p} + P_{drain,total,n} \cdot C_{jsw,n} + \\ & W_{total,p} \cdot C_{O,p} + W_{total,n} \cdot C_{O,n} + \\ & A_{gate,p} \cdot \eta_p \cdot C_{ox,p} + A_{gate,n} \cdot \eta_n \cdot C_{ox,n}, \end{aligned}$$

where η_p and η_n are 0 in cutoff or saturation, but $1/2$ in the linear region. Reading the diagram, and keeping in mind that the transistors are all 2λ long, we find that the area and perimeter (sans channel side) for all last-stage MOSFET drains, as well as the gate widths and areas.

$$\begin{aligned} A_{drain,total,p} &= 7 \cdot 6 \cdot 2\,\lambda^2 = 84\,\lambda^2 \\ A_{drain,total,n} &= 6 \cdot 6 + 3 \cdot 1\,\lambda^2 = 39\,\lambda^2 \\ P_{drain,total,p} &= 2(7 \cdot 2 + 6)\,\lambda = 40\,\lambda \\ P_{drain,total,n} &= 6 \cdot 2 + 6 + 1 \cdot 2\,\lambda^2 = 20\,\lambda^2 \\ W_{total,p} &= 6 \cdot 2\,\lambda = 12\,\lambda \\ W_{total,n} &= 3\,\lambda \\ A_{gate,p} &= 12 \cdot 2\,\lambda^2 = 24\,\lambda \\ A_{gate,n} &= 3 \cdot 2\,\lambda^2 = 6\,\lambda^2 \end{aligned}$$

Thus, we have

$$\begin{aligned} C_{total} =& 84\,\lambda^2 \cdot C_{j,p} + 39\,\lambda^2 \cdot C_{j,n} + \\ & 40\,\lambda \cdot C_{jsw,p} + 20\,\lambda \cdot C_{jsw,n} + \\ & 12\,\lambda \cdot C_{O,p} + 3\,\lambda \cdot C_{O,n} + \\ & 24\,\lambda^2 \cdot \eta_p \cdot C_{ox,p} + 6\,\lambda^2 \cdot \eta_n \cdot C_{ox,n}, \end{aligned}$$

where η_p and η_n are 0 in cutoff or saturation, but $1/2$ in the linear region.

2. **(10 total pts.)** Consider the following equation for some sort of power consumption in an integrated circuit:

$$P_? = C \cdot {V_{DD}}^2 \cdot f \cdot A.$$

(a) **(2 pts.)** Use at most two sentences to explain what type of power consumption this equation models.

Power dissipated in resistors (e.g., the channel and interconnect) due to charging and discharging load capacitances (e.g., gate, drain, and interconnect capacitances) in a synchronous system.

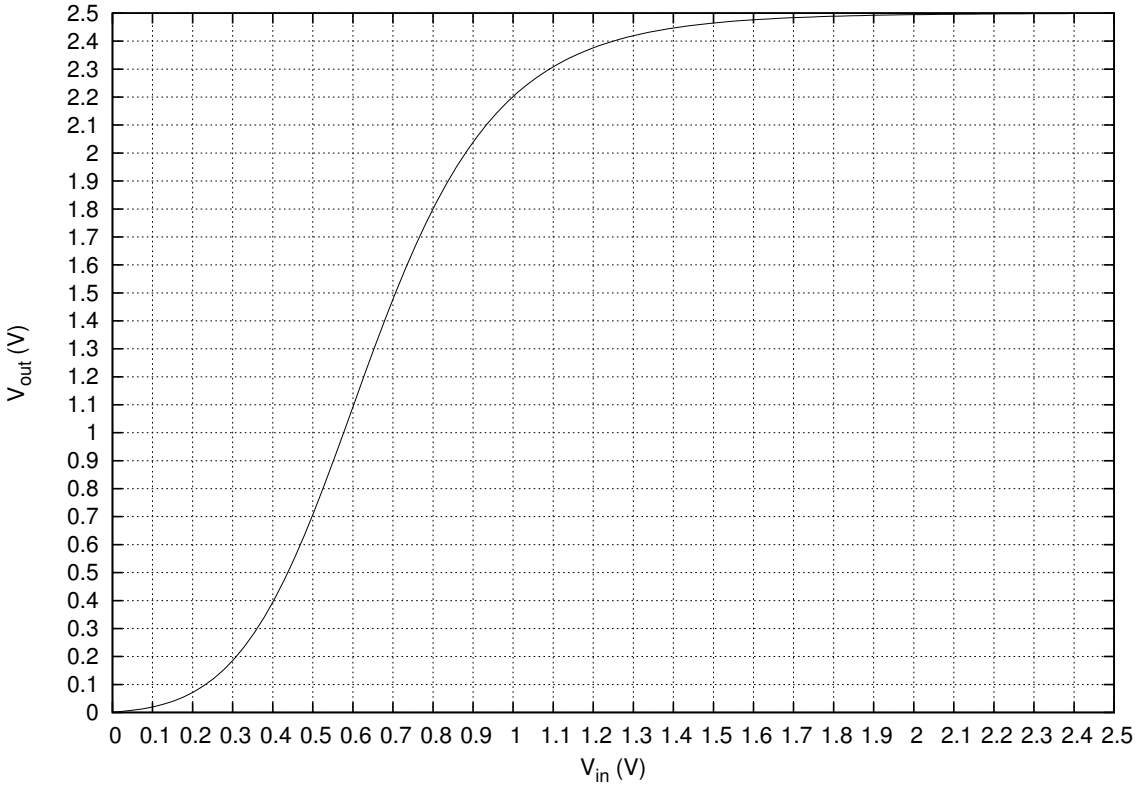
(b) **(4 pts.)** Use at most one sentence to define C in this equation. A single-word definition would be insufficient.

Total circuit capacitive load that may be charged or discharged due to clock transitions.

(c) **(4 pts.)** Use at most two sentences to describe how C might be reduced.

Make the transistors smaller **or** use low-κ dielectric around interconnect.

3. **(10 total pts.)** Consider the following transfer curve.



(a) **(2 pts.)** What type of device is this?

Buffer.

(b) **(4 pts.)** What are its NM_H and NM_L?

$$NM_H \approx 1.5\,\text{V and}$$
$$NM_L \approx 0.25\,\text{V}$$

(c) **(4 pts.)** What is its V_M and g (gain)?

$$
\begin{aligned}
V_M &\approx 0.77\,\mathrm{V} \text{ and} \\
g &\approx \frac{y_2 - y_1}{x_2 - x_1} \\
&\approx \frac{1.5\,\mathrm{V} - 0.4\,\mathrm{V}}{0.7\,\mathrm{V} - 0.4\,\mathrm{V}} \\
&\approx \frac{1.1\,\mathrm{V}}{0.3\,\mathrm{V}} \\
&\approx 3.7
\end{aligned}
$$

4. **(10 pts.)** Use three or fewer sentences to describe the properties of CMOS devices that prevented their earlier widespread use? I.e., why did BJTs long remain dominant for use in digital logic?

   Slow. Poor reliability due to difficult-to-fabricate gate dielectric.

5. **(10 total pts.)** Draw a side view of a PMOSFET.

   (a) **(4 pts.)** Label each region with the type of material used.

   (b) **(3 pts.)** Label the source, drain, gate, and bulk terminals.

   (c) **(3 pts.)** Indicate any diodes in the structure.

   See the lecture notes or book.

6. **(5 pts.)** Use at most one sentence to describe why an extremely low V_{DD} can result in a higher energy consumption for a particular task than a higher, but still sub-threshold, V_{DD}.

   At extremely low V_{DD} values, the delay increases so much that the energy consumption can increase despite reduction in power consumption.

7. **(10 pts.)** If an NMOSFET gate's dielectric were changed from SiO_2 to a low-κ material with half the permittivity of SiO_2, what would happen to its I_D? You may assume that the NMOSFET is not velocity saturated, and that its $V_{GS} \geq V_{TN}$. State any assumptions and provide evidence for your answer, e.g., by writing the applicable expression for I_D.

$$
\begin{aligned}
I_D &= k' \frac{W}{L} \left(V_{GS} - V_T\right) V_{DS} - \frac{V_{DS}^2}{2} \text{ or} \\
I_D &= k' \frac{k'}{2} \frac{W}{L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right)
\end{aligned}
$$

   Assuming that the change does not influence V_T, k' would be halved, resulting in I_D being halved.

8. **(10 total pts.) (7 pts.)** List the following interconnect fabrication steps in chronological order:

- Etch metal.
- Expose photoresist using mask.
- Remove all photoresist.
- Deposit photoresist.
- Deposit metal everywhere.

    - Deposit metal everywhere.
    - Deposit photoresist.
    - Expose photoresist using mask.
    - Etch metal.
    - Remove all photoresist.

(3 pts.) What type of metal is this process appropriate for?

Al.

1 Reference material

	C_{OX} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MODELS FOR CMOS DEVICES

CMOS (0.25 µm) – Unified Model.

	V_{T0} (V)	γ (V$^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	–0.4	–1	-30×10^{-6}	–0.1

CMOS (0.25 µm) – Switch Model (R_{eq})

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

CMOS (0.25 µm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

Name	Value
kT/q	$25.875\,\mathrm{mJ/C}$
NMOSFET I_S	$21.0\,\mathrm{pA}$
PMOSFET I_S	$41.8\,\mathrm{pA}$
n (for I_D calculation)	1.5

VALUES OF MATERIAL AND PHYSICAL CONSTANTS

Name	Symbol	Value	Units
Room temperature	T	300 (= 27°C)	K
Boltzman constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Thermal voltage	$\phi_T = kT/q$	26	mV (at 300 K)
Intrinsic Carrier Concentration (Silicon)	n_i	1.5×10^{10}	cm^{-3} (at 300 K)
Permittivity of Si	ε_{si}	1.05×10^{-12}	F/cm
Permittivity of SiO_2	ε_{ox}	3.5×10^{-13}	F/cm
Resistivity of Al	ρ_{Al}	2.7×10^{-8}	Ω-m
Resistivity of Cu	ρ_{Cu}	1.7×10^{-8}	Ω-m
Magnetic permeability of vacuum (similar for SiO_2)	μ_0	12.6×10^{-7}	Wb/Am
Speed of light (in vacuum)	c_0	30	cm/nsec
Speed of light (in SiO_2)	c_{ox}	15	cm/nsec

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\ RC$

Distributed *RC*: $t_p = 0.38\ RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$