EECS 312: Digital Integrated Circuits
Midterm Exam

8 October 2013

Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids, e.g., calculators. One sheet of notes is permitted.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

1. Circle the features/components that would be unsurprising in an embedded microprocessor designed for use in smartphones, but unexpected in a general-purpose microprocessor.
   (a) Cache.
   (b) Analog wireless communication transceivers.
   (c) Multiple cores.
2. Circle all that apply. Transitioning from large single-core processors to similar-sized multi-core processors has the following benefits:
   (a) Reduced power consumption,
   (b) Improved single-thread performance,
   (c) Reduced software application design complexity, and/or
   (d) Reduced on-chip communication delay for many signals.
3. In a misguided attempt to increase the number of usable gates per unit area of IC, a designer has decided to use CMOS only for inverters, and to build all other (non-inverting) logic gates using pull-up networks composed of NMOSFETs and pull-down networks composed of PMOSFETs.
   (a) How many transistors are required to implement a three-input AND using this design style?
   (b) Does the IC have a good chance of implementing the desired logic functions ("Yes" or "No")? Ignore the impact on performance for this question.
   (c) List two disadvantages of the proposed design style.
4. Use up to two sentences to explain why holes generally travel more slowly than electrons in IC semiconductors.
5. What is the primary advantage of single-electron tunneling transistors over MOSFETs (up to five words)?
6. The PMOSFETs and NMOSFETs in an inverter have been sized to achieve balanced rise and fall times. However, process variation has caused the implementation to deviate from the design. The A line in Figure 1 is associated with an inverter that has
   (a) Lower-than-planned resistance PMOSFET and higher-than-planned resistance NMOSFET.
   (b) Higher-than-planned resistance PMOSFET and lower-than-planned resistance NMOSFET.

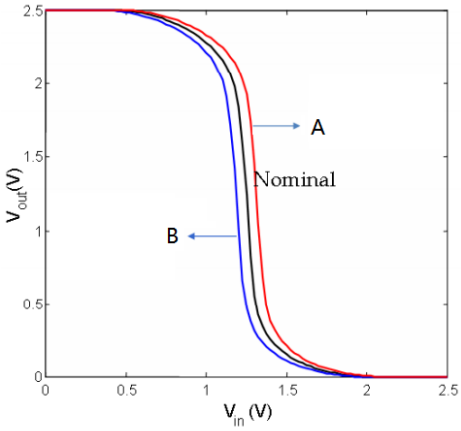

Figure 1: Inverter transfer functions.

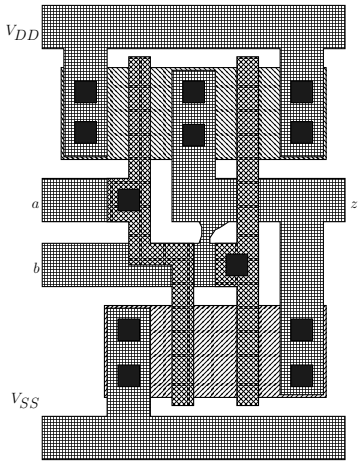

Figure 2: Corrupted layout.

7. A dust particle did something horrible to a mask, causing the implemented layout to differ from the designed layout. Consider the corrupted layout shown in Figure 2.

   (a) What type of gate was the designer most likely trying to implement?

   (b) Draw the gate- or transistor-level schematic for the gate actually implemented.

   (c) Is there any input vector (a, b) for which the output and power consumption will be as the designer originally intended? If so, indicate the input vector.

8. Give the truth table and transistor-level schematic for a three-input OR gate implemented in CMOS.

9. Consider the circuit in Figure 3. In the following circuit the capacitance of C_L is 50 fF. C_L is initially charged to 2.5 V. At time zero, its gate is attached ground, as shown in the figure. V_{TP} = -0.5 V. You may ignore the effects of leakage.

   (a) If we replace the PMOSFET channel with a 2 kΩ resistor, how long does it take for the capacitor to discharge to $V_{DD}/2$?

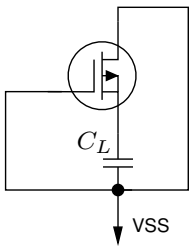

Figure 3: PMOSFET with grounded gate.

(b) If we consider transistor cut-off, what is the final voltage of the capacitor?

10. A synchronous IC has a total capacitance of 200 pF, a V_{DD} 2.5 V, and an average switching activity factor of 0.1, it can run at a clock frequency of 1 GHz. A task requires 1,000 cycles to complete. The total leakage power consumption is 10 µW, and it is almost entirely a result of subthreshold leakage power consumption.

    (a) What is the total energy consumed?

    (b) Consider the impact of reducing V_{DD} to 1.25 V. Assume, for the sake of simplicity, that logic gate delay is inversely proportional to V_{DD} and that subthreshold leakage power consumption is proportional to V_{DD}. Indicate the resulting change in task completion time and total energy consumption

11. Consider an inverter driving a capacitive load, C. The inverter input voltage is initially 2.5 V, and inverter output voltage is static. At time 0 s, the input voltage instantly transitions from 2.5 V to 0 V.

    (a) How much energy is eventually provided by the power supply?

    (b) How much energy is stored in the capacitor?

    (c) Use one sentence to indicate the reason for the difference in these values.

12. Consider two inverters in series. Assume standard process values for anything not given. You are welcome to use the tables at the end of the exam. Assume that capacitances are constant within operating regions, but may vary between operating regions. All gates are 0.25 µm long. All diffusion regions are 0.50 µm long. V_{DD} is 2.5 V. Answers within 10% of the correct values are accurate enough. As a result, you may be able to neglect some complex-to-calculate capacitances. Get a decent solution, first, and come back to this problem to solve more precisely if time permits.

Transistor	Gate width (µm)
First PMOSFET	1.0
First NMOSFET	0.5
Second PMOSFET	40.0
Second NMOSFET	20.0

    The input voltage of the first inverter has been 2.5 V for a very long time. At 0 s, it transitions instantly to 0 V.

    (a) What is the capacitive load seen by the first inverter?

    (b) Determine when the input of the second inverter will reach 0.8 V.

13. Consider the circuit in Figure 4. Write an expression for the voltage at V_x. You may assume that n=1 to simplify calculation. We won't define n here, but when you figure it out, you will know you are on the right track. There is no need to calculate a number; giving an expression is sufficient.

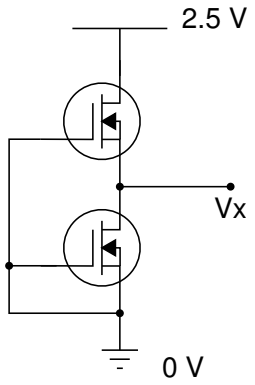

Figure 4: NMOSFETs with grounded gates.

1 Reference material

	C_{OX} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MODELS FOR CMOS DEVICES

CMOS (0.25 µm) – Unified Model.

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	–0.4	–1	-30×10^{-6}	–0.1

CMOS (0.25 µm) – Switch Model (R_{eq})

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

CMOS (0.25 µm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

Name	Value
kT/q	$25.875\,^{\mathrm{mJ}}/_{\mathrm{C}}$
NMOSFET I_S	21.0 pA
PMOSFET I_S	41.8 pA
n (for I_D calculation)	1.5

VALUES OF MATERIAL AND PHYSICAL CONSTANTS

Name	Symbol	Value	Units
Room temperature	T	300 (= 27°C)	K
Boltzman constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Thermal voltage	$\phi_T = kT/q$	26	mV (at 300 K)
Intrinsic Carrier Concentration (Silicon)	n_i	1.5×10^{10}	cm^{-3} (at 300 K)
Permittivity of Si	ε_{si}	1.05×10^{-12}	F/cm
Permittivity of SiO_2	ε_{ox}	3.5×10^{-13}	F/cm
Resistivity of Al	ρ_{Al}	2.7×10^{-8}	Ω-m
Resistivity of Cu	ρ_{Cu}	1.7×10^{-8}	Ω-m
Magnetic permeability of vacuum (similar for SiO_2)	μ_0	12.6×10^{-7}	Wb/Am
Speed of light (in vacuum)	c_0	30	cm/nsec
Speed of light (in SiO_2)	c_{ox}	15	cm/nsec

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot {V_{DD}}^2 \cdot f \cdot A$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance
f : switching frequency
b : MOS transistor gain
t : rise/fall time of inputs

V_{DD} : high voltage
A : switching activity
V_T : threshold voltage

$\dagger\ P_{SHORT}$ usually $\leq 10\%$ of P_{SWITCH}

Smaller as $V_{DD} \to V_T$

$A < 0.5$ for combinational nodes, 1 for clocked nodes.

FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\,RC$

Distributed *RC*: $t_p = 0.38\,RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$