EECS 312: Digital Integrated Circuits
Midterm Exam

2 December 2010

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Show your work. Derivations are required for credit; end results are insufficient.
Closed book. No electronic mental aids, e.g., calculators.

Honor Pledge: I have neither given nor received aid in this exam.

Signature:

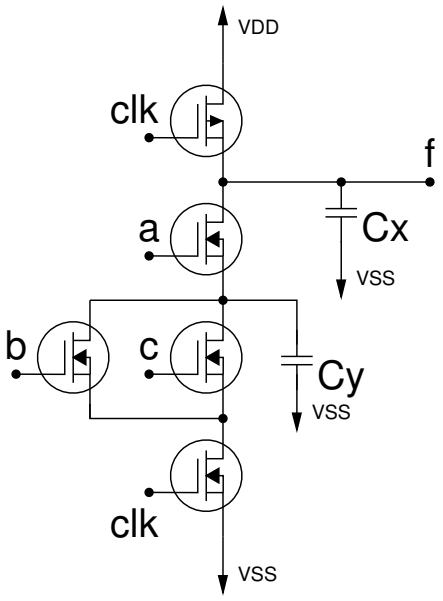


Figure 1: Example circuit.

1. **(20 pts.)** Consider the circuit in Figure 1. Hint: The top transistor is a PMOSFET and the rest are NMOSFETs.

   (a) **(1 pts.)** What style of logic is this implemented in?

   "Dynamic CMOS" or "Dynamic".

   (b) **(1 pts.)** Is this an example of ratioed logic?

   No. Comment: Ratioed logic is a class of static logic for which steady-state correctness depends on transistor sizing. One example is pseudo-NMOS.

   (c) **(5 pts.)** What function is implemented?

$f(a, b, c) = \overline{a} + \overline{b}\,\overline{c}$

(d) **(8 pts.)** If $C_x = 5C_Y$, then what is the lowest voltage node f may reach during the evaluate stage if a transitions from 0 V to 2.5 V but b and c remain at 0 V. Show your work. State and support your assumptions.

Assume transistor a stays on.

$$C_x = \frac{\Delta q}{\Delta V_x}, \tag{1}$$

$$C_y = \frac{\Delta q}{\Delta V_y}, \text{ and} \tag{2}$$

$$C_x = 5C_y. \tag{3}$$

Thus,

$$\frac{\Delta V_y}{\Delta V_x} = 5 \tag{4}$$

We also know that

$$2.5\,\text{V} - \Delta V_x = 0\,\text{V} + \Delta V_y \text{ so} \tag{5}$$

$$\frac{2.5\,\text{V} - \Delta V_x}{\Delta V_x} = 5 \tag{6}$$

$$\Delta V_x = \frac{2.5\,\text{V}}{6} = 0.42\,\text{V}. \tag{7}$$

V_x and V_y may both reach 2.08 V. That is high enough to turn off transistor a because $2.5\,\text{V} - 0.43\,\text{V} = 2.07\,\text{V}$. However, 2.08 V does provide a fairly tight lower bound on V_x. The error is less than 0.002 V. It was also fine to compute the exact V_x when transistor a turns off.

(e) **(5 pts.)** If clk, a, b, and c are all 0 V, V_{C_Y} is 0.25 V, and Figure 2 gives the I_D–V_{GS} curve for each NMOSFET, find an upper bound on the leakage current for the logic gate. Hint: It is fine to extrapolate.

Current for transistor a is approximately 10^{-12} A. That provides a upper bound on the current for the entire gate. Comment: It was also fine to attempt to consider the impacts of the other series transistors on leakage.

2. **(10 pts.)** Consider a load with resistance R and capacitance C that is driven by a time-varying voltage source.

(a) **(5 pts.)** Derive an expression for the total energy consumed in the resistor if the voltage source changes instantly from 0 V to 2.5 V at time zero.

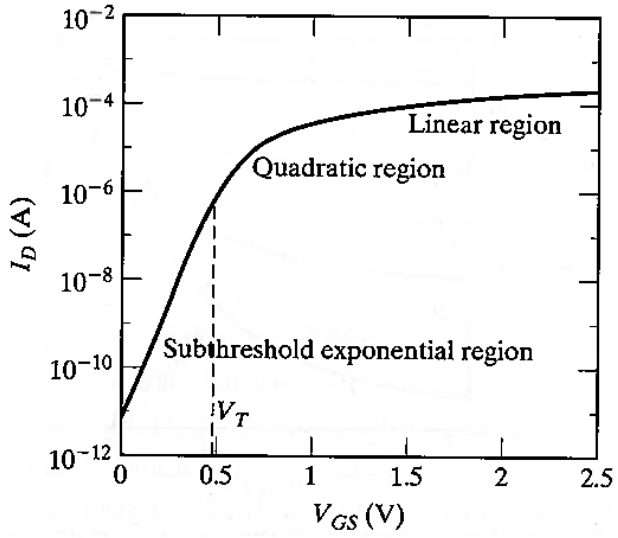


Figure 2: NMOSFET I_D–V_{GS} curve.

$$
\begin{aligned}
E_R^{step} &= \int_{t=0}^{\infty} V_R(t)\, I_R(t)\, dt \\
E_R^{step} &= \int_{t=0}^{\infty} V_R(t)\, \frac{V_R(t)}{R} dt \\
E_R^{step} &= \int_{t=0}^{\infty} V_{DD} e^{-t/RC}\, \frac{V_{DD} e^{-t/RC}}{R} dt \\
E_R^{step} &= \frac{{V_{DD}}^2}{R} \int_{t=0}^{\infty} e^{-2t/R} dt \\
E_R^{step} &= \frac{{V_{DD}}^2}{R} \left(-\frac{RC}{2}\right) \left(e^{-2t/RC}\right)_{t=0}^{\infty} \\
E_R^{step} &= \frac{-{V_{DD}}^2 C}{2} (0-1) \\
E_R^{step} &= \frac{{V_{DD}}^2 C}{2}
\end{aligned}
$$

(b) **(5 pts.)** If the input voltage changes from 0 V to 2.5 V gradually instead of instantly, what is the effect on the total energy consumed in the resistor? Explain your answer. A correct but unsupported answer is not sufficient.

It is reduced because V_R must be less than in the prior case and any increase in time will be compensated for by a quadratic improvement in power consumption.

3. **(10 pts.)** Consider the circuit in Figure 3. V_s changes from 0 V to 2.5 V at time zero.

(a) **(5 pts.)** Derive an expression for the time constant when driving node d.

$\tau_d = r2\,(c1 + c3 + c4 + c5 + c6) + (r2 + r3)\,c7.$

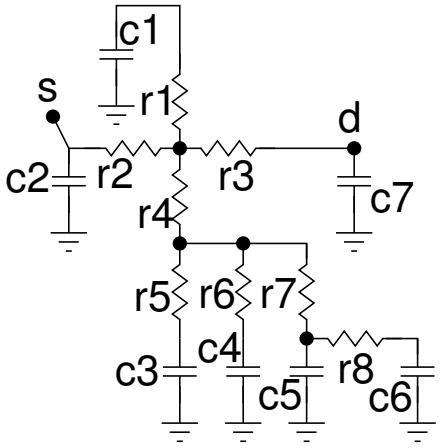


Figure 3: RC network.

(b) **(5 pts.)** Derive an expression for the time at which V_d will reach 2 V. Hint: If you think you need a calculator, check the references at the end of the exam for a good alternative.

$$2.0\,\mathrm{V} = 2.5\,\mathrm{V}\left(1 - e^{\frac{-t}{\tau}}\right) \tag{8}$$

$$\frac{4}{5} = 1 - e^{\frac{-t}{\tau}} \tag{9}$$

$$\frac{1}{5} = e^{\frac{-t}{\tau}} \tag{10}$$

$$\ln\left(\frac{1}{5}\right) = \frac{-t}{\tau} \tag{11}$$

$$t = -\tau \ln\left(\frac{1}{5}\right) \tag{12}$$

$$t = 1.6\tau \tag{13}$$

4. **(10 pts.)** Consider the layout in Figure 4.

(a) **(2 pts.)** What type of logic function does this layout implement?

A messed up inverter.

(b) **(8 pts.)** Point out the three largest problems with this layout. For each explain the impact on gate behavior. When possible, indicate the ways in which important parameters are influenced, e.g., k'.

i. The bottom half of the NMOSFET gate is missing.

ii. The PMOSFET drain is bigger than it needs to be, increasing capacitance without benefit.

iii. The NMOSFET and PMOSFET active regions are the same width, which would result in asymmetric pull-up and pull-down resistances if the gates were designed correctly.

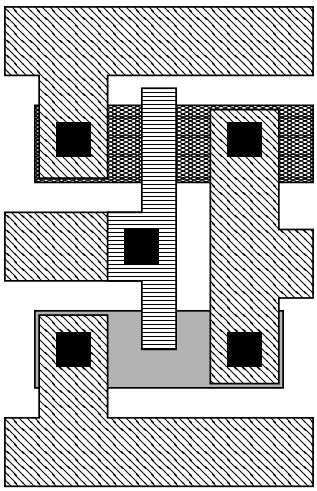


Figure 4: Messed up layout.

5. **(5 pts.)** Using three or fewer sentences, explain one difference in the requirements for 6T cell SRAM sense amplifiers and 1T cell DRAM sense amplifiers.

   1T DRAM has destructive reads, so re-writing sense amplifiers are useful for it. This isn't required for 6T SRAM.

6. **(5 pts.)** Using three or fewer sentences, explain what silicides are and why they are useful.

   In the context of digital integrated circuits, silicides are compounds of silicon and metal. They are useful because they have significantly lower resistances than silicon, even heavily-doped silicon.

7. **(5 pts.)** Draw both a high-level symbol and transistor-level schematic for a falling-edge triggered flip-flop with two inputs, a and b. The output of the flip-flop should toggle if a is 2.5 V or b is equal to the current output of the flip-flop but should otherwise remain unchanged. If gate sizing is important, specify it. You may use hierarchy, i.e., once you show the structure of an inverter once and give a symbol for it, you may use the symbol from then on.

a	b	f^+
0	0	1
0	1	0
1	0	$\overline{f}$
1	1	$\overline{f}$

   The symbol's clock input should have a bubble and triangle. $f^+ = a\overline{f} + \overline{a}\,\overline{b} = \overline{\overline{a\overline{f}}\;\overline{\overline{a}\,\overline{b}}}$, e.g., three two-input NANDs. The rest of this is a D flip-flop. See lecture notes or textbook for schematics of these gates. If it still isn't clear, email me and I will scan and post valid design.

8. **(5 pts.)** Using three or fewer sentences, give an example of a situation in which it is important to consider interconnect parasitic inductance and explain a problem caused by this parasitic inductance.

   Off-chip interconnect is used to supply power to an integrated circuit with rapidly varying power consumption. During rapid current increase, the voltage across the parasitic inductor increases, decreasing the voltage across the integrated circuit. This is called $L\frac{dI}{dt}$ drop.

1 Reference material

	C_{OX} (fF/µm^2)	C_O (fF/µm)	C_j (fF/µm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/µm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

MODELS FOR CMOS DEVICES

CMOS (0.25 µm) – Unified Model.

	V_{T0} (V)	γ (V$^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	–0.4	–0.4	–1	-30×10^{-6}	–0.1

CMOS (0.25 µm) – Switch Model (R_{eq})

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

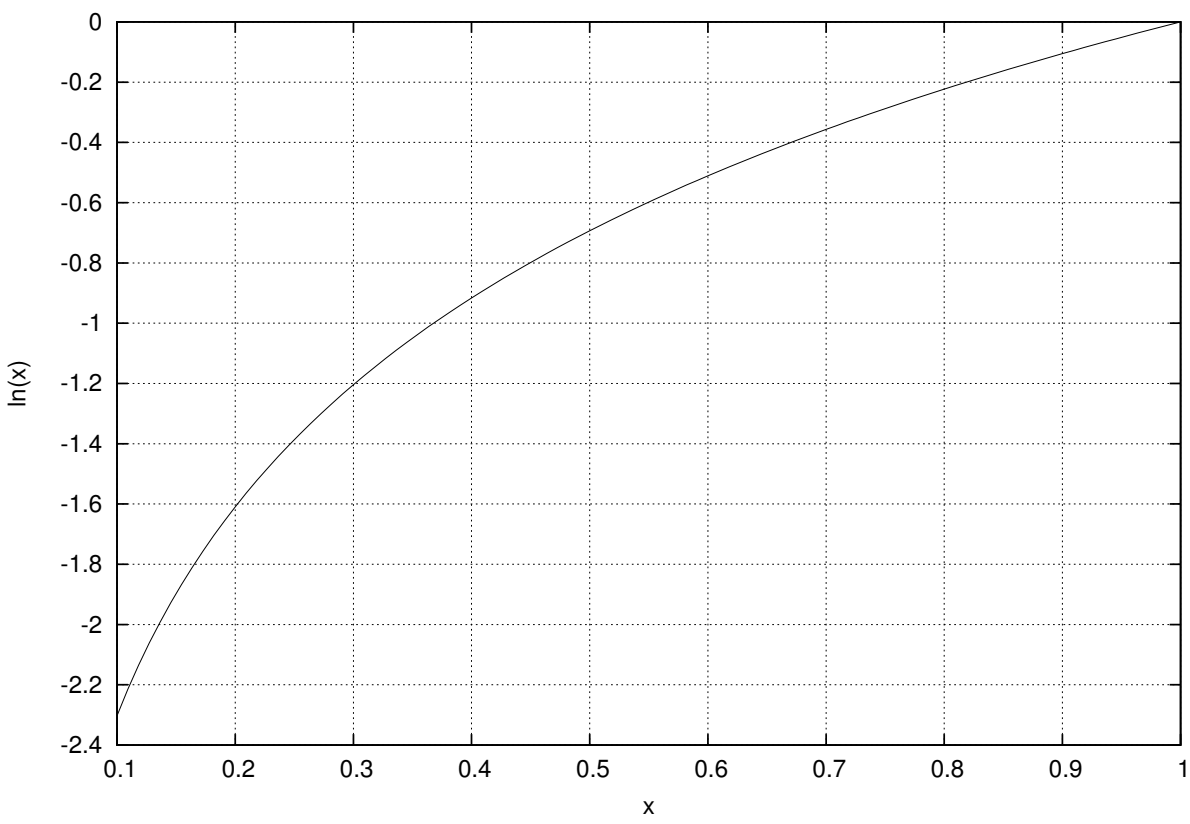
CMOS (0.25 µm) – BSIM Model

See Website: *http://bwrc.eecs.berkeley.edu/IcBook*

Name	Value
kT/q	25.875 mJ/C
NMOSFET I_S	21.0 pA
PMOSFET I_S	41.8 pA
n (for I_D calculation)	1.5

VALUES OF MATERIAL AND PHYSICAL CONSTANTS

Name	Symbol	Value	Units
Room temperature	T	300 (= 27°C)	K
Boltzman constant	k	1.38×10^{-23}	J/K
Electron charge	q	1.6×10^{-19}	C
Thermal voltage	$\phi_T = kT/q$	26	mV (at 300 K)
Intrinsic Carrier Concentration (Silicon)	n_i	1.5×10^{10}	cm^{-3} (at 300 K)
Permittivity of Si	ε_{si}	1.05×10^{-12}	F/cm
Permittivity of SiO_2	ε_{ox}	3.5×10^{-13}	F/cm
Resistivity of Al	ρ_{Al}	2.7×10^{-8}	Ω-m
Resistivity of Cu	ρ_{Cu}	1.7×10^{-8}	Ω-m
Magnetic permeability of vacuum (similar for SiO_2)	μ_0	12.6×10^{-7}	Wb/Am
Speed of light (in vacuum)	c_0	30	cm/nsec
Speed of light (in SiO_2)	c_{ox}	15	cm/nsec



FORMULAS AND EQUATIONS

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \text{ (sat)}$$

$$I_D = \upsilon_{sat} C_{ox} W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \text{ (velocity sat)}$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right) \text{ (triode)}$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \text{ (subthreshold)}$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L(V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{rV_{DD}}{1+r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped *RC*: $t_p = 0.69\ RC$

Distributed *RC*: $t_p = 0.38\ RC$

RC-chain:

$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

CMOS COMBINATIONAL LOGIC

Transistor Sizing using Logical Effort

$$F = \frac{C_L}{C_{g1}} = \prod_1^N \frac{f_i}{b_i} \qquad G = \prod_1^N g_i \qquad D = t_{p0}\sum_{j=1}^{N}\left(p_j + \frac{f_j g_j}{\gamma}\right)$$

$$B = \prod_1^N b_i \qquad H = FGB \qquad D_{min} = t_{p0}\left(\sum_{j=1}^{N} p_j + \frac{N(\sqrt[N]{H})}{\gamma}\right)$$