Midterm exam practice problems

EECS 312: Digital Integrated Circuits

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Initially, I had planned on making a review assignment for the final exam. However, after a student asked for review questions for the second midterm exam I put together some questions to help.

1. Inverter chain sizing for driving large loads.

   Pick Cload and Cinitial values and determine the optimal-delay number of inverters and the input capacitance of each.

2. Types of power consumption, dependence on V, f, and C.

   Write the equation for dynamic power consumption and the equation for static power consumption. Explain the circuit characteristics (e.g., Vt, temperature, or gate size) that each depends on. Point out recent trends for these characteristics.

3. Energy consumption implications of fixed-voltage and fixed-current charging.

   Derive the conditions under which fixed-current charging is more energy-efficient than voltage step function charging.

4. Appropriate interconnect models for different types of interconnect.

   Indicate the conditions under which each of the following models must be considered: ideal, C, RC, and RLC.

5. Reasons for interconnect parasitic capacitances.

   Physically, what is the cause of interconnect parasitic capacitance? How can it be reduced?

6. Trends in integrated circuit interconnect structure.

   What has been happening to interconnect aspect ratio? Number of metal layers?

7. Rent's rule. Know what it is.

   State Rent's rule.

8. Sheet resistance concept.

   Define sheet resistance.

9. Impact of material resistivities. Al and Cu in particular.

   What impact did the move from Al to Cu have on circuit performance?

10. Silicides. Know what they are and why they are used.

    What are silicides? How are they made? Why are they used?

11. Elmore delay modeling. Understand it and be able to use it proficiently.

    Do closed-form analysis on a distributed RC model for a wire. Also, draw an RC tree and solve for the Elmore delay at a few different leaf nodes in the tree. Review the homework and lab assignments on this.

12. Know what happens to the shape of a voltage step function as it propagates along a wire, i.e., a distributed RC network.

    Review the lecture slides on this and the expression for the impact on propagation delay.

13. Transistor sizing. Know how to balance worst-case pull-up and pull-down resistances for complex logic gates. Don't forget impact of mobility.

    Size transistors in an implementation of $f(a,b,c,d) = ab'cd' + a'c' + dab$ to achieve the same worst-case pull-up and pull-down resistances as a minimum-width balanced inverter. Explain the impact of capacitance on delay, and why considering only resistances is insufficient for perfectly balancing t_{plh} and t_{phl}.

14. TG-based design and pass transistor based design using 2^{n-1} MUX as a starting point.

    Implement $f(a,b,c,d) = ab'cd' + a'c' + dab$ using TGs and again with pass transistors.

15. Miller effect. What is it? How can it be modeled?

    Given a physical inverter structure, determine the appropriate gate capacitance to ground, taking into consideration the Miller effect.

16. Stack effect. What is it? What impact does it have on leakage current?

    Explain why putting two off transistors in series results in a different current than would be implied by putting two resistors in series. Explain how to calculate the current.

17. Hazards. What are they? What problems can they cause? What is their fundamental cause? How can they be eliminated?

18. DCVSL design.

    Implement $f(a,b,c,d) = ab'cd' + a'c' + dab$ using DCVSL. State the main advantages of DCVSL.

19. Dynamic logic design.

    Implement $f(a,b,c,d) = ab'cd' + a'c' + dab$ using dynamic logic. State the main advantages of dynamic logic.

20. Charge sharing. How to calculate its impact? How to compensate for it?

21. Leakage in dynamic logic. Use of keepers.

22. Role of combinational and sequential logic.

    Explain the roles of each, and the two ways for sequential logic to maintain state.

23. Latches and flip-flops. Meaning of symbols and behavior. Setup and hold time.

    Describe the operation of D, T, and RS latches and flip-flops. Indicate meanings of clock triangle and bubble symbols. Define setup and hold time.

24. Analysis of simple circuits with feedback, for which the RS latch provided an example.

    Describe the operation of a circuit with the same structure as an RS latch, but in which one two-input NAND and one two-input NOR is used.

25. Bistability.

    Explain why an inverter feedback pair is bistable.

26. Schmitt triggers.

    Design a Schmitt trigger. Explain a possible use.