Homework One

EECS 312: Digital Integrated Circuits
History, context, and diodes

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Due: 24 September

You may discuss the assignment with your classmates. However, you need to understand and write the solutions independently. Please stop by in office hours, ask questions in class, and use the discussion list for clarification and help. Don't be shy about asking for more information or help.

1. Diodes: For this problem, you may use an intrinsic carrier concentration $n_i = 1.5 \times 10^{10}$ 1/cm³ at 300 K and $n_i = 0.7381$ 1/cm³ at 150 K, an electrical permittivity of silicon $\epsilon_{si} = 10^{-12}$ F/cm, and a diode cross sectional area $A_D = 0.5\,\mu\text{m}^2$.

   (a) **(5 pts.)** Compute the built-in potentials of a diode at 150 K and 300 K with

   $$N_A = 10^{18} \text{ atoms/cm}^3 \text{ and}$$
   $$N_D = 10^{18} \text{ atoms/cm}^3.$$

   (b) **(5 pts.)** Compute the built-in potentials of a diode at 150 K and 300 K with

   $$N_A = 10^{16} \text{ atoms/cm}^3 \text{ and}$$
   $$N_D = 10^{20} \text{ atoms/cm}^3.$$

   (c) **(5 pts.)** Compute the depletion-region widths at zero bias using the same diodes at 300 K.

   (d) **(5 pts.)** Compute the n-side/p-side depletion-region width ratios for the same diodes.

   (e) **(5 pts.)** Using at most four sentences, discuss relations between the depletion-region widths and carrier concentrations.

   (f) **(5 pts.)** For the second diode at 300 K, compare the junction capacitances when $V_D = 0$ V, $V_D = 1/2$ V, and $V_D = -2.0$ V. Assume the junction is abrupt.

2. **(10 pts.)** Plot the number of additions per second the most advanced computing technology (other than human and animal brains) could carry out as a function of year, starting from the year 1800 and ending in 2013. Use points to indicate technology milestones, and approximate the trend using a manually fitted line or curve. Having enough (four or five) points to indicate the trend is sufficient for full credit. We will be generous with credit, provided you make a solid effort to make realistic estimates. Labeling your points with the corresponding technologies will make this easier.

3. **(5 pts.)** Estimate the trend in number of additions per second in the coming ten years. Justify your estimate. Use three or fewer sentences.

4. **(10 pts.)** Consider the approximations on slide 19 of the second lecture note packet. Back up your answers via reference to the equations in the lecture notes or textbook. Simplification: Logic gate delay can be roughly approximated as inversely proportional to V_{DD} if $V_{DD} \gg V_T$, and you can assume that $V_{DD} \gg V_T$ for this problem.

   (a) If you halve V_{DD}, what change in operating frequency is required?

(b) Write an expression for energy as a function of power consumption and time.

(c) Operating at this new V_{DD} and f, what is the approximate change in total dynamic energy consumption required to run a particular program to completion? Keep in mind that the number of cycles required to finish the program does not change.

5. **(5 pts.)** If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, what should the ratio of NMOSFET to PMOSFET transistor widths be? Simplifications: Assume, when answering this question, that the fabrication process under consideration allows lines of arbitrary width. When solving this problem, ignore the effect that changing width has on MOSFET capacitance. We will revisit this problem later in the course when we have learned more about MOSFET structure and capacitance.

6. **(5 pts.)** In the context of digital integrated circuits, what are holes? Use three or fewer sentences.

7. **(5 pts.)** Use up to three sentences to define "microprocessor cache".

8. **(10 pts.)** Give two reasons for the recent increase in popularity of multi-core processors.

9. **(5 pts.)** List three advantages of CMOS over NMOS, and one advantage of NMOS over CMOS.

10. PMOS inverter: Assume you have a fabrication technology that can only be used to produce PMOS-FETs, resistors, and wires.

    (a) **(5 pts.)** Draw a schematic for an inverter implemented using this technology. Label the resistor as having resistance R and the PMOSFET as having resistance R_{FET} (when on). When off, the PMOSFET can be assumed to have infinite resistance.

    (b) **(5 pts.)** Write the expression for the output voltage of the inverter when the input is $0\,\text{V}$ as a function of R and R_{FET}.

    (c) **(5 pts.)** Write the expression for the output voltage of the inverter when the input is V_{DD} as a function of R and R_{FET}.

11. Charge carriers:

    (a) **(5 pts.)** When a mobile intrinsic charge carrier is promoted to the conduction band due to thermal energy, is a mobile charge carrier also created in the valence band? Explain why in three or fewer sentences.

    (b) **(5 pts.)** When a mobile intrinsic charge carrier is promoted to the conduction band from a donor ion, is a mobile charge carrier also created in the valence band? Explain why in three or fewer sentences.

12. **(5 pts.)** If electrical fields did not cause charge carriers to drift (i.e., considering only diffusion), what would the steady-state difference in charge between the N and P regions of a diode be, assuming that C_A acceptor ions and C_D donor ions were implanted?