EECS312 HW1 solution

1. (a) 1.09V 0.94V

   (b) 1.09V 0.94V

   (c) 3.43 e-5 cm 4.85 e-6 cm

   (d) 1 1 e-4

   (e) The depletion region width is inversely proportional to carrier concentration.

   (f) 1.46 e-16 F 2.13 e-16 F 0.83 e-16 F

2.

3.

4. (a) frequency should halve

   (b) E = P*t

   (c) 1/4

5. Since the mobility of electron is normally twice of the mobility of holes, we need to make the width of PMOS twice as large as the width of NMOS.

6. Majority carrier in the PMOS carries positive charge.

7. It's on chip memory which can be accessed quickly by CPU.

8. Can do multiple program in parallel.

   Consume less power

9. adv. of CMOS :

   Less power consumption

   High noise immunity

   Faster

   Adv. of NMOS

   Smaller gate

10. (a)

    (b) Vout = (Rfet / (R+Rfet)) * Vdd

    (c) 0

11. (a) a hole is left in the valance band, and it’s carrier.

    (b) No carrier in the valance band

12. Carriers will evenly distribute