Homework Three

EECS 312: Digital Integrated Circuits

Teacher: Robert Dick
Assigned 22 October
Due 29 October

You may discuss the assignment with your classmates. However, you need to understand and write the solutions independently.

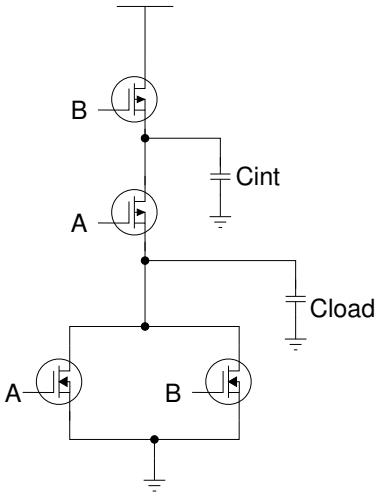


Figure 1: Logic gate.

1. **(10 pts.)** Delay depends on the input patterns. Consider Figure 1. To assist those unfamiliar with these MOSFET symbols, we note that those in the pull-up network are PMOSFETs and those in the pull-down network are NMOSFETs. In input pattern P, inputs A and B are each low for a long time, then input B transitions instantly to V_{DD}. In input pattern Q, inputs A and B are each low for a long time, then both transition to V_{DD} simultaneously and instantly. Which input pattern results in more delay? Explain why.

2. **(10 pts.)** Consider the logic gate shown in Figure 2. What should the ratio of PMOSFET width to NMOSFET width be to achieve balanced rise and fall times? What's capacitances to nodes A and B have? You may assume that the layout around nodes A and B are optimized, i.e., vias and interconnects are only used when actually required.

3. **(10 pts.)** Consider a technology with a linear V–V transfer curve of slope -1 with V_{IH} and V_{IL} (arbitrarily) defined to be $2V_{DD}/3$ and $V_{DD}/3$. If noise may result in a voltage variation of 10% per logic stage (relative to $V_{DD} - V_{SS}$), how long may an inverter chain be while still providing a valid output to the following stage? The input to the first stage is 0 V (V_{SS}).

4. **(10 pts.)** Assuming a three-segment piecewise-linear transfer function, what must the slope of the middle segment be greater than to allow an arbitrary-length inverter chain to operate correctly. For continuous functions, V_{IH} and V_{IL} are defined as the V_I values at which $|dV_O/V_I| = 1$. For the model in this problem, these points will be at the discontinuities.

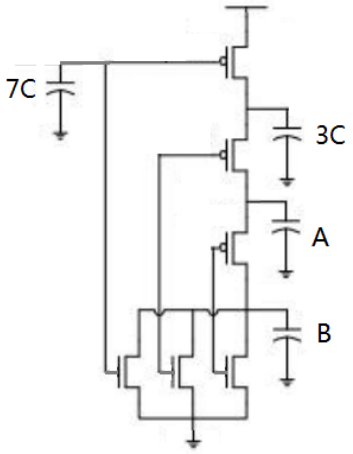


Figure 2: Another logic gate.

5. **(5 pts.)** Using only a few words, indicate the primary advantages and disadvantages of multi-chip modules relative to both single-chip ICs and printed circuit boards.

6. **(10 pts.)** A 4λ wide inverter with input capacitance C_m must drive a load of $83.7C_m$. The output signal may not be inverted. Determine the optimal number of inverters and their optimal sizes, which must be integer multiples of λ. γ=1.1. You may assume it to be zero if you can provide evidence that this introduces little error. Do the analytical portions of this problem manually. You may use a calculator or computer to help evaluating options when discretizing widths.

7. **(5 pts.)** Given that an output from a minimum-width inverter must drive a load with the same capacitance as the inverter, how many and what widths of inverters should be inserted between the two to minimize delay? Use at most three sentences to explain why.

8. **(10 pts.)** Use at most one sentence each to describe the following terms and indicate whether each is significant in high-performance synchronous integrated circuits fabricated using modern, e.g., 45 nm, fabrication processes. If significant, give the approximate percentage (within 10–15%).

   (a) dynamic power consumption,

   (b) short-circuit power consumption,

   (c) drain junction leakage power consumption,

   (d) gate leakage power consumption, and

   (e) subthreshold leakage power consumption.

9. **(10 pts.)** Show the circuit diagram for

$$f(a, b, c) = ab + \overline{a}\,\overline{b}\,\overline{c} \tag{1}$$

   implemented with

   (a) **(5 pts.)** Transmission gates (with output buffer or inverter) and

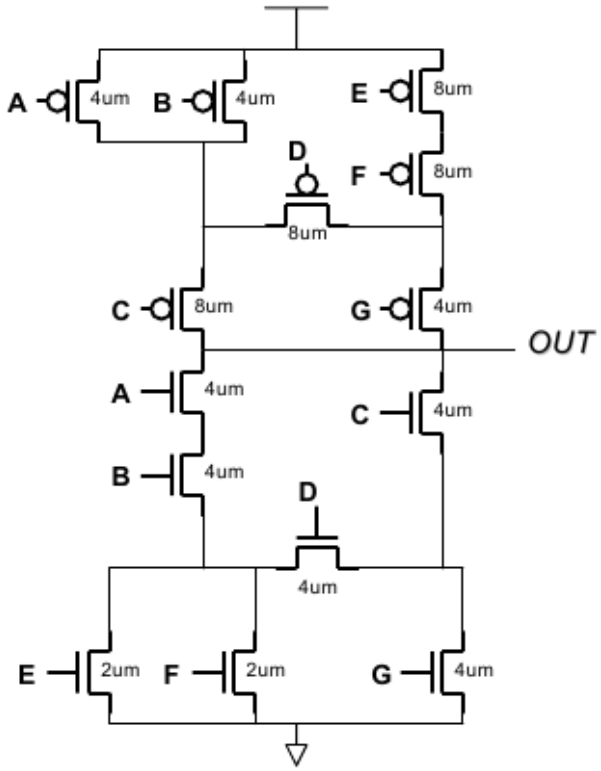
   (b) **(5 pts.)** Pass transistors (with output buffer or inverter).

Do not assume access to complemented input literals.

10. **(10 pts.)** Use default parameters unless alternate values are given.

    (a) **(3 pts.)** Write a logic equation for this complex gate.

    (b) **(7 pts.)** Determine the worst case t_{phl} and t_{plh} transitions in the complex gate given in figure below Indicate an initial and final input pattern in each case. Complex calculations are not required.



11. **(10 pts.)** Derive the propagation delay of an aluminum wire that is 2 cm long and 500 nm wide. Does using a lumped model introduce significant error? You may assume a sheet resistance of $0.075\,\Omega/\square$. Derive the propagation delay of a copper wire with the same shape. State, and verify, any assumptions.

12. **(10 pts.)** Indicate the Elmore delay time constant for node 2 of Figure 4-12 on page 153 of the textbook, in response to a change in voltage at node i. Neglect the voltage source on node s. We are using the same circuit structure, but a different voltage source and terminal node than the example problem in the book.