EECS 312: Digital Integrated Circuits
Lab Project 2 – Extracting Electrical and Physical Parameters from MOSFETs

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1 Introduction

In this lab project, we will apply stimuli to an NMOSFET and a PMOSFET in order to build models of these devices. Although we could be doing this with actual discrete MOSFETs, voltage sources, and oscilloscopes (and there are some advantages to doing it that way), the time cost for learning to work with the equipment would be higher and that approach would be difficult to scale. For example, the simulation software we will use makes it easy to determine what is happening deep inside a circuit composed of many transistors. We need to learn more about the Cadence tools for our later circuit design lab projects anyway, and we can use those tools to very closely approximate what would happen with real MOSFETs in much less time. This is the advantage of simulation: it allows us to try out many ideas quickly. The disadvantage is that the behavior of real devices is seldom perfectly modeled. Fortunately, the NMOSFET and PMOSFET models in the simulator capture everything important. Enough background – onward.

Before you begin, you should create a new library, e.g., proj2, to hold all schematics for this lab. See the first lab assignment for help. If you run into trouble, please contact us.

Table 1: Known transistor parameters

Parameter	NMOS	PMOS
V_{DSAT} (V)	0.63	-1.0
Substrate Doping ($^1/_{cm^3}$)	$N_A = 2.35\times10^{17}$	$N_D = 4.16\times10^{17}$
L_{eff} (µm)	0.20	0.20

Before we begin, please see Table 1 for a few known properties of the transistors you will be characterizing.

2 NMOSFET and PMOSFET Characterization

Use the Cadence tools to enter a characterization circuit similar to Figure 1. This is essentially the same as wiring a discrete device up to test equipment. It will allow you to control the gate voltage, source–drain voltage, and body bias of an NMOSFET. Use the "nmos4" and "pmos4" devices in this lab project. These are the four-terminal (SGDB) versions of the devices.

Make sure your circuit has passed Check and Save. Now, you will analyze this circuit by performing a DC analysis to obtain the desired I-V curves for this device.

1. Open the Analog Design Environment (ADE) and choose DC as your analysis type. Under DC Sweep Analysis, hit Select Source and click the voltage source V_{DS} on the schematic. Enter from 0 to 2.5 by 0.1 and click OK.
2. Click on Variables → Copy From Cellview. Double click on the variables under the "Design Variables" box in the main ADE window. Change the values to 2.5 for both V_{GS} and V_{DS} in the "Value(exp)" box of the window that pops up. Set value of V_{BS} to 0 V.
3. To get the I_{DS} vs. V_{DS} curve, click on Outputs → To be Plotted → Select on Schematic and select the Drain Terminal of the NMOS on the schematic. NOTE: You need to select the square red terminal on the NMOS to get the current at that node. If you select a wire, it will give you the voltage at that node.

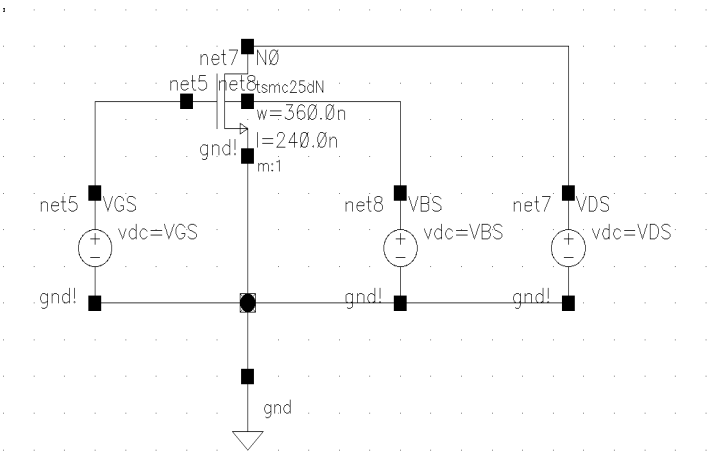

Figure 1: NMOSFET characterization circuit.

4. The selected terminal name will appear in the ADE under Outputs. Double-click on the terminal name and check the "Saved" box and hit OK.
5. Perform a parametric analysis on V_{GS} From 0 V to 2.5 V in Linear Step size of 0.5 V.
6. The plot should automatically pop up. Save the plot as a .png file by clicking on Save as Image.
7. You will need to add cursors showing the data values so you can record these to determine device parameters. Make sure the value of the cursor location on the x-axis (V_{DS}) is visible so you can record this value. You can add a marker to all the plot lines at one by clicking on Trace → Vert, dragging the cursor to the desired x-position, and the pressing m. To view the values of all markers, click on Marker → Show Table.
8. Be sure to label all plots in your report.
9. Use a few cursors on the plot of the NMOSFET response to determine the values of V_{T0n}, k_n', and λ_n. Report these values. Sanity check these values against those for the default process in the textbook. They needn't be identical but possible reasons for large differences should be explained. Explain anything unusual but if you have nothing to say, don't force it. Include any work done during the analysis process including long-hand math and analysis tool scripts.
10. Explain how you can you tell from the plot whether this is a velocity saturated device.
11. Design a circuit to analyze a PMOSFET with the same width and length as the NMOSFET. Hand in this plot, as well as all the other deliverables required for the NMOSFET.

3 Body Bias

Redo the work and prepare the deliverables described in Section 2, but using a V_{BS} of -1 V for the NMOSFET and 1 V for the PMOSFET. Use the unbiased and biased data to calculate the body effect coefficient γ and $2\phi_f$ for the NMOSFET and PMOSFET.

4 Test for Short Channel Effects

For the NMOSFET, set V_{DS} to 2.5 V, without body bias. Choose the DC analysis type and do a DC sweep analysis for a V_{GS} ranging from 0 V to 2.5 V in steps of 0.1 V. in Variables → Copy From Cellview, indicate a default V_{GS} of 2.5 V. Plot

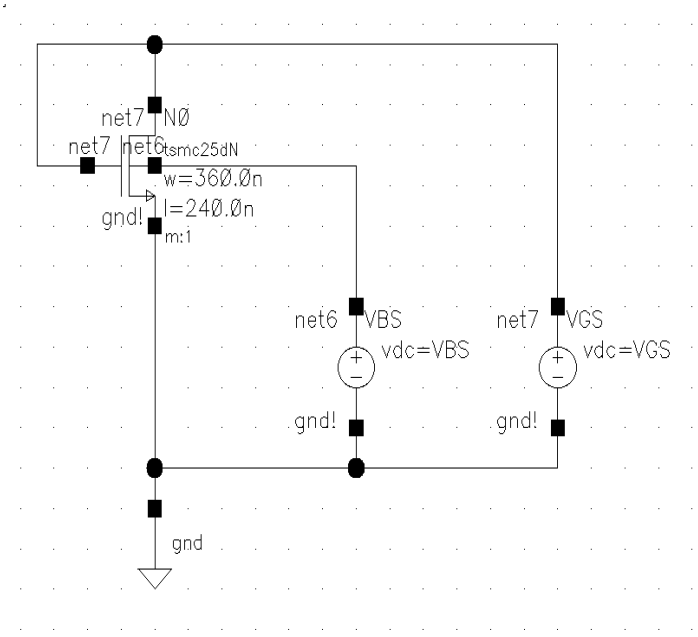

Figure 2: Circuit to keep NMOSFET in saturation.

the drain current as a function of V_{GS}. Hand in this labeled plot. Use your plot to determine whether the NMOSFET is subject to short-channel effects and explain how you were able to draw your conclusion. Repeat a similar analysis for the PMOSFET.

5 Alternative Method to Determine V_T and k

We will now use a different technique to measure the threshold voltage and gain factor (k) directly from the MOS I_D-V_{GS} relationship. We will start by revisiting the equation for drain current for a MOS device operating in the saturation region. Consider the following equation:

$$I_D = \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 . \tag{1}$$

There is a quadratic relationship between the voltage applied on the gate and the resulting drain current (in the saturated region). To extract values like k and V_T from this equation, it would be nice to work with a more linear relationship. Re-write the equation for drain current while in saturation to solve for $\sqrt{k}\left(V_{GS} - V_T\right)$. Please note that k should be substituted for k'_n for the NMOSFET and k'_p PMOSFET. $k = k'^{W}/_{L}$.

A circuit to keep the device in saturation is given in Figure 2. In this circuits, drain and gate are shorted forcing $V_{DS} = V_{GS}$ and therefore $V_{DS} > V_{GS} - V_{T0}$ for all V_{GS}, keeping it in saturation but ideally not velocity saturation. Both k and V_{T0} can be directly measured by plotting vs. V_{GS} to find the slope and x-intercept of the resulting line with no body bias applied. Now carry out the following simulation steps.

1. If you are still in simulation mode from previous simulations, exit and close all open schematics.
2. Open the NMOS schematic and for V_{BS}, enter the the DC Voltage as V_{BS} and for V_{GS}, enter the DC voltage as V_{GS}. Open the ADE.
3. Choose DC as your analysis type. Under DC Sweep Analysis , hit Select Source and click the voltage source V_{GS} on the schematic. Enter From 0 V to 2.5 V by 0.1 V and click OK.
4. Click on Variables → Copy From Cellview and enter the default value of 2.5 V for V_{GS} and 0 V for V_{BS}.

5. To get the I_{DS} vs. V_{GS} curve, click on Outputs → To be Plotted → Select on Schematic and select the Drain Terminal of the NMOS on the schematic. You need to select the square red terminal on the NMOS to get the current at that node. If you select a wire, it will give you the voltage at that node.

6. The selected terminal name will appear in the ADE under Outputs. Double-click on the terminal name and check the "Saved" box and hit OK.

7. Now perform a parametric analysis on V_{BS} From -2 V to 0 V in Linear Step size of 0.5 V

8. A plot of I_{DS} vs. V_{GS} should open for different values of V_{BS}. However, we need to plot the square root of twice the drain current, so we will use the Waveform Calculator to do this for us. First single left click one of the plot lines to select it. Then, in the waveform viewer, click on Tools → Calculator. A box that resembles a calculator should appear on the screen.

9. You will see a number of mathematical functions in the calculator. Select "sqrt()" and then inside the parenthesis, type "2* 'plotline name' ".

10. In the Calculator, change Append to New Win and then click on the Eval button. A waveform showing the square root of $2I_{DS}$ should open in a new window for the value of V_{BS} specified in the equation.

11. Now change New Win back to Append in the calculator and change the value of V_{BS} in the equation and hit Eval. Do this for all 5 different values of V_{BS}.

12. Add at least two cursors (since you will need to calculate slope) at different points of the region that has a linear relationship between $\sqrt{2I_{DS}}$ and V_{GS}.

13. Print this plot, and save it.

14. Design a corresponding circuit for analyzing a PMOSFET and repeat the above steps for this circuit.

15. For the PMOS circuit, enter "-2*" for Step 9 since I_{DS} is negative.

16. Calculate and report k_n, k_p, V_{T0n}, V_{T0p}, γ_n, γ_p, $2\phi_{fn}$, and $2\phi_{fp}$ using the plots. Please indicate which values you are using from the graph to calculate these parameters. How do these values differ from those in Section 2? Provide all plots.

In the process of computing these parameters, you will find that some are highly sensitive to the points used to compute the slope. For example, V_{T0n} may vary from 0 V to 0.7 V: a large error. This is not surprising if one attempts to fit a line to a curve with only two points. Instead, please do the following. Take five points along the most linear portion of the curve and use linear regression software to fit a line to them with minimal error. Many software packages will do this, e.g., MATLAB. You may also use an on-line fitting tool, e.g., that offered at http://wessa.net//slr.wasp.

6 Report preparation and submission

You may submit a PDF file via CTools or hand a hardcopy in during class.

The report should contain the following items.

1. PNG[1] files of Section2 Step6 (Both NMOS and PMOS).

2. Calculation values and explanation of Section2 Step9 (Both NMOS and PMOS).

3. Explanation of Section2 Step10 (Both NMOS and PMOS).

4. PNG files of Section3 (Both NMOS and PMOS).

[1] You don't really need to use PNG, but you should not do lossy compression of your line art, e.g., JPEG.

5. Calculation values of Section3 (Both NMOS and PMOS).
6. PNG files of Section4 (Both NMOS and PMOS).
7. Calculation values of Section4 (Both NMOS and PMOS).
8. PNG files of Section5 Step13 (Both NMOS and PMOS).
9. Calculation values and explanations of Item 16 in Section 5 (Both NMOS and PMOS).