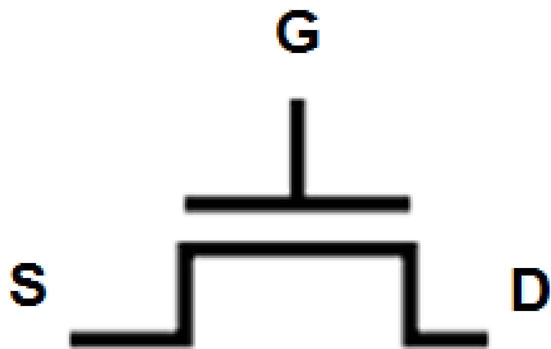
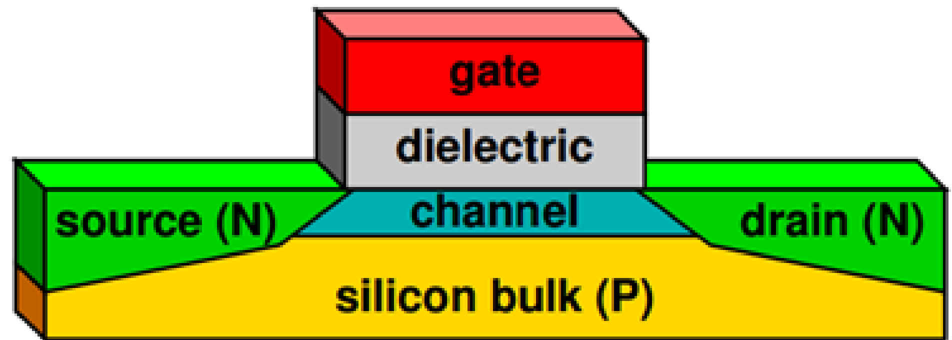
EECS 312 Discussion 12
Review 1

11/22

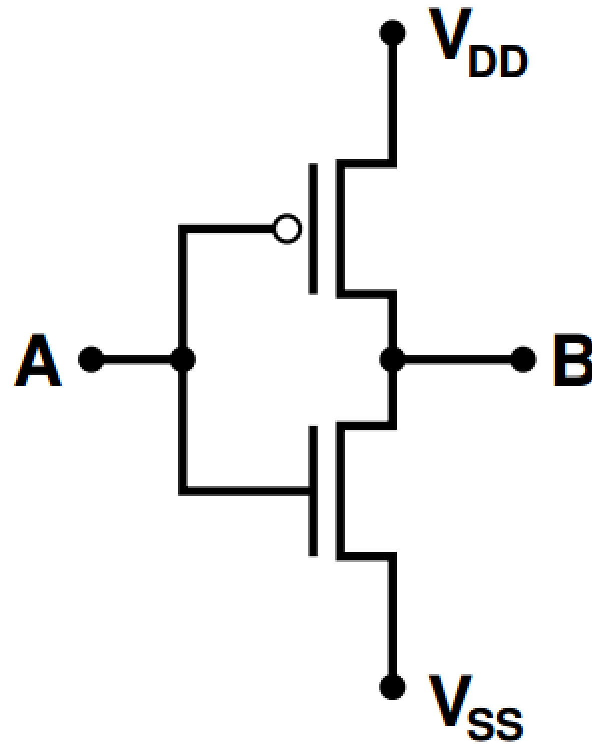
Shengshuo Lu
(luss@umich.edu)

NMOS





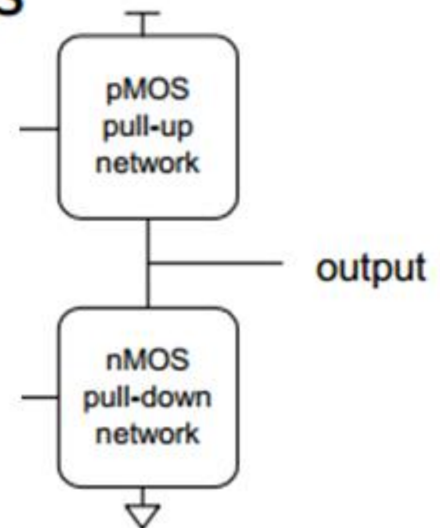
Logic Gates



Inverter

Complementary CMOS

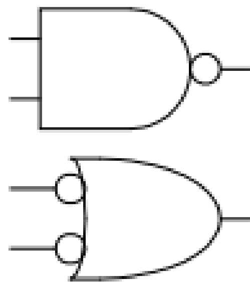
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - Also called static CMOS

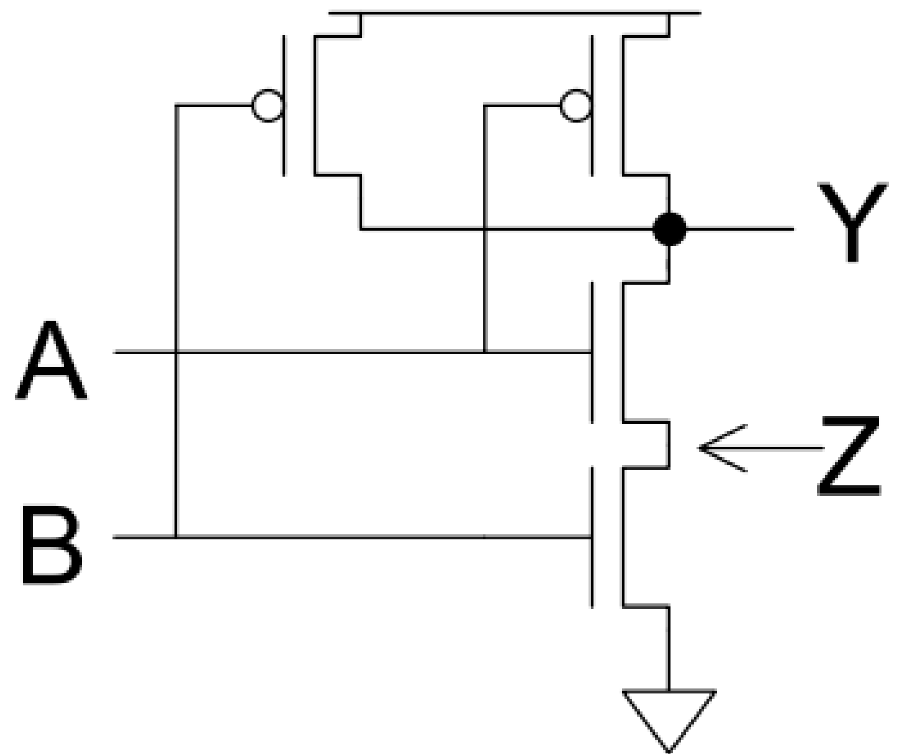


	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

CMOS NAND Gate

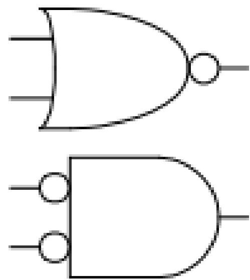
A	B	Y	Z
0	0	1	~100mV
0	1	1	0
1	0	1	VDD-Vth
1	1	0	0

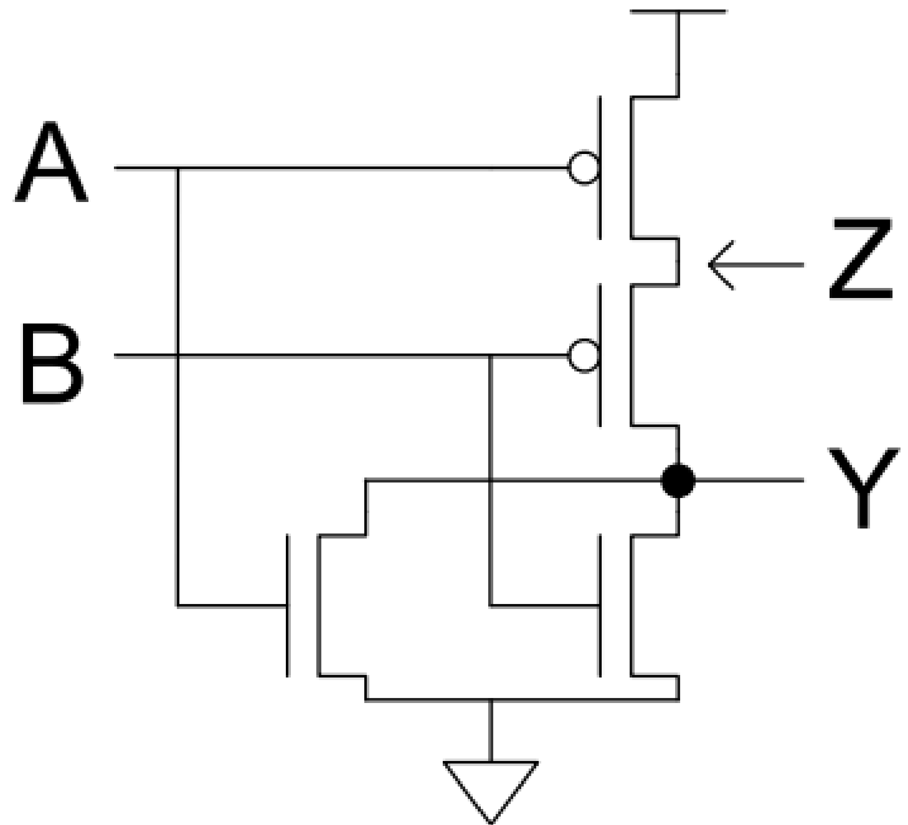




CMOS NOR Gate

A	B	Y	Z
0	0	1	1
0	1	0	1
1	0	0	Vth
1	1	0	~VDD-100mV

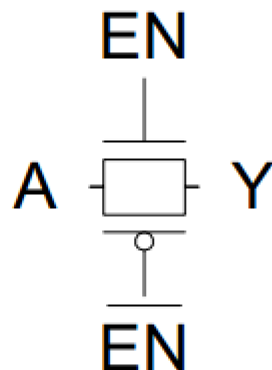


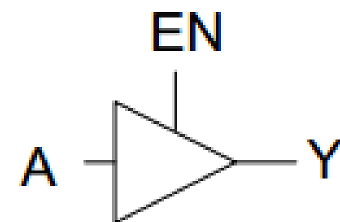


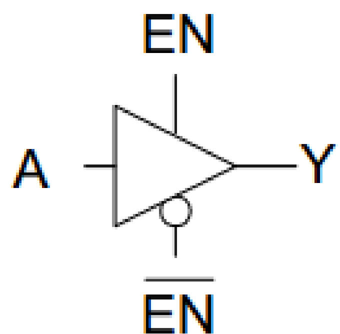
Tristates

- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

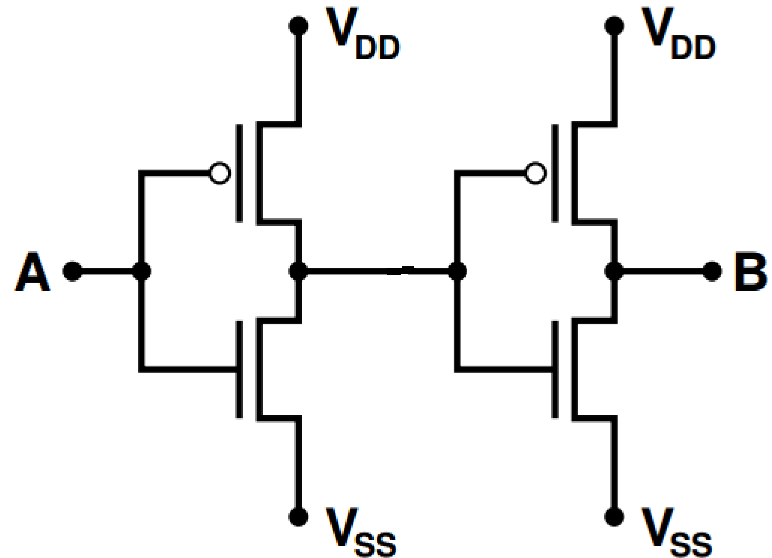






Power

- Dynamic Power
- Static Power
- Short-Circuit Power *



Power

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot V_{DD}^{2} \cdot f \cdot A$$

$$\frac{1}{2} f C V_{dd}^{2}$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance

V_{DD} : high voltage

f : switching frequency

A : switching activity

b : MOS transistor gain

V_T : threshold voltage

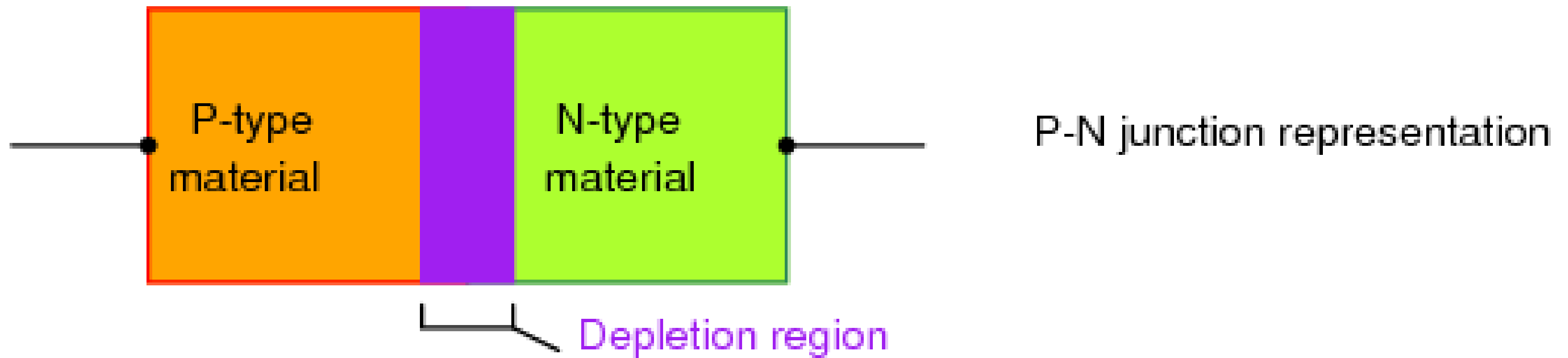
t : rise/fall time of inputs

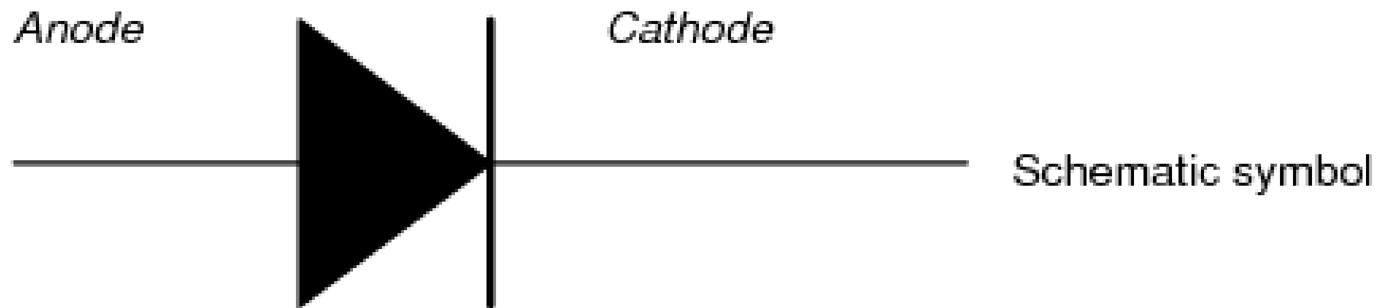
† P_{SHORT} usually $\leq 10\%$ of P_{SWITCH}

Smaller as $V_{DD} \rightarrow V_T$

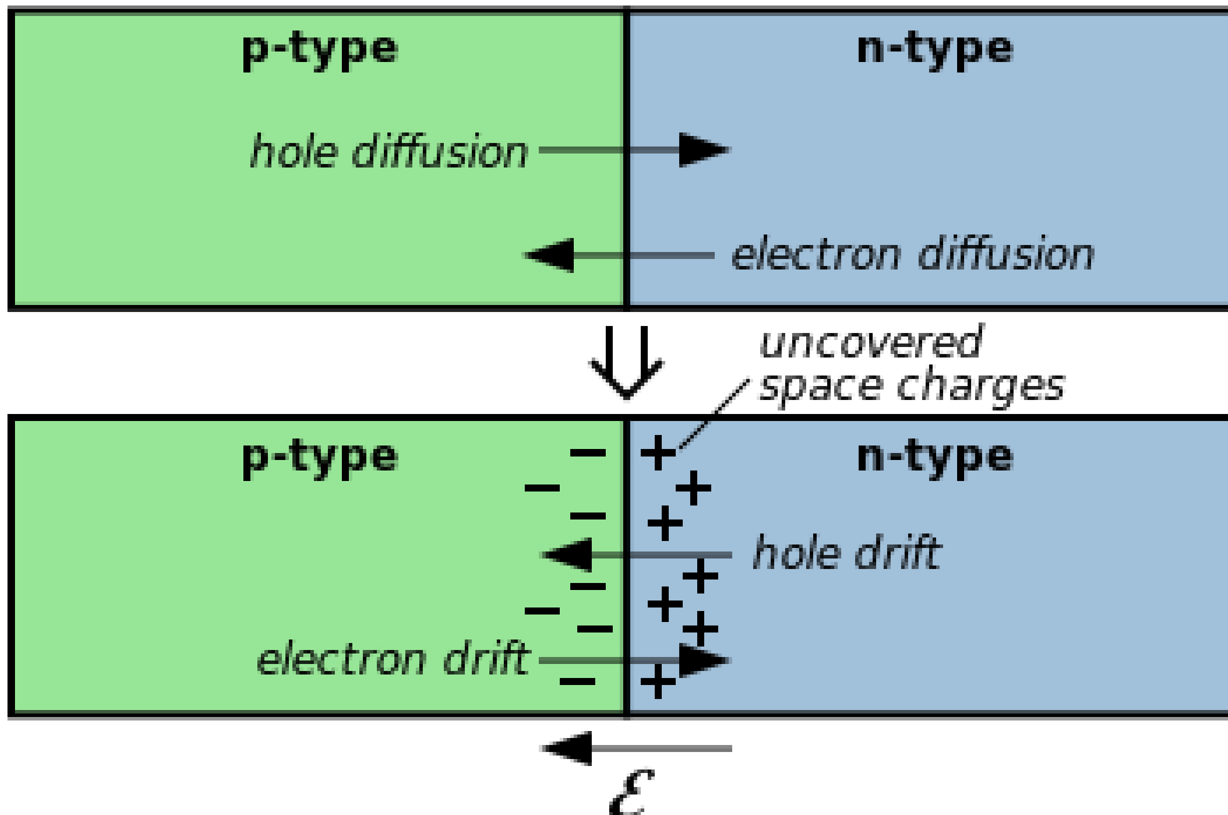
$A < 0.5$ for combinational nodes, 1 for clocked nodes.

Diode



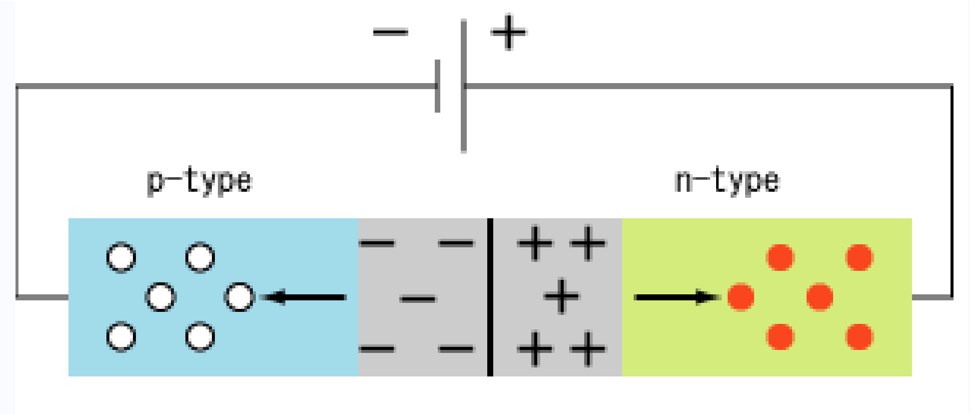


Diode

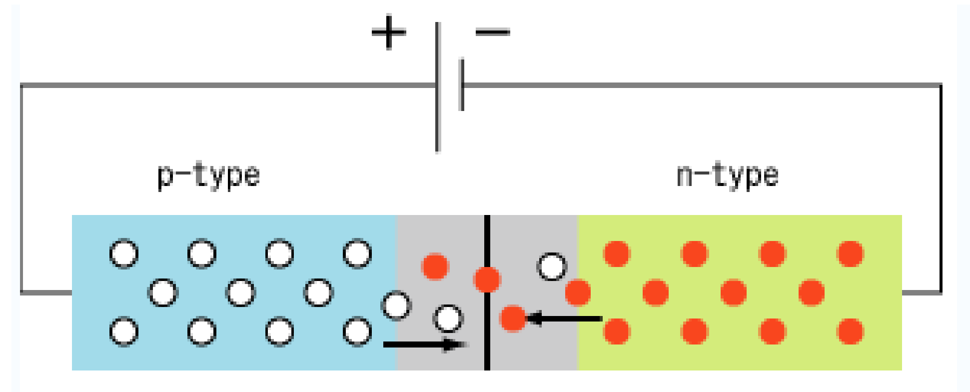


Diode

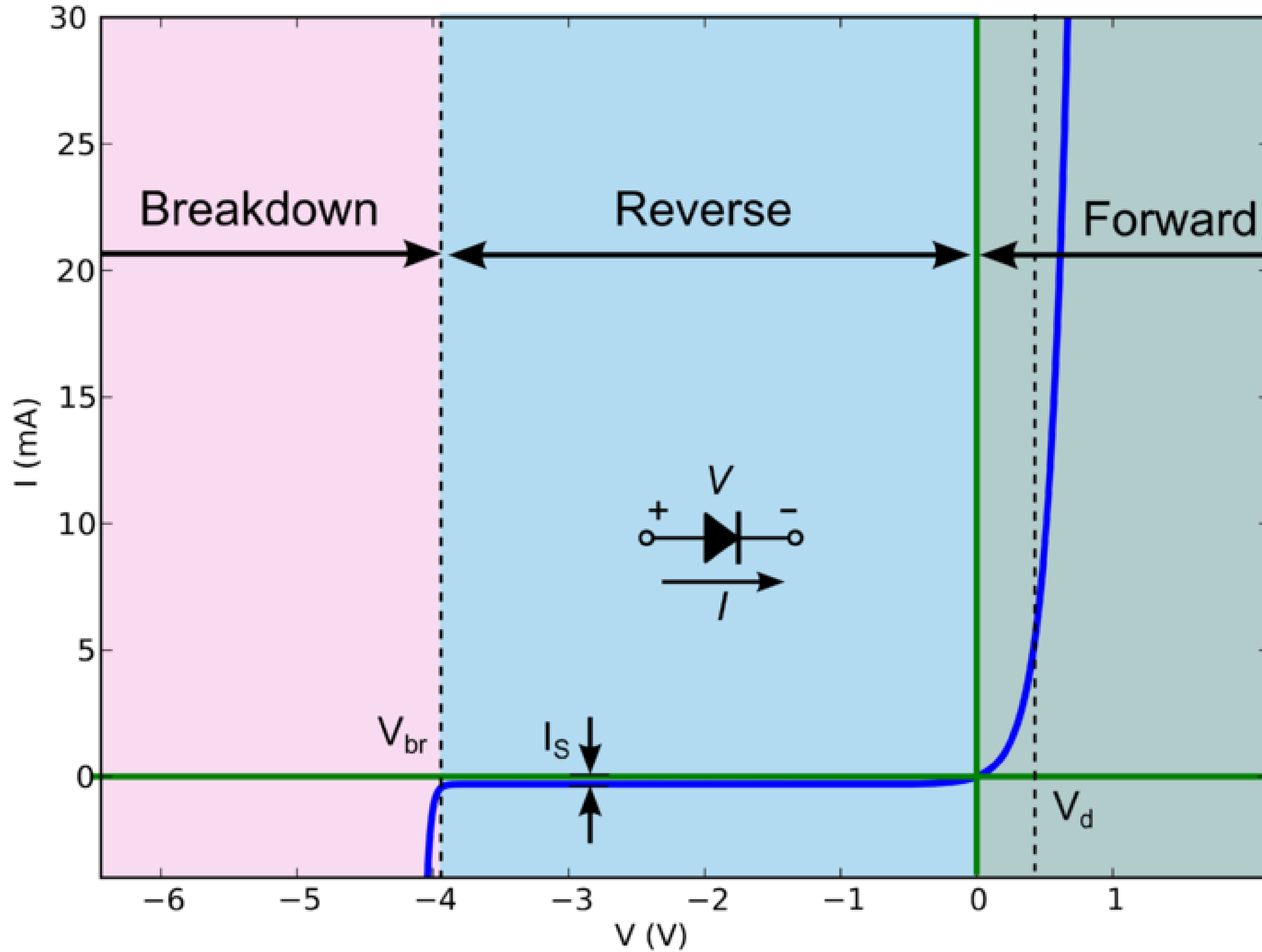
- Reverse Bias



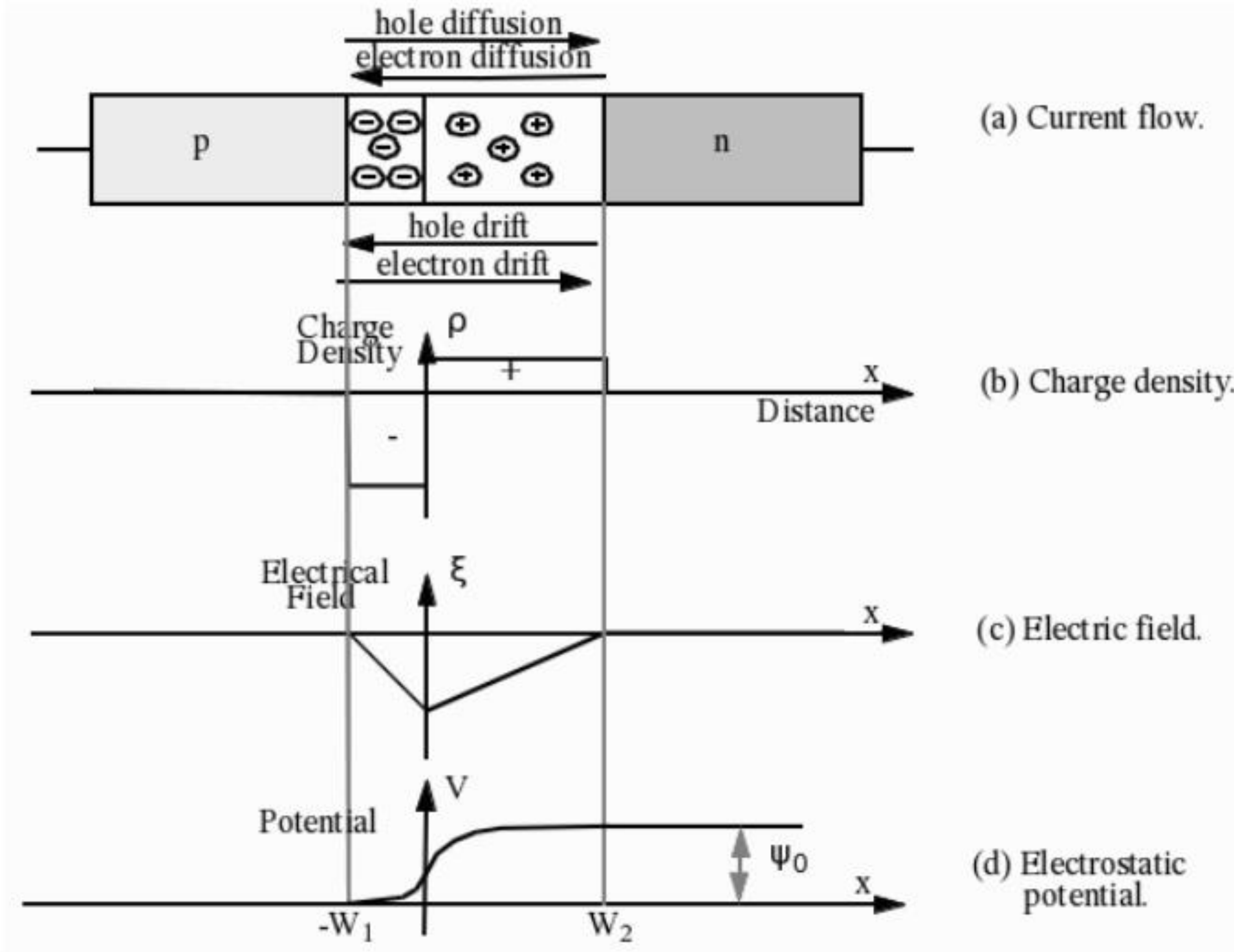
- Forward Bias



Diode



Diode



Built-in Potential
Depletion Region Width

$$\Phi_0 = \Phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$\Phi_T = \frac{kT}{q}$$

$$W \approx \left[\frac{2\epsilon_r\epsilon_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\Phi_0\right]^{\frac{1}{2}}$$

- n_i: intrinsic charge carrier concentration.
- N_x: acceptor and donor concentrations.
- k: Boltzmann constant
- T: temperature
- q: elementary charge

Diode Current

$$I_D = I_S \left(e^{\frac{V_D}{\phi_T}} - 1 \right)$$

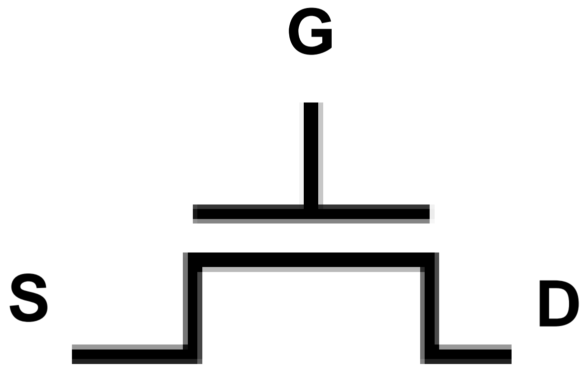
- I_D: diode current
- V_D: diode voltage
- I_S: saturation current constant
- $\phi_T = \frac{kT}{q}$: thermal voltage
  - k: Boltzmann constant
  - T: temperature
  - q: elementary charge

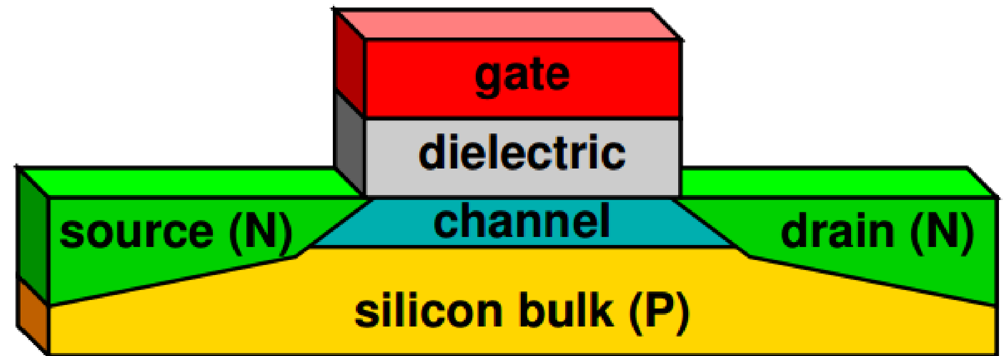
Diffusion capacitance

$$C_{J0} = A_D \sqrt{\frac{\epsilon_{Si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{\phi_0}}$$

- A_D: area of diode
- ϵ_{Si}: permittivity of silicon
- N_X: carrier density
- $\phi_0 = \phi_T \ln \frac{N_A N_D}{n_i{}^2}$
  - $\phi_T = \frac{kT}{q}$
  - n_i: intrinsic carrier concentration

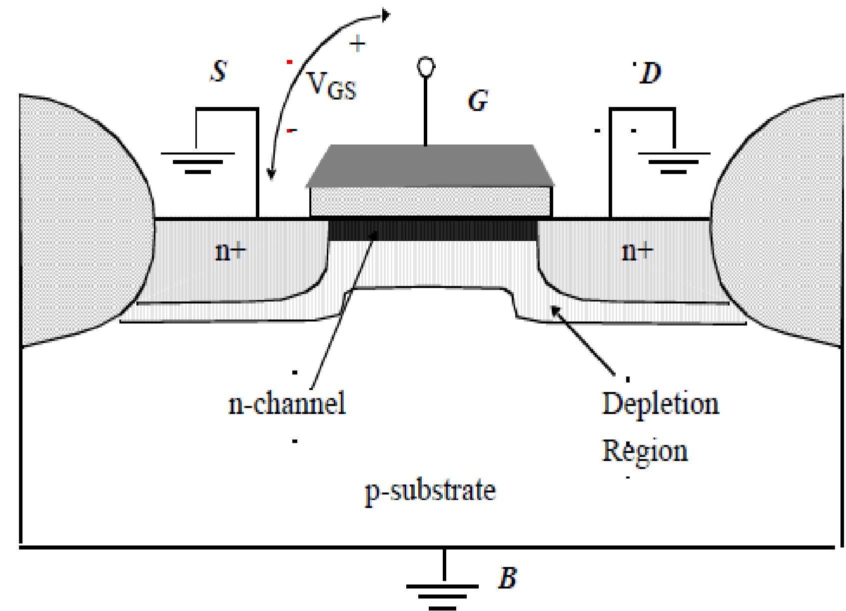
NMOS



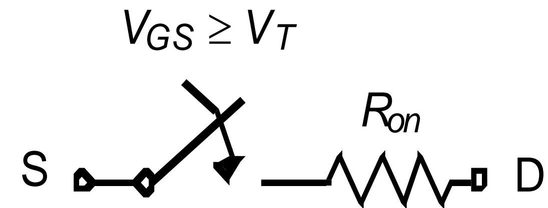


Threshold Voltage

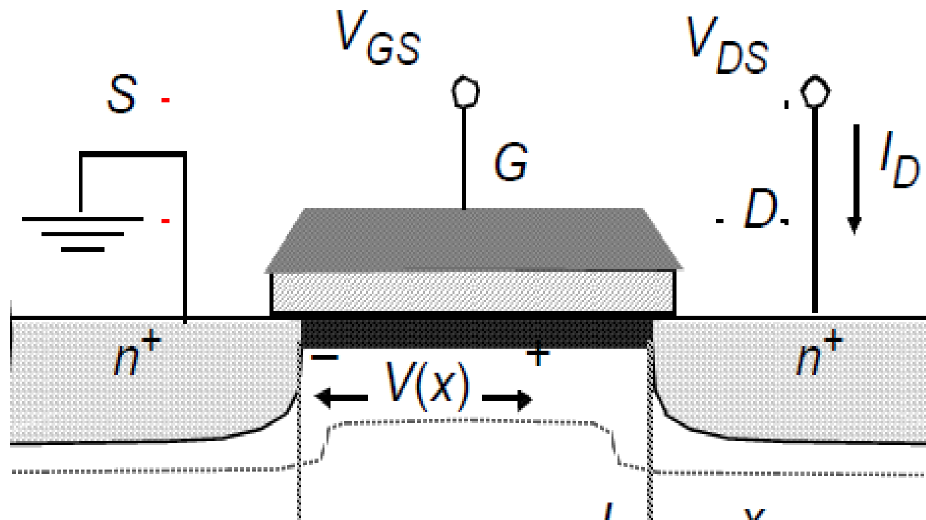
- $0 < V_{GS} < V_T$
  - Repel mobile holes and accumulation of electron beneath the gate oxide



- $V_{GS} > V_T$
  - Surface is as strongly n-type as the substrate is p-type



Operation Regions – Linear (lab 2)



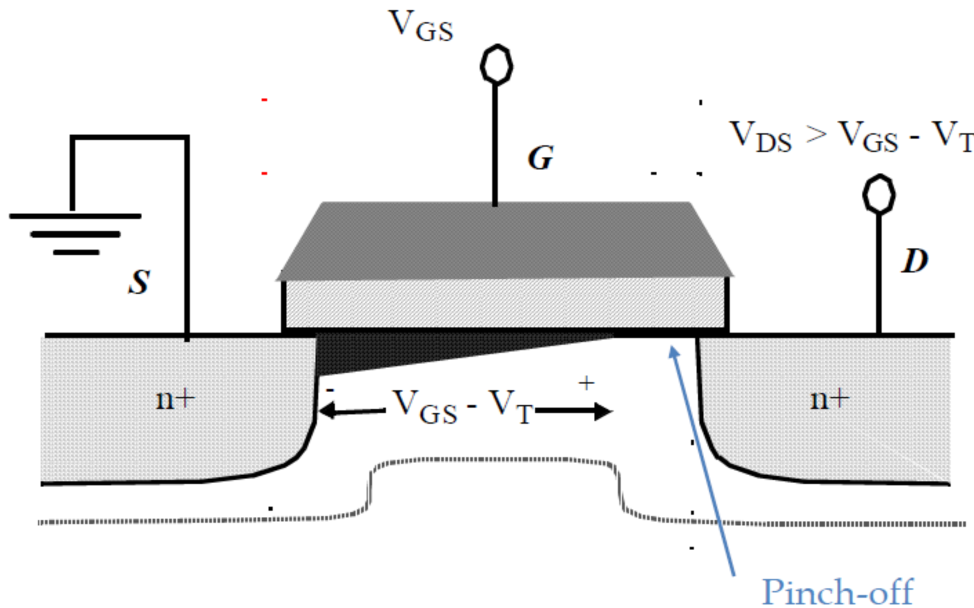
1. $V_{GS} > V_T$
2. $V_{GS} - V_T > V_{DS}$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

3. Linear contribution of V_{GT} to I_D
4. $k'_n = \mu_n C_{ox}$

In case of a P-type MOSFET, the inequalities used above should be directed opposite

Operation Regions – Saturation (lab 2)



1. $V_{GS} > V_T$
2. $V_{GS} - V_T \leq V_{DS}$

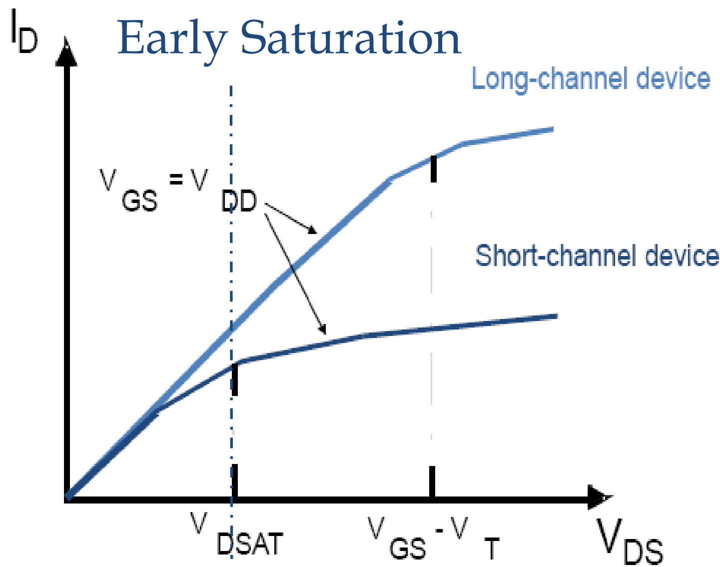
$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

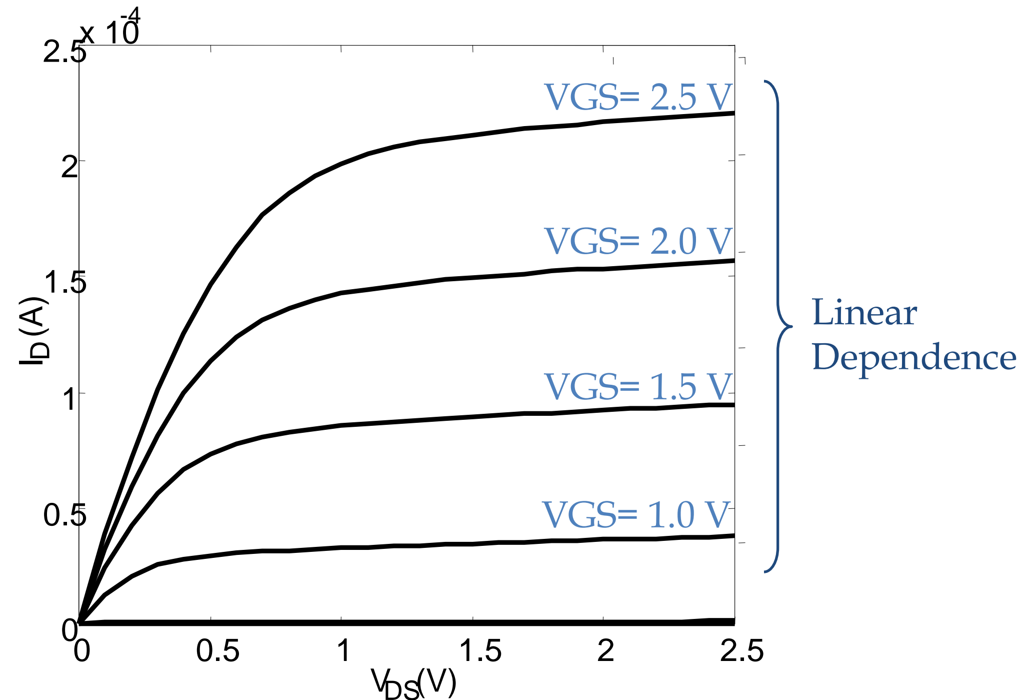
3. Quadratic contribution of V_{GT} to I_D
4. λ channel-length modulation parameter

In case of a P-type MOSFET, the inequalities used above should be directed opposite

Operation Regions – Velocity Saturated

Short Channel Effects

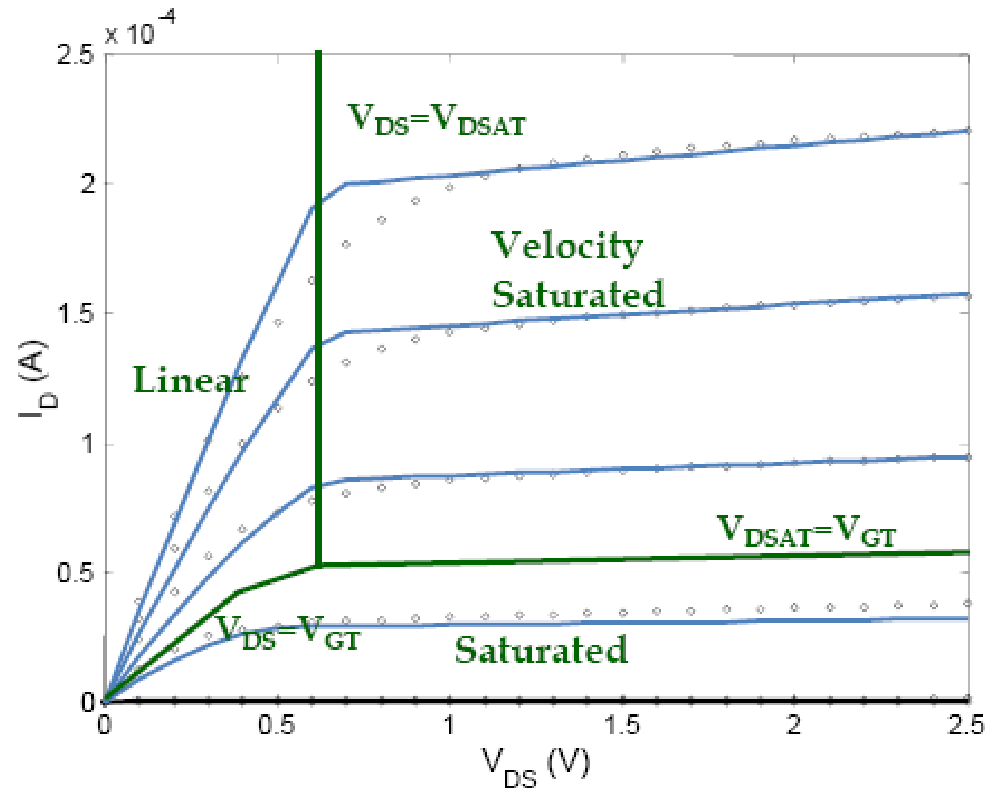




Strong electric field causes carrier mobility degradation

: Compared to feature scaling, voltage scaling is lagging behind

A unified model



$$I_D = 0 \ \text{for} \ V_{GT} \leq 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \ \text{for} \ V_{GT} \geq 0$$

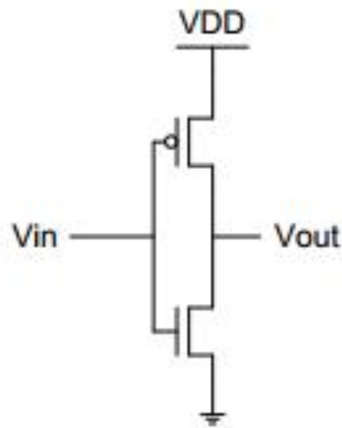
with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

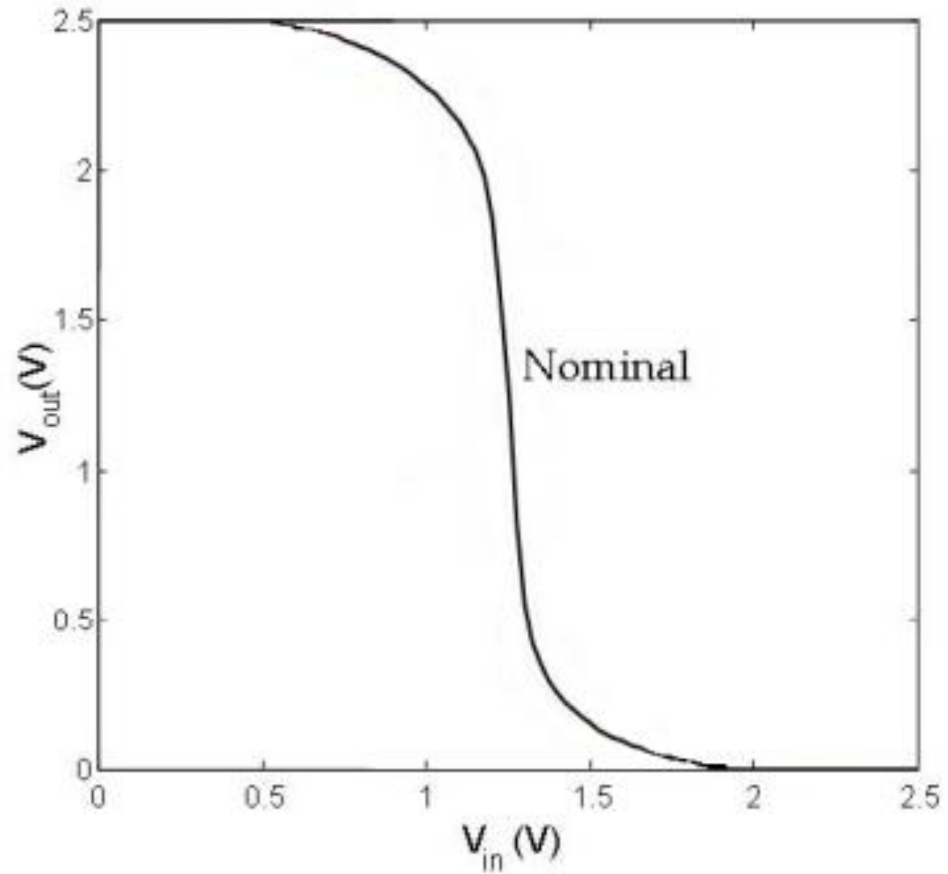
$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

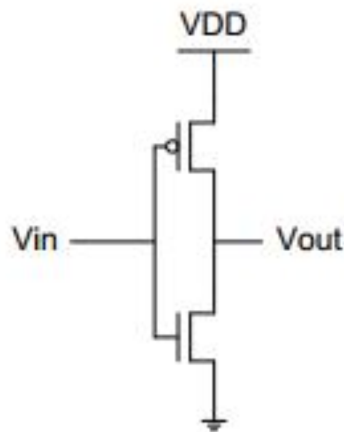
1. If V_{DS} is minimum:
   Linear region
2. If V_{GT} is minimum:
   Saturation Region
3. If V_{DSAT} is minimum :
   Velocity saturated region

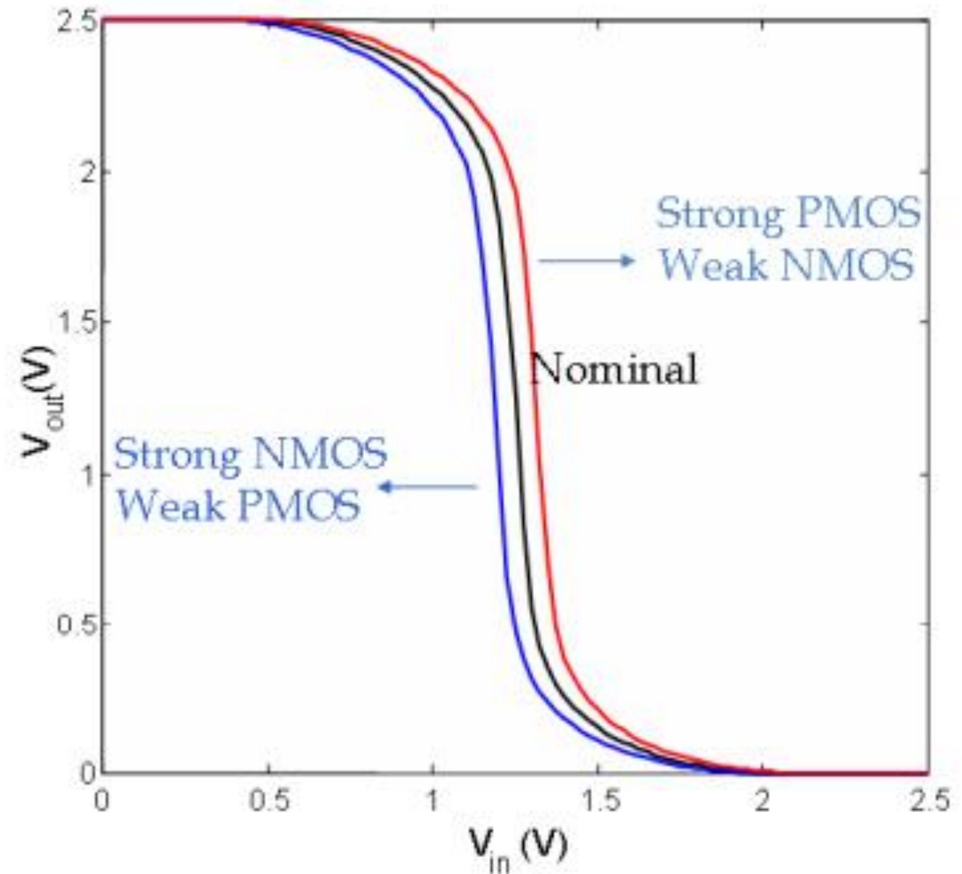
CMOS Inverter



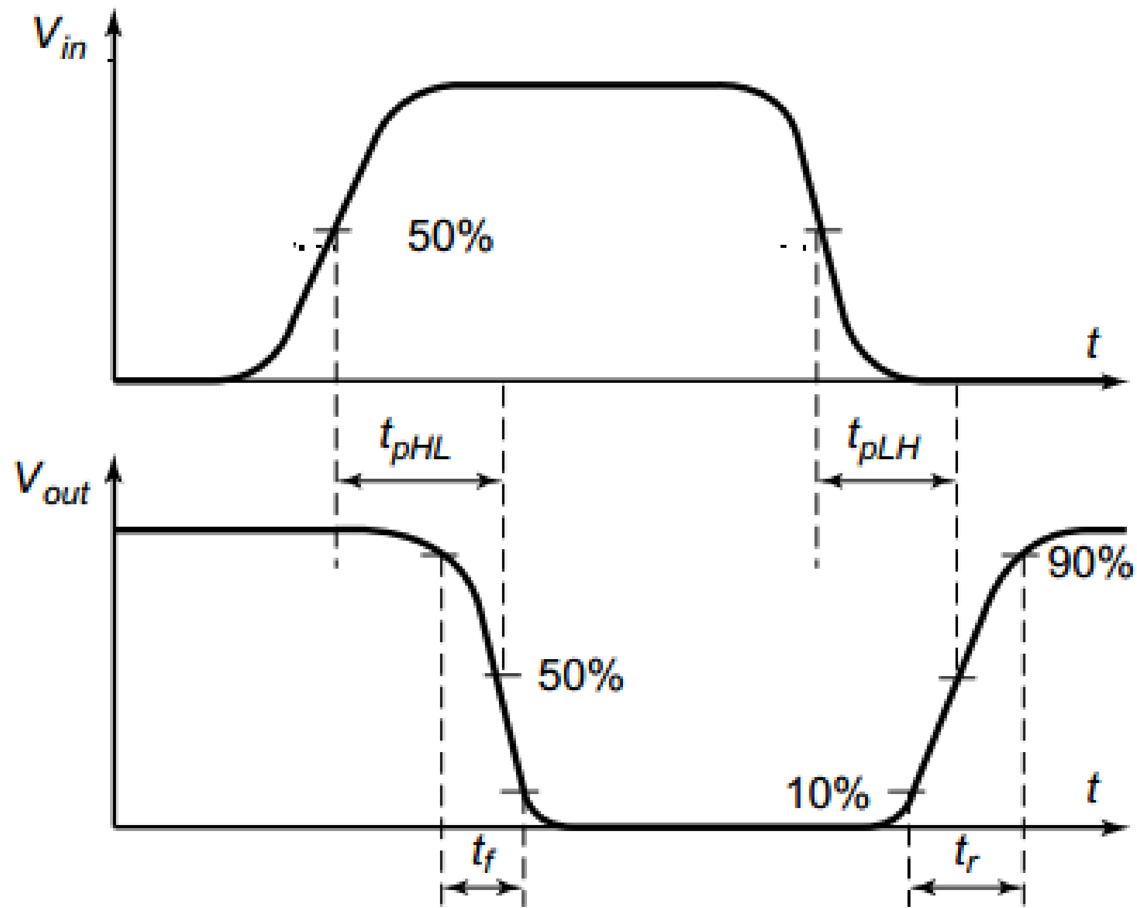


CMOS Inverter

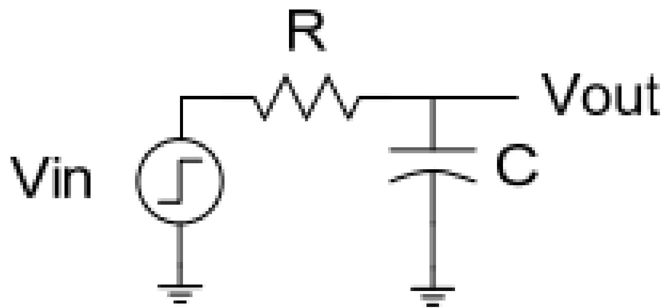




Delay Definition



A Frist-Order RC Network



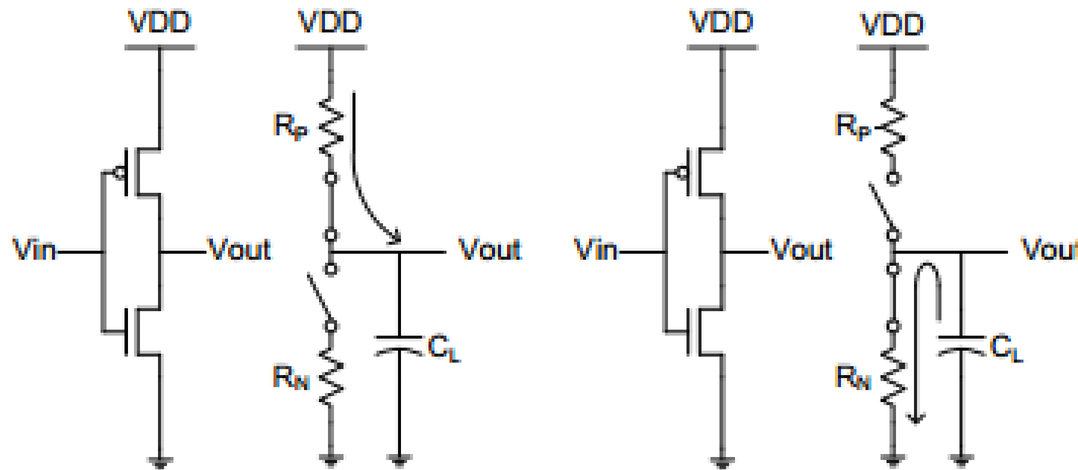
$$V_{out}(t) = (1 - e^{-t/\tau})V$$

$$\tau = R \times C$$

$$t_p = \ln(2)\tau = 0.69 R \times C$$

50% voltage

CMOS Inverter: Transient Response



(a) Low-to-high

(b) High-to-low

$$t_{pHL} = f(R_N \times C_L)$$

$$t_{pHL} = 0.69 R_N \times C_L$$

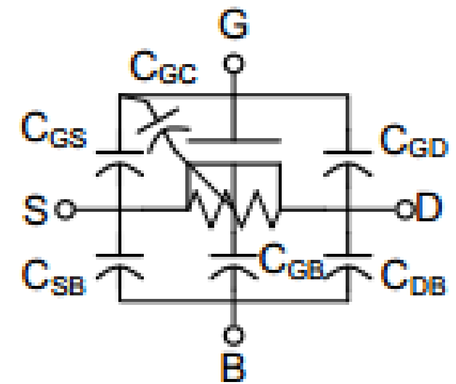
$$t_{pLH} = 0.69 R_p \times C_L$$

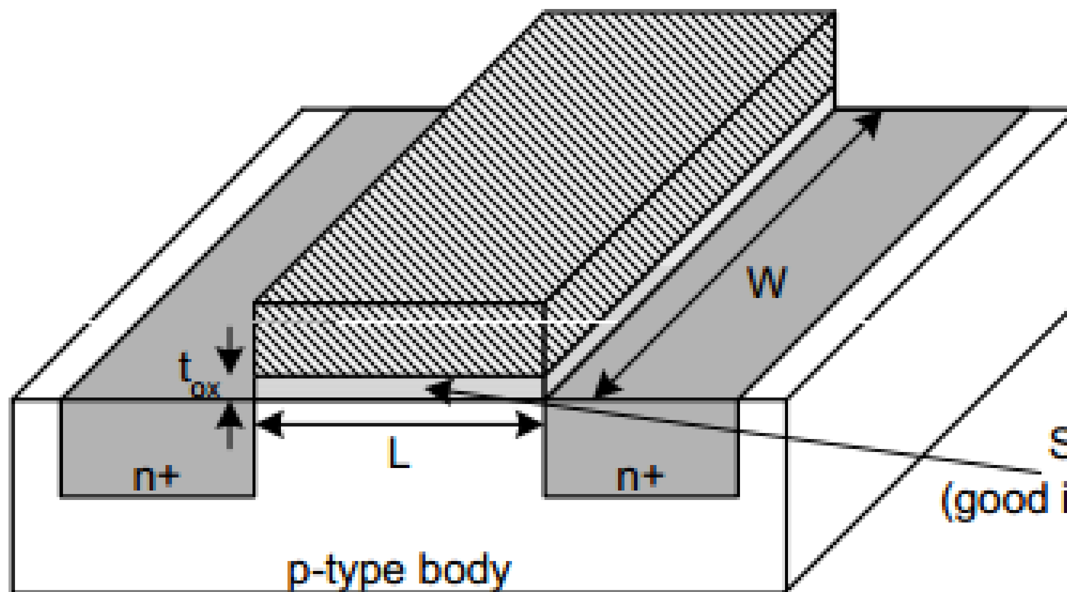
Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

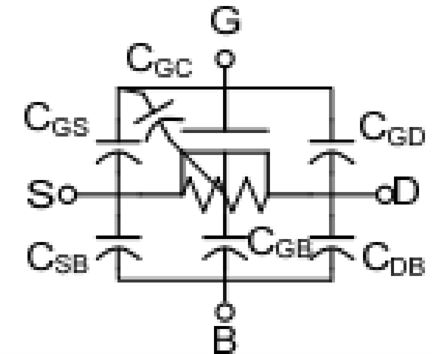
- Gate capacitance can be complex, but we will use a simple model
- $C_{GC} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{per_micron}W$

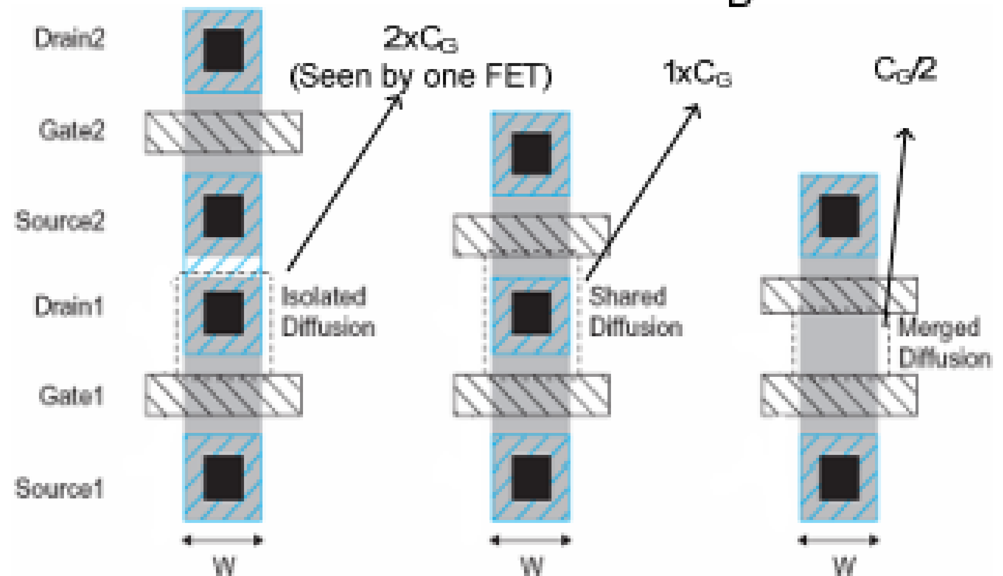




Diffusion Capacitance

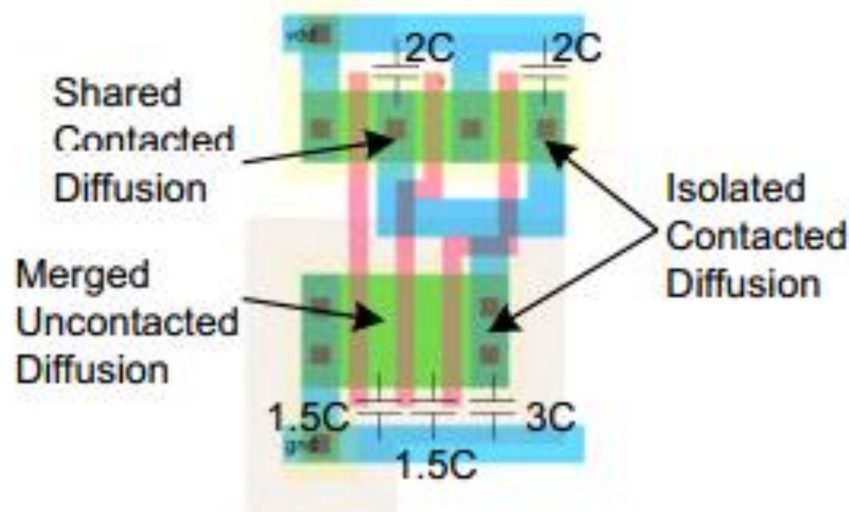
- C_{SB}, C_{DB}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_G for contacted diff
  - ½ C_G for uncontacted
  - Varies with process

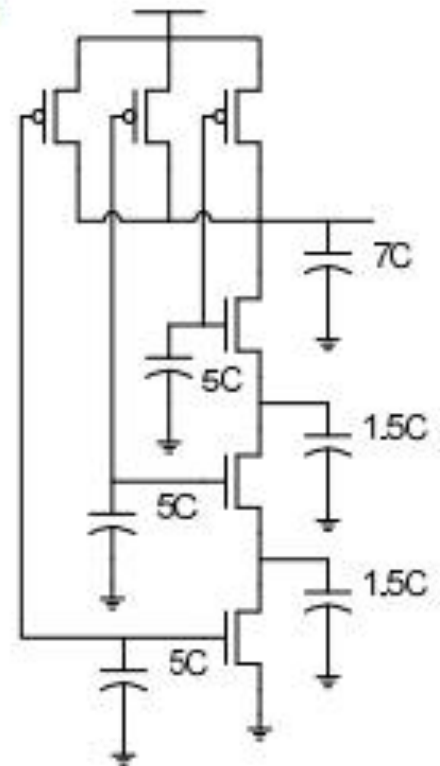




Diffusion Capacitance: Example

- Easiest to assume a contacted diffusion on every source/drain
- BUT: Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion helps also





Design for Performance

- Keep capacitances small – lower C
  - Compact layout, good placement (short wires & no diffusion routing)
- Increase transistor sizes – lower R
  - Watch out for self-loading! – parasitic C increases!
- Increase V_{DD}
  - Not usually possible due to reliability and power penalties

Device Sizing

x 10^-11

3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2

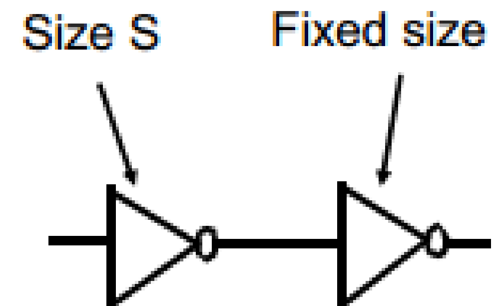
t_p (sec)

(for fixed load)

2 4 6 8 10 12 14

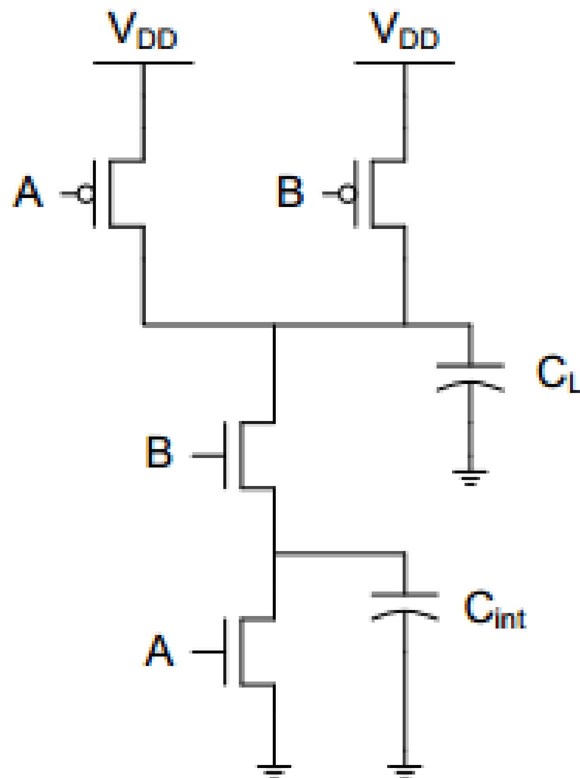
S

$S = Wp/Wp_min = Wn/Wn_min$



Increasing device width
Leads to self-loading:
Intrinsic capacitances
dominate

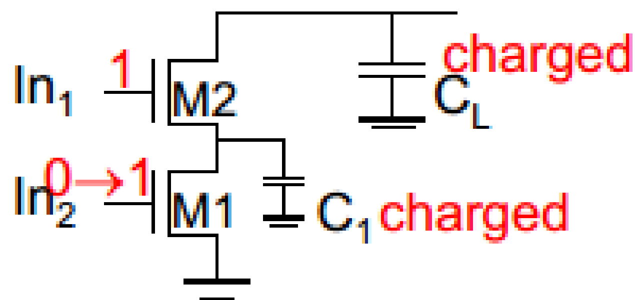
Input Pattern Effects on Delay

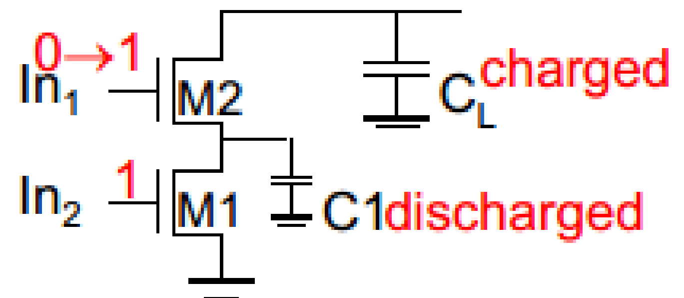


- Delay is dependent on the pattern of inputs
- *Ignore Cint for the moment!*
- Low to high transition
  - both inputs go low
    - delay is 0.69 $R_p/2$ C_L
  - one input goes low
    - delay is 0.69 R_p C_L
- High to low transition
  - both inputs go high
    - delay is 0.69 $2R_n$ C_L

Fast Complex Gates: Design Techniques

- Transistor Ordering

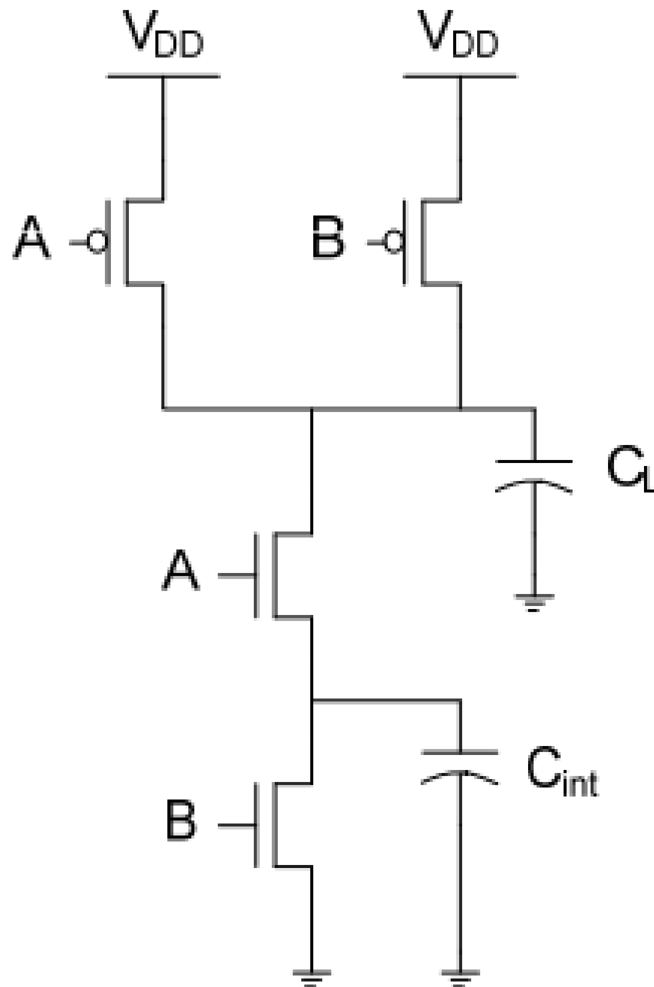




delay determined by time to discharge C_L, C_1

delay determined by time to discharge C_L

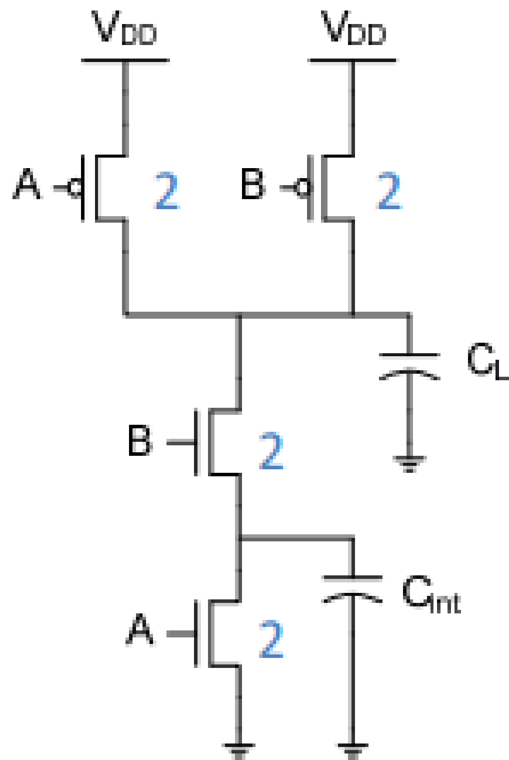
Delay Dependence on Input Patterns

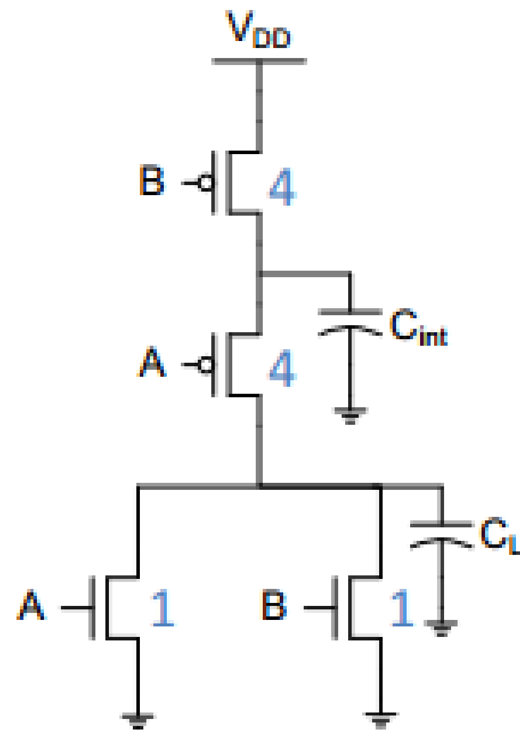


Input Data Pattern	Delay (psec)
A=B=0→1	69
A=1, B=0→1	62
A= 0→1, B=1	50
A=B=1→0	**35**
A=1, B=1→0	**76**
A= 1→0, B=1	57

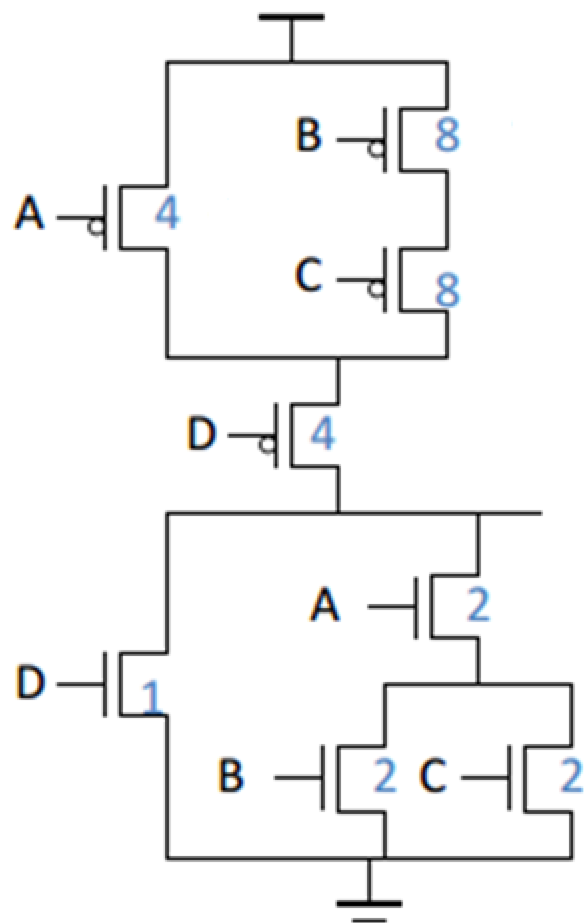
NMOS = 0.5μm/0.25 μm
PMOS = 0.75μm/0.25 μm
C_L = 100 fF

Transistor Sizing





Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$