EECS 312 Discussion 13
Review 2

12/03

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Logic Effort

Logical Effort Motivation

- Sizing of a chain of inverters
  - Geometric progression
- How about more complex logic?
- Logical Effort objectives:
  - Quick & dirty, back of the envelope sizing
  - Make trade-off between circuits
  - What is the best circuit topology for a function?
  - How many stages of logic give least delay?
  - How wide should the transistors be?

Delay in a Logic Gate

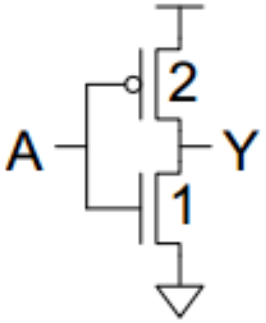
- Express delays in process-independent unit
- Delay has two components:

$$d = f + p$$

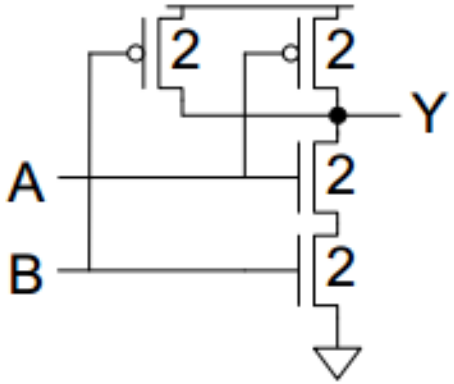
- f: *effort delay* = gh (a.k.a. stage effort)
  - Again has two components
- g: *logical effort*
  - Measures relative ability of gate to deliver current
  - $g \equiv 1$ for inverter
- h: *electrical effort* = C_{out} / C_{in}
  - Ratio of output to input capacitance
  - Sometimes called fanout
- p: parasitic delay
  - Represents delay of gate driving no load
  - Set by internal parasitic capacitance

Computing Logical Effort

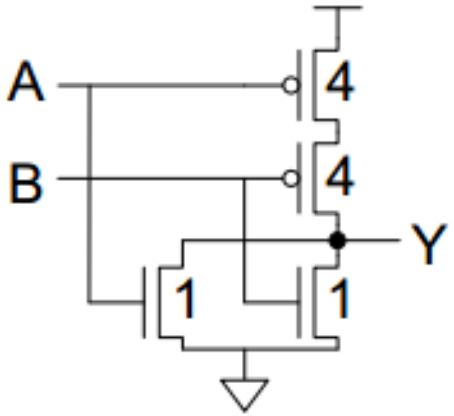
- DEF: *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current (i.e, effort delay under same loading)*.
- Measure from delay vs. fanout plots
- Or estimate by counting transistor widths



C_{in} = 3
g = 3/3



C_{in} = 4
g = 4/3



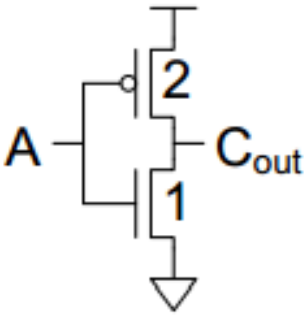
C_{in} = 5
g = 5/3

Logical effort (g)

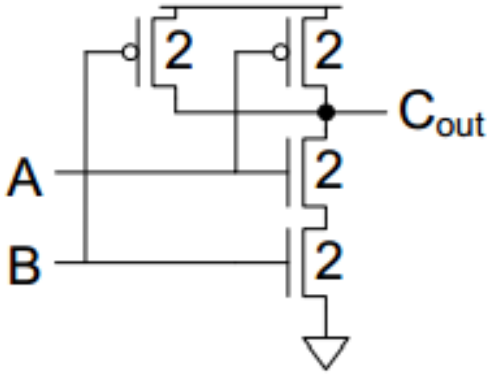
	Number of inputs					
Gate type	**1**	**2**	**3**	**4**	**5**	**n**
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n + 2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3
Multiplexer		2	2	2	2	2

Computing Parasitic Delay

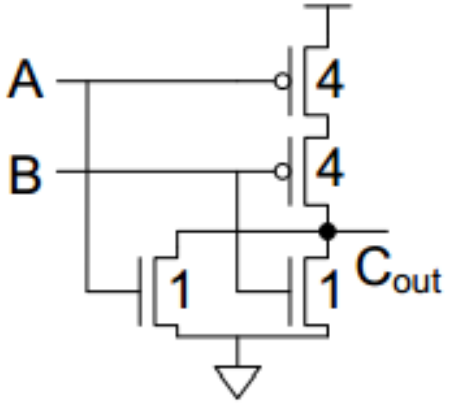
- Measure from delay vs. fanout plots
- Or estimate by counting self loading on output node for sizing with equal output current to inverter
- For simplification, we ignore internal node capacitance



$C_{out} = 3$
$p = 3/3$



$C_{out} = 6$
$p = 6/3 = 2$

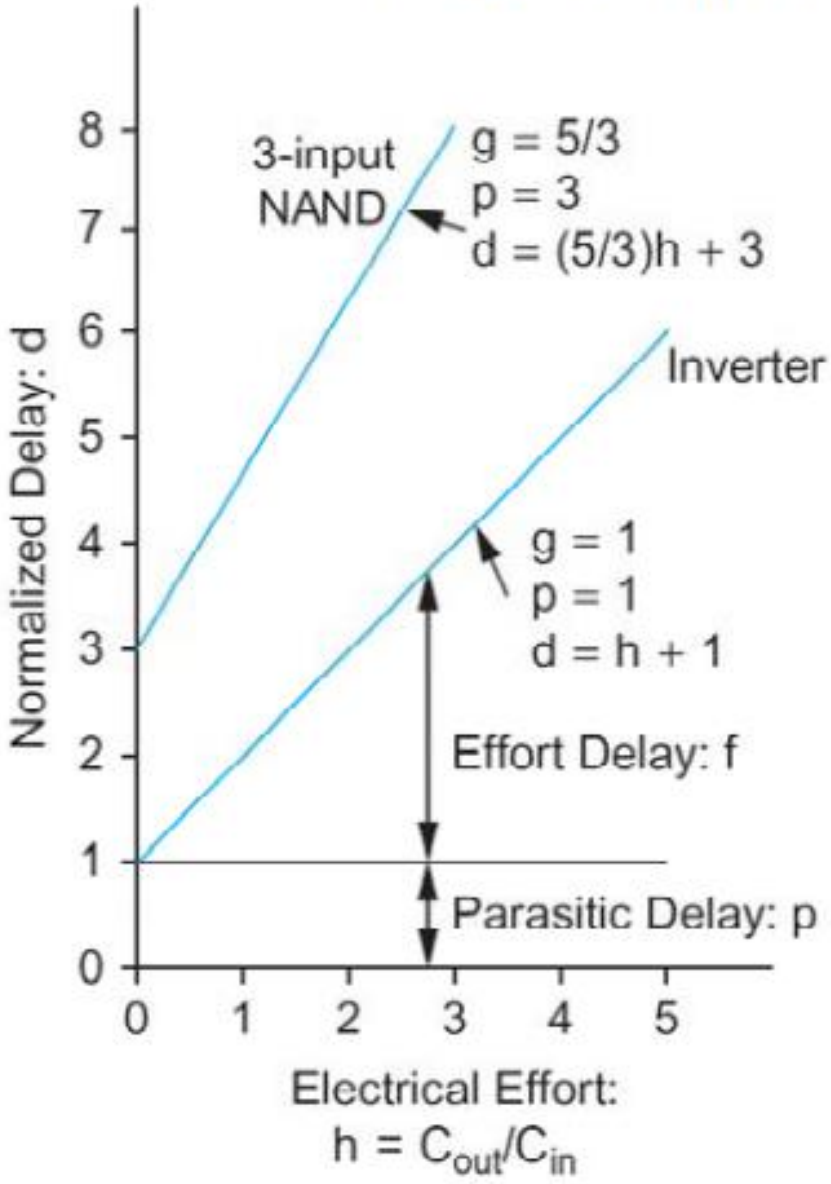


$C_{out} = 6$
$p = 6/3 = 2$

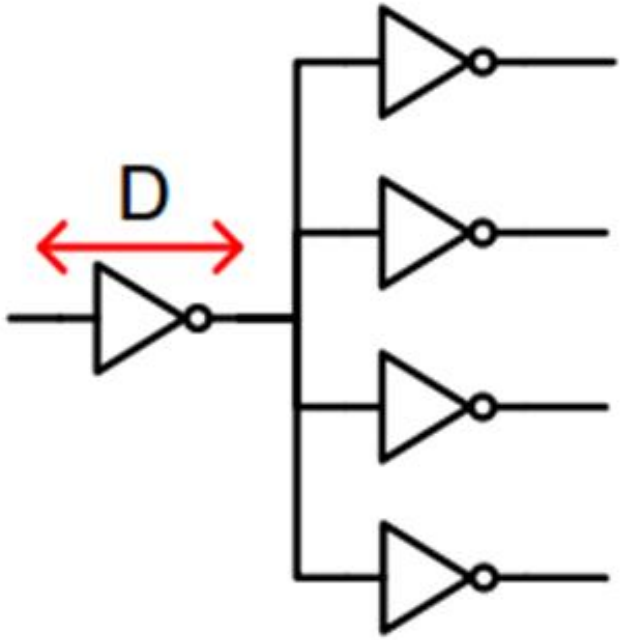
Parasitic Delay (p)

Gate type	Parasitic Delay
Inverter	p_{inv}
n-input NAND	$n.p_{inv}$
n-input NOR	$n.p_{inv}$
n-way multiplexer	$2n.p_{inv}$

Delay components



Fanout 4 Example



$$C_{out} = 4C_{in}$$

$$h = 4$$

$$g = 1$$

$$p = 1$$

$$D = 4 + 1 = 5\tau$$

FO4 delay

96ps of 250nm

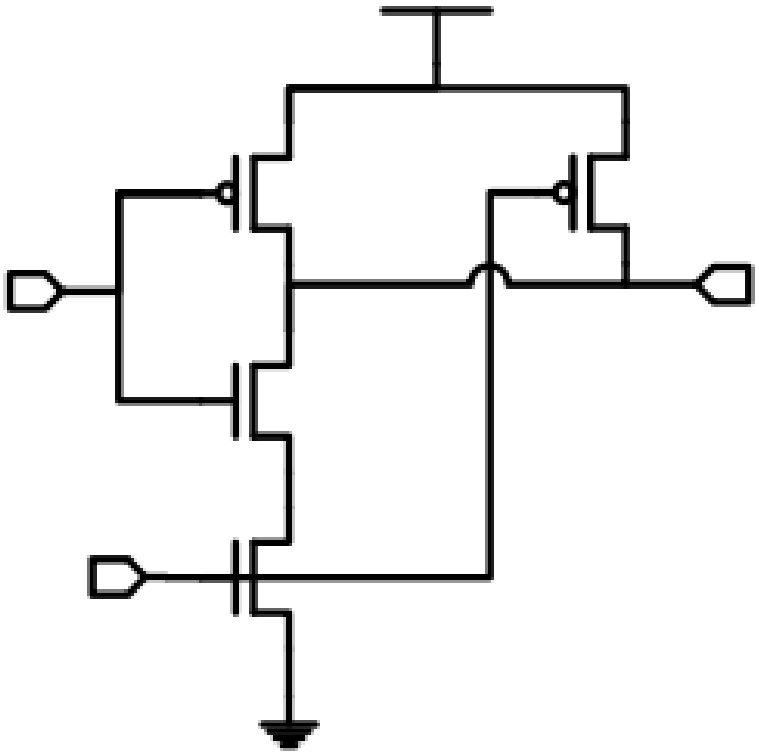
Logic Effort

- Uncovered Topic: Branch

Static Logic Families

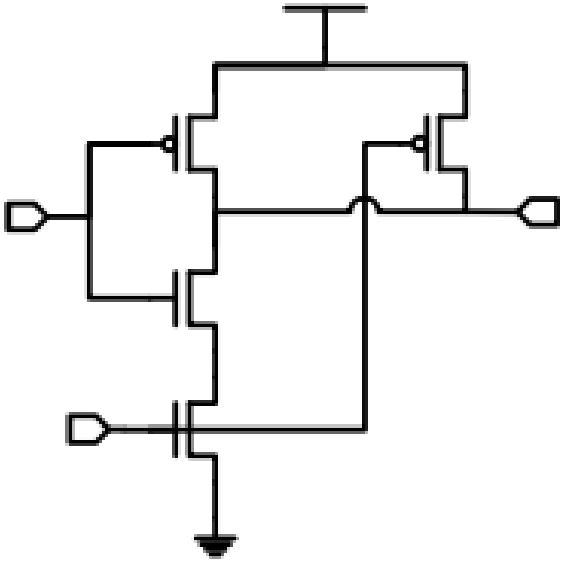
Classic CMOS

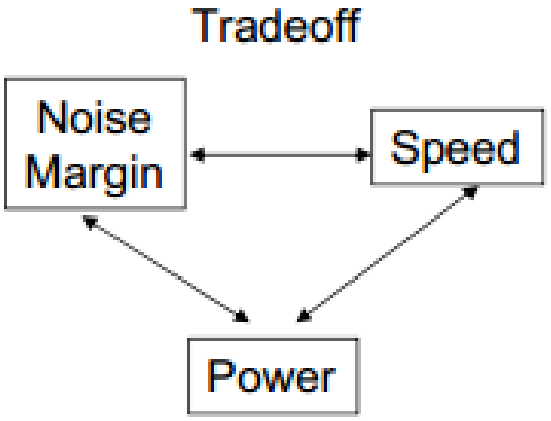
- Advantages:
  - Non-ratioed
  - ~0 static power
  - Low S.C. power ~ 10% of dynamic power
  - Full rail swing
  - Good noise margins
  - True and complement functions



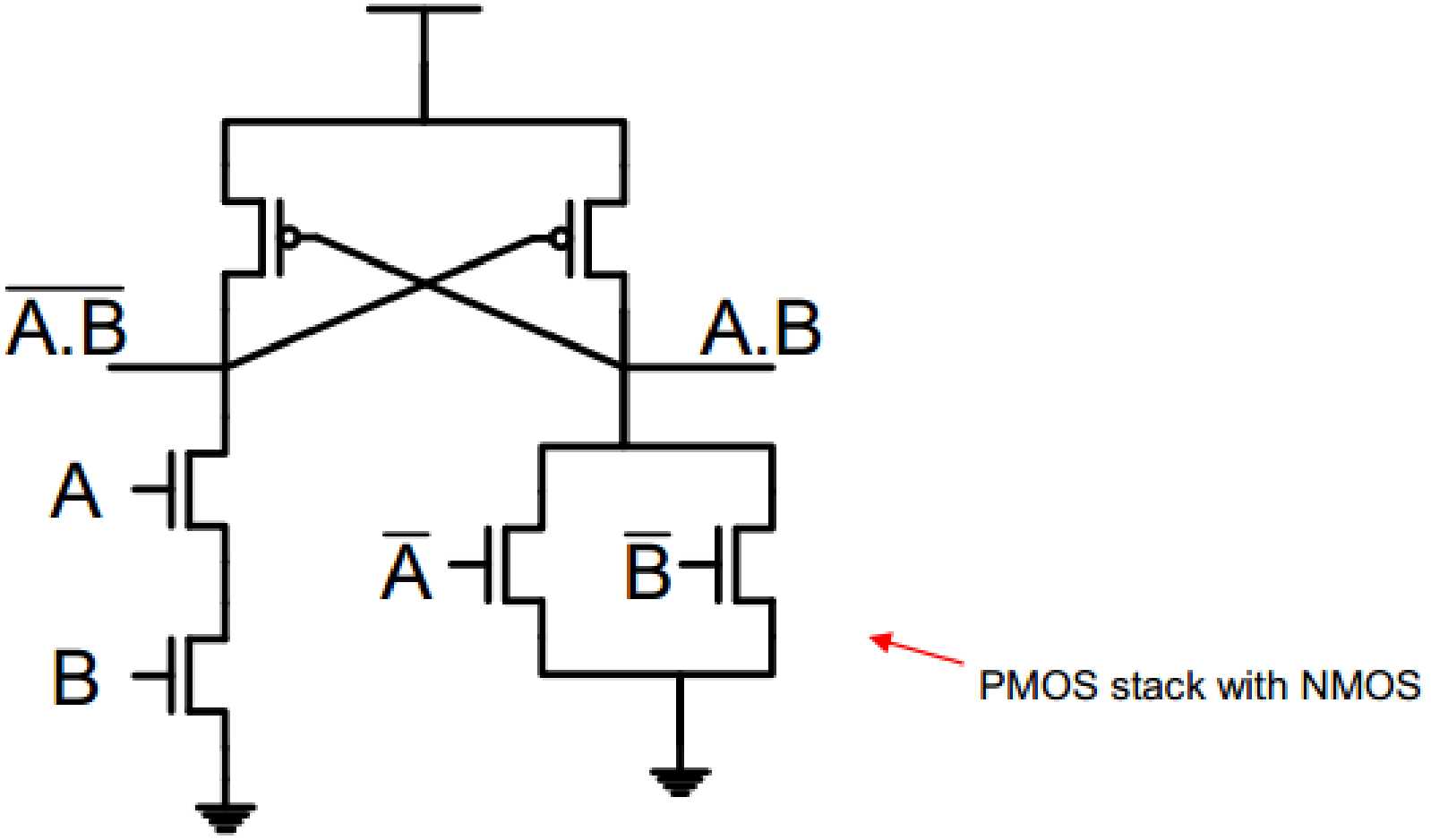
Classic CMOS

- Disadvantages:
  - Large # of transistors, large area
  - Slow
    - PMOS mobility
    - Transistor cap from dual function
  - Increasing static power due to leakage





Differential Cascode Voltage Switch DCVS



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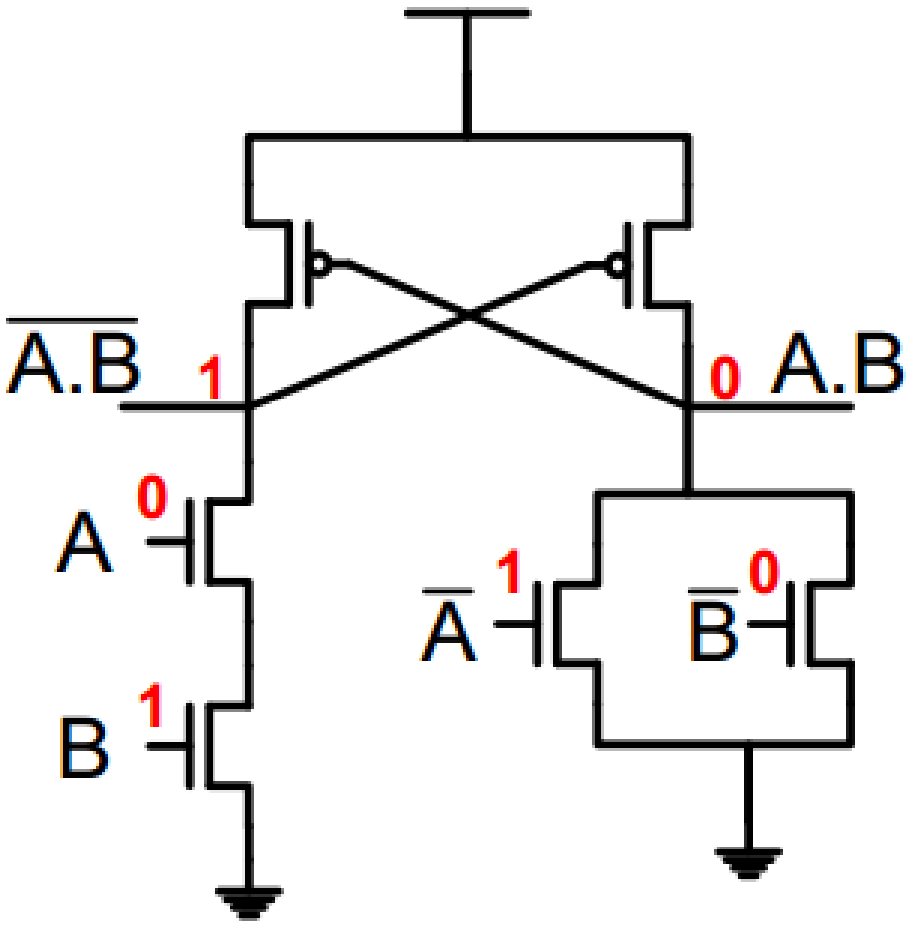
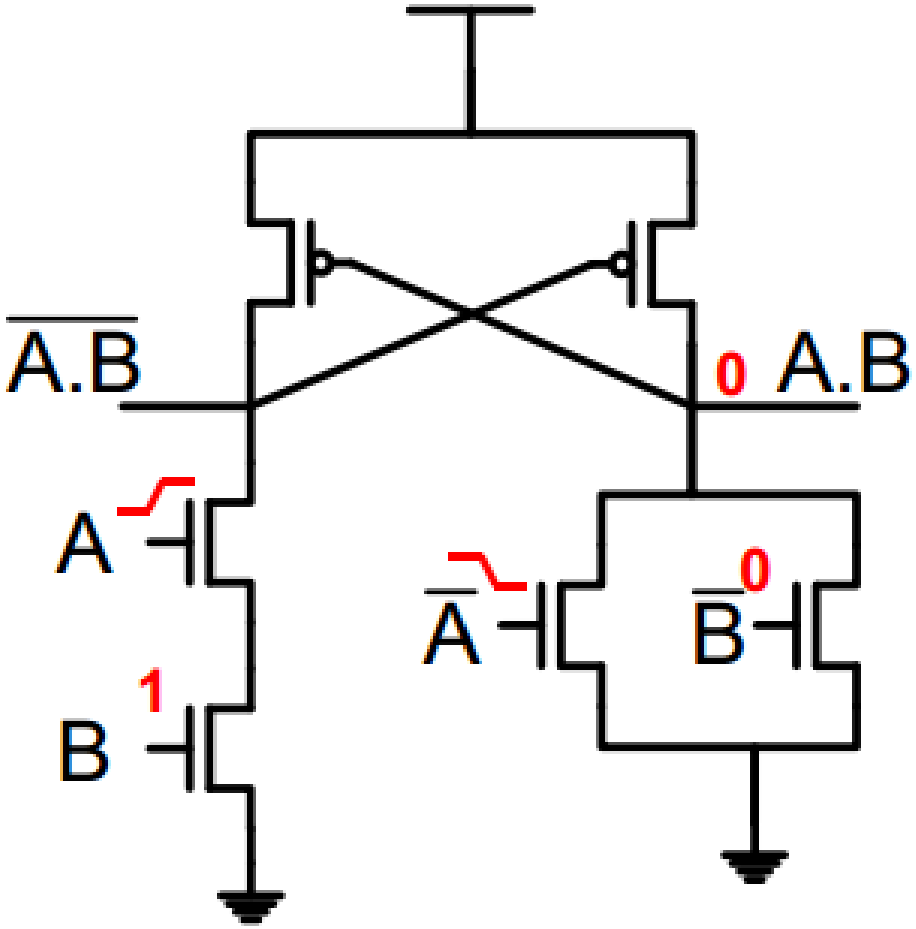
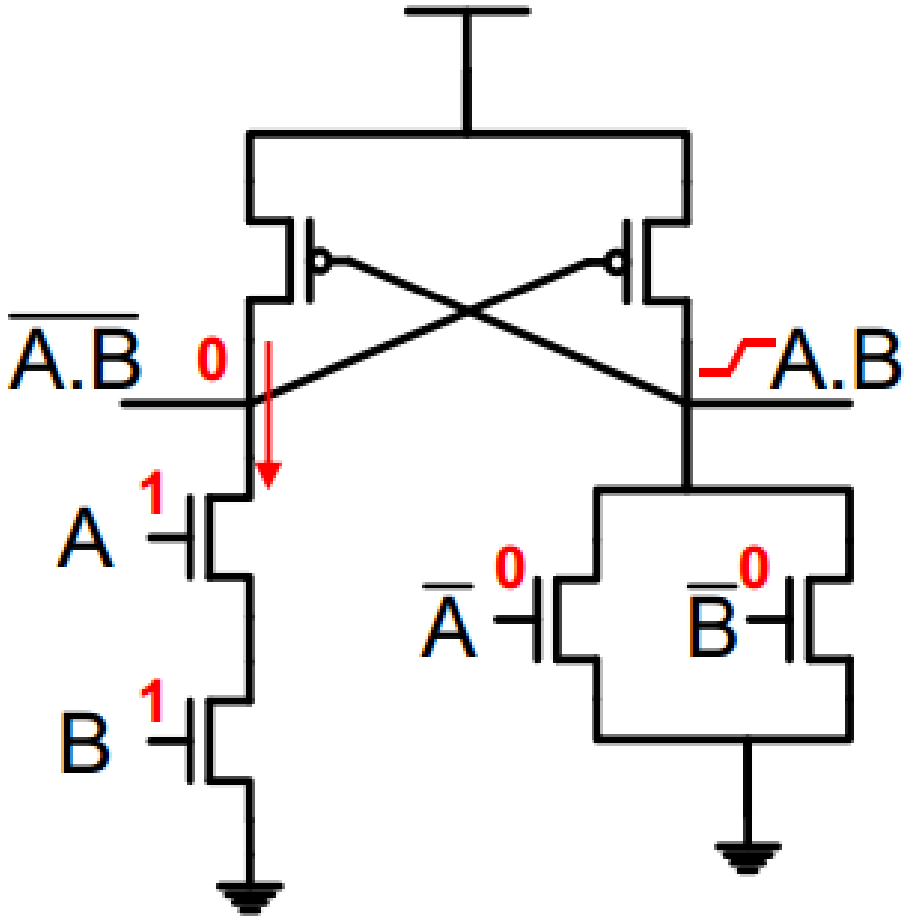


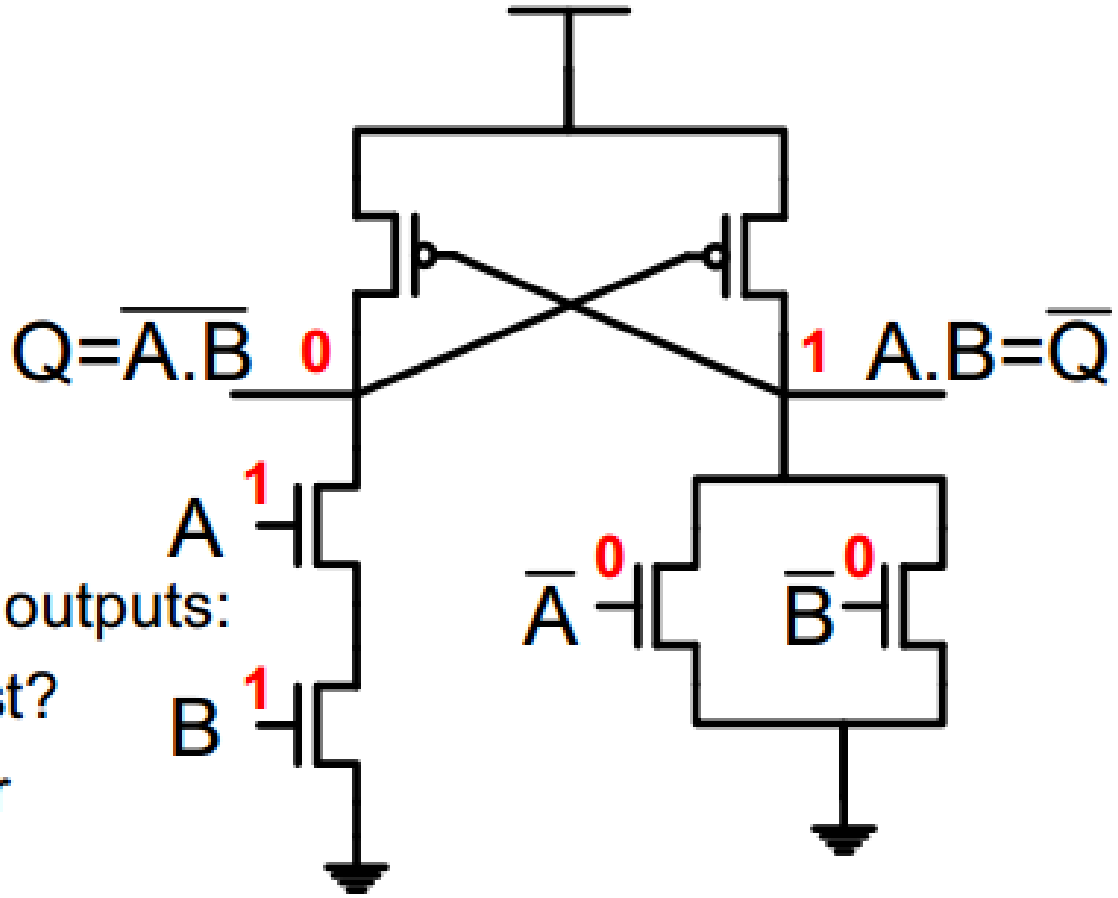
Differential Cascode Voltage Switch DCVS



Differential Cascode Voltage Switch DCVS



Differential Cascode Voltage Switch DCVS

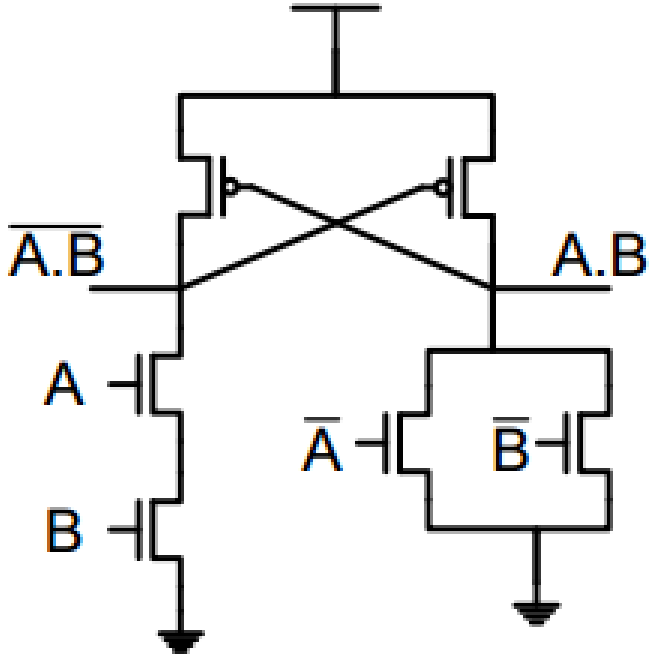


Timing of outputs:

Which first?

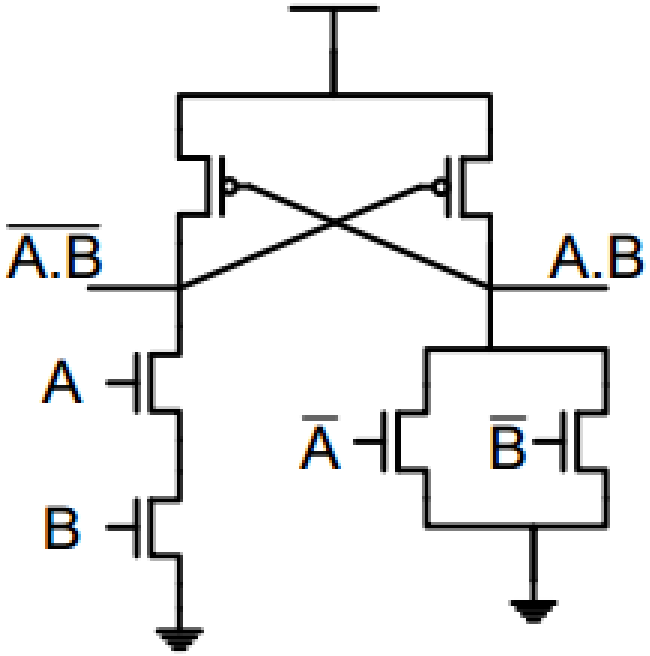
Q or Qbar

Differential Cascode Voltage Switch DCVS



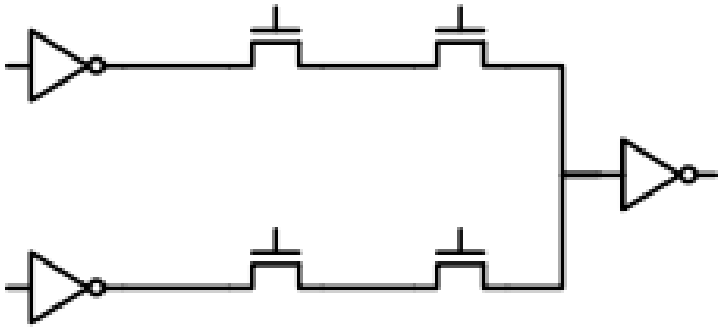
- Advantages:
  - No PMOS duality
    - Lower input cap.
    - Use only NMOS
  - Faster than CMOS
  - Can evaluate complex logic trees in 1 stage

Differential Cascode Voltage Switch DCVS



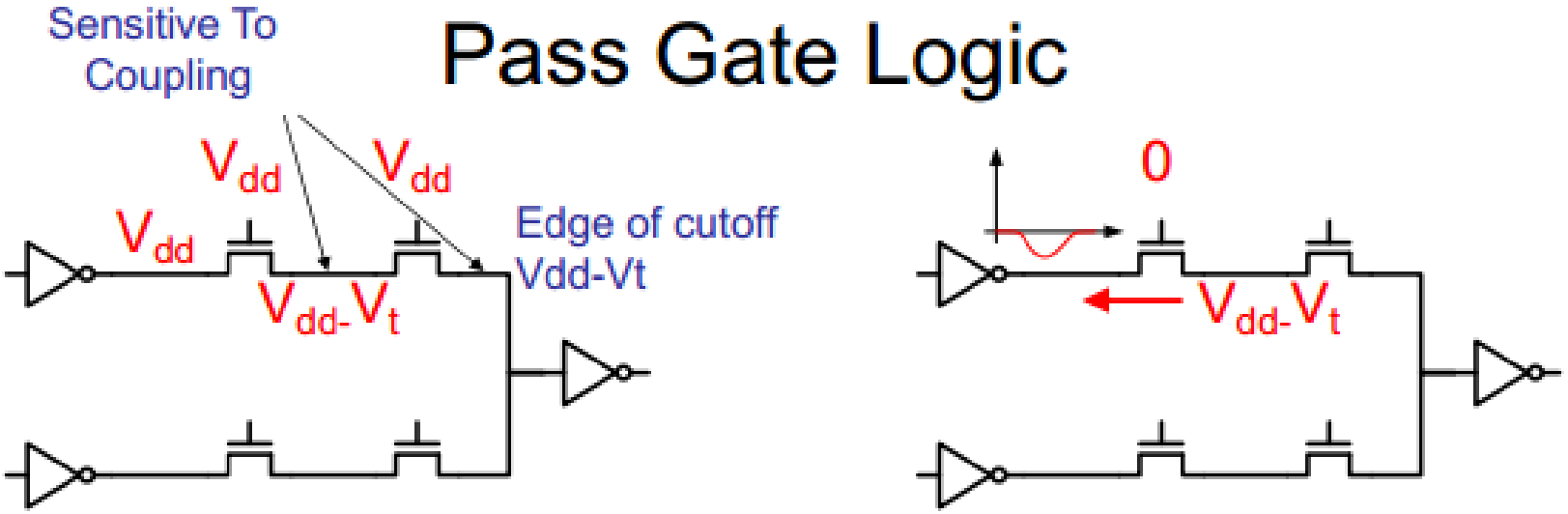
- Disadvantages:
  - Need complementary inputs (dual rail)
  - Cross-bar current
    - Sensitive to input timing
  - Sizing of PMOS is hard
    - Too large → PDN does not switch the output
    - Too small → Slow rise time
- Ratioed Logic?

Pass Gate Logic



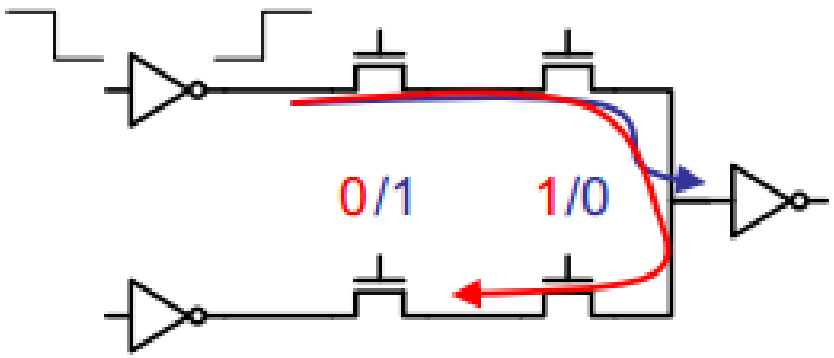
- Advantages:
  - Speed: 20-50% faster (less capacitance)
    - In some circuits, such as XOR/MUX
  - Lower dynamic power

Pass Gate Logic



- Disadvantages:
  - Very sensitive to noise: 2 types
    - Vt drop → must level restore someplace
    - Sensitive to undershot voltage noise on inputs
      - Buffers at inputs suppresses this effect
  - Body effect → limit # of FETs in series

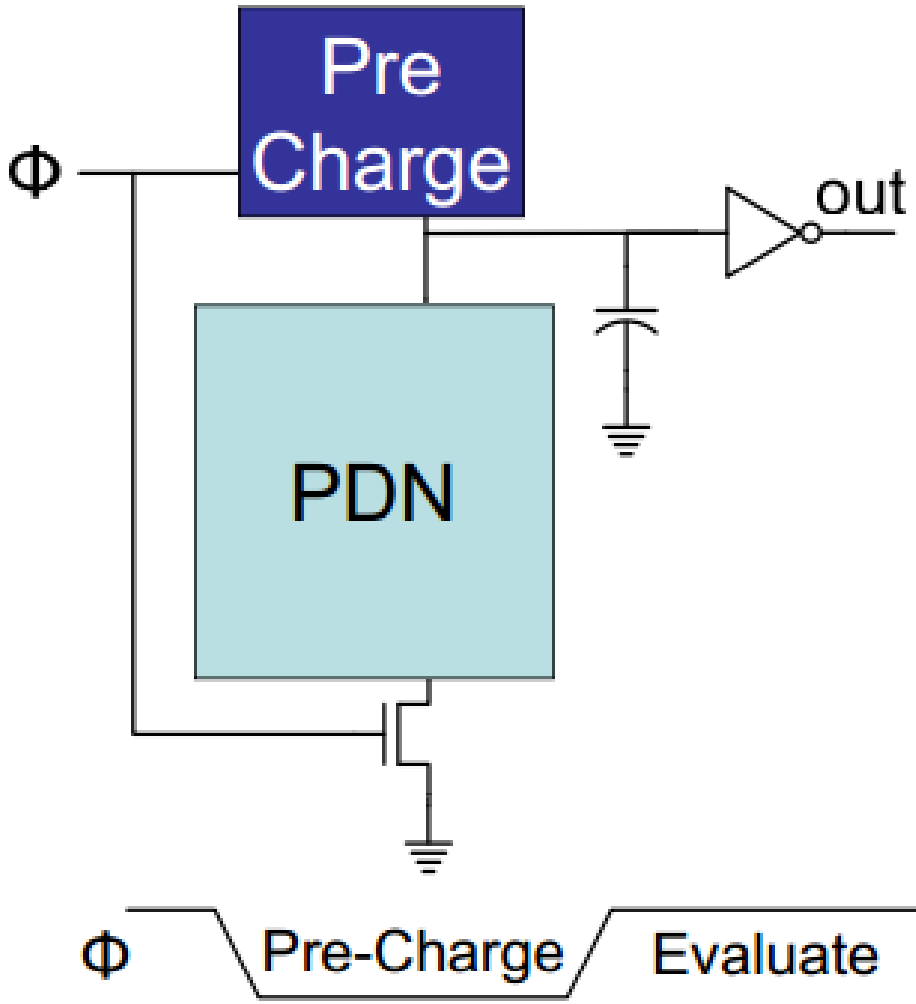
Pass Gate Logic



- Disadvantages:
  - Delay dependence on state
  - Cannot be cascaded without output inverter
  - Added leakage in output inverter

Dynamic Logic Families

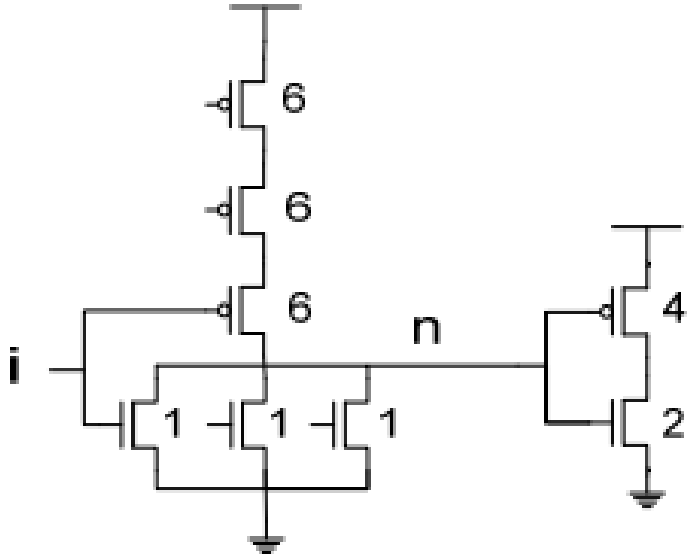
Basic Domino gate

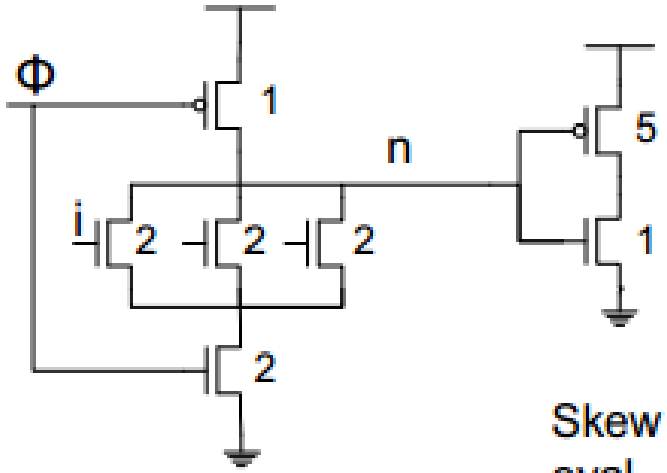


- Divide the clock in 2 phases:
  - Precharge
    - Output Low
    - Dyn. Cap precharge
    - PDN Off
  - Evaluate
    - Conditional discharge
    - Input must be stable and monotonic L→H

Domino / Static C_{in}/C_{out}

3-input OR gate



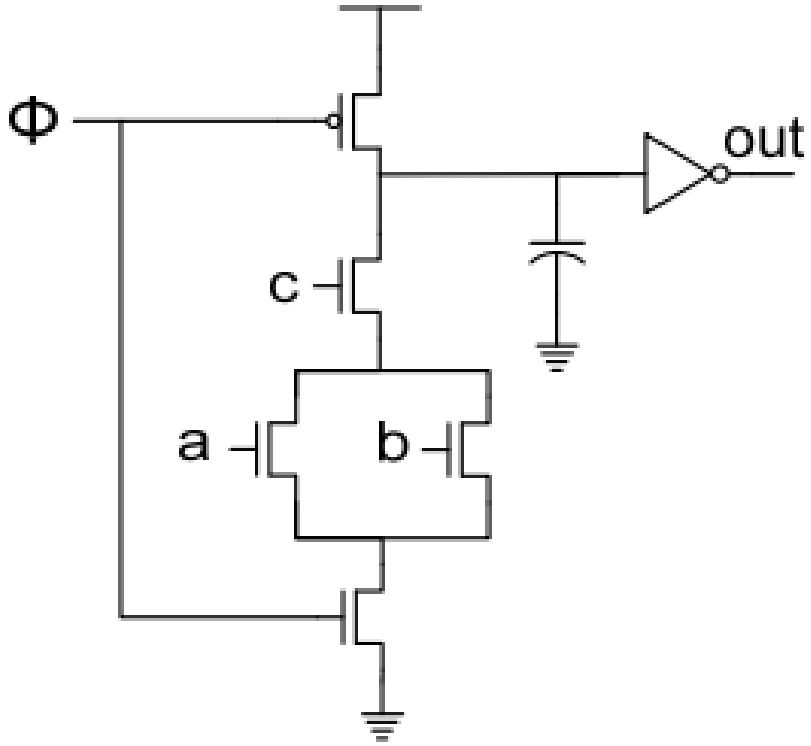


Skew for eval

Static:
$C_i = 7$
$C_n = 9$

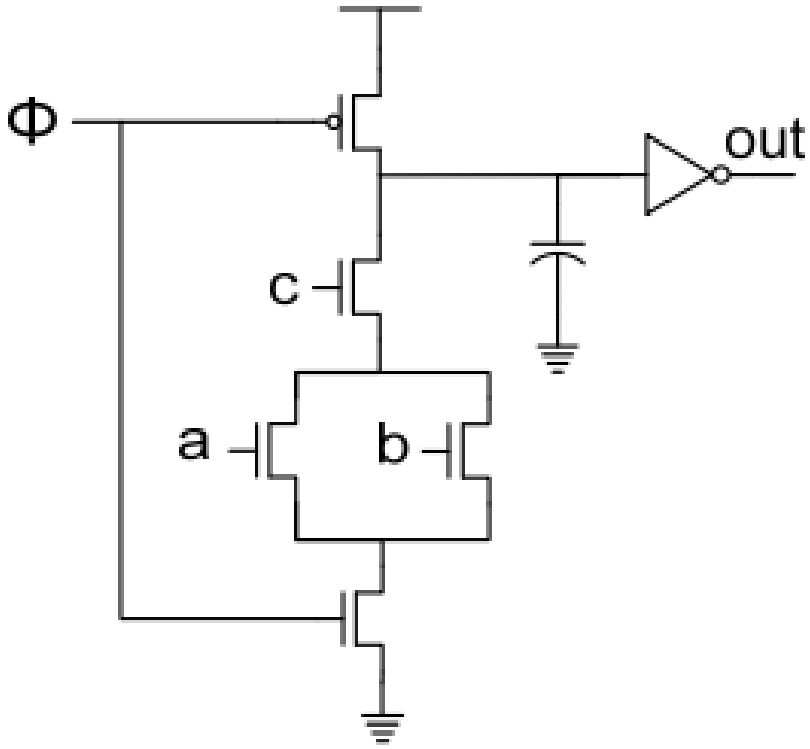
Dynamic:
$C_i = 2$
$C_n = 7$

Basic Domino gate



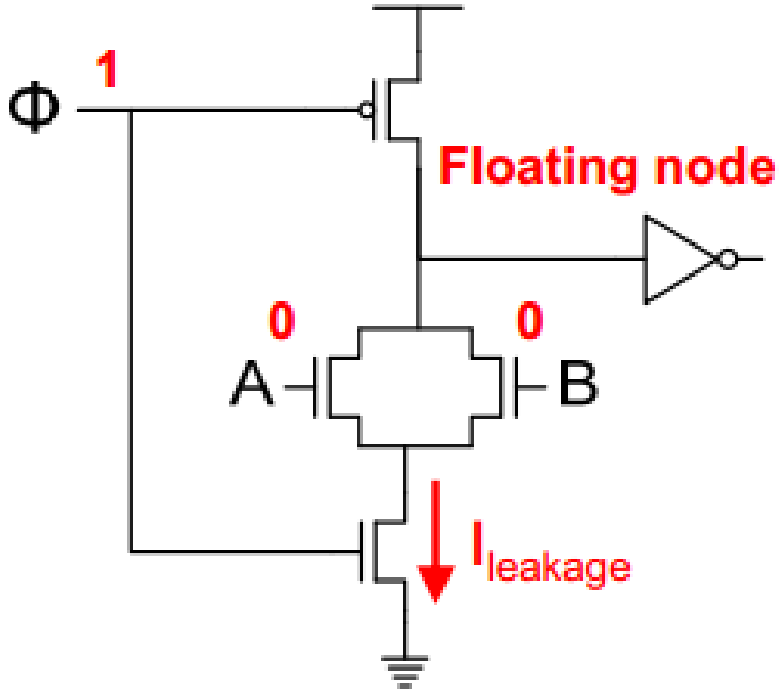
- Advantages:
  - Faster than CMOS
  - Input capacitance is lower
  - Early switch point
  - Inverter P/N > 2 (only rising delay important)

Basic Domino gate



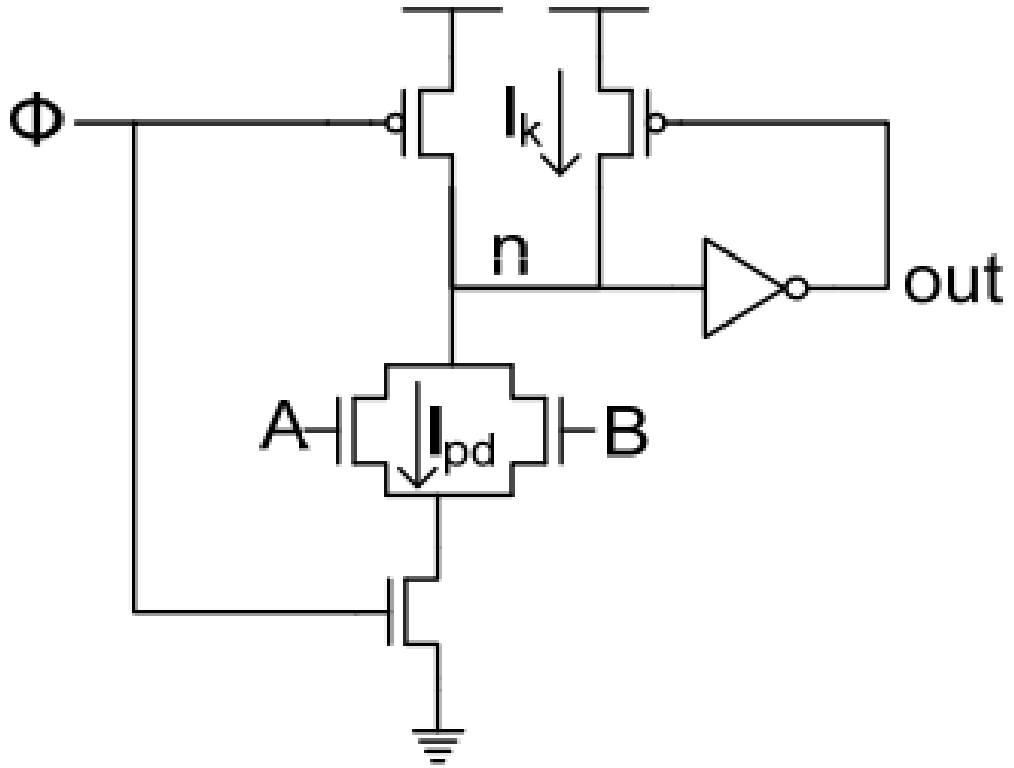
- Disadvantages:
  - Low noise margin
  - Charge sharing
  - Leakage currents
  - Internal capacitance charge sensitive to noise

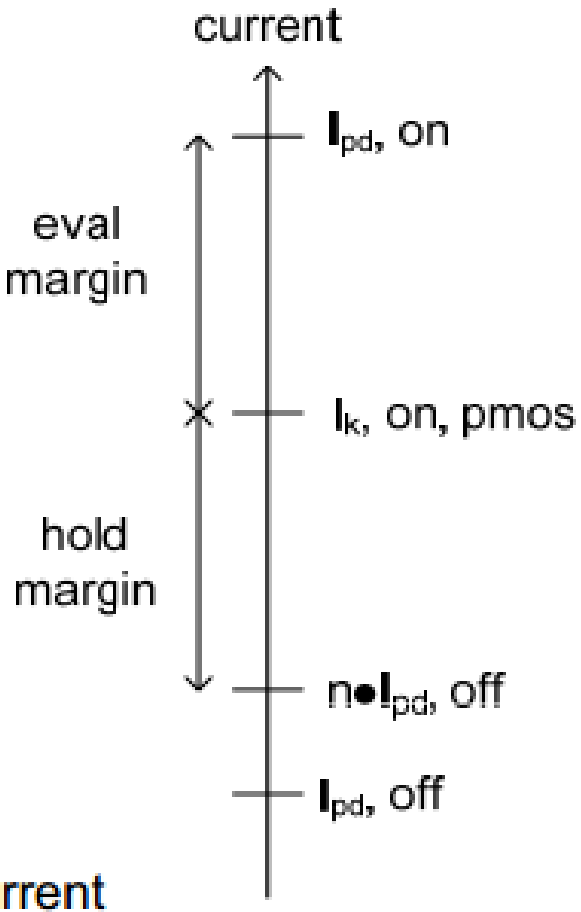
Issues: Leakage



- Dynamic node is floating during evaluation
  - Leakage current of NMOS can discharge it

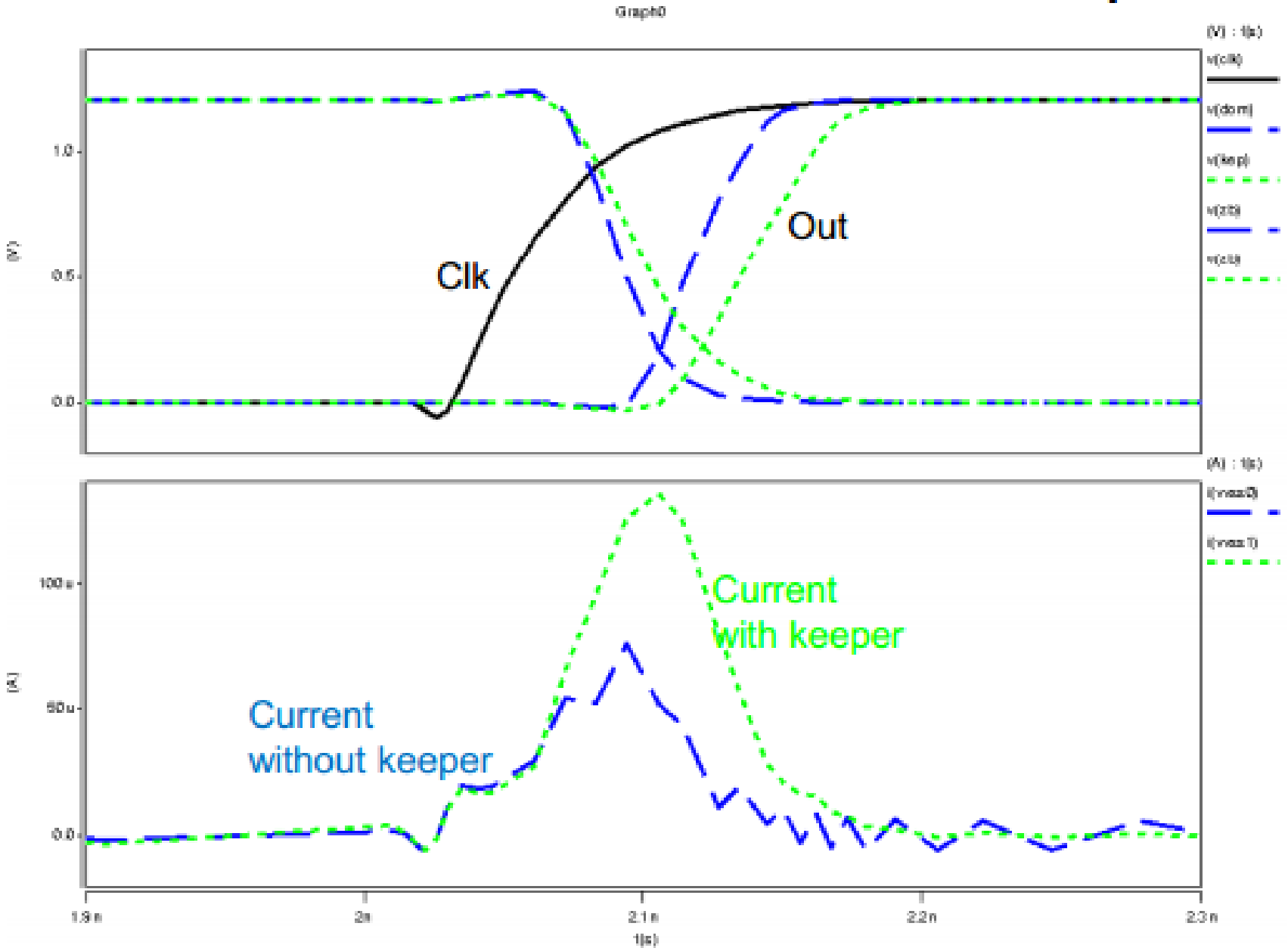
Issues: Leakage



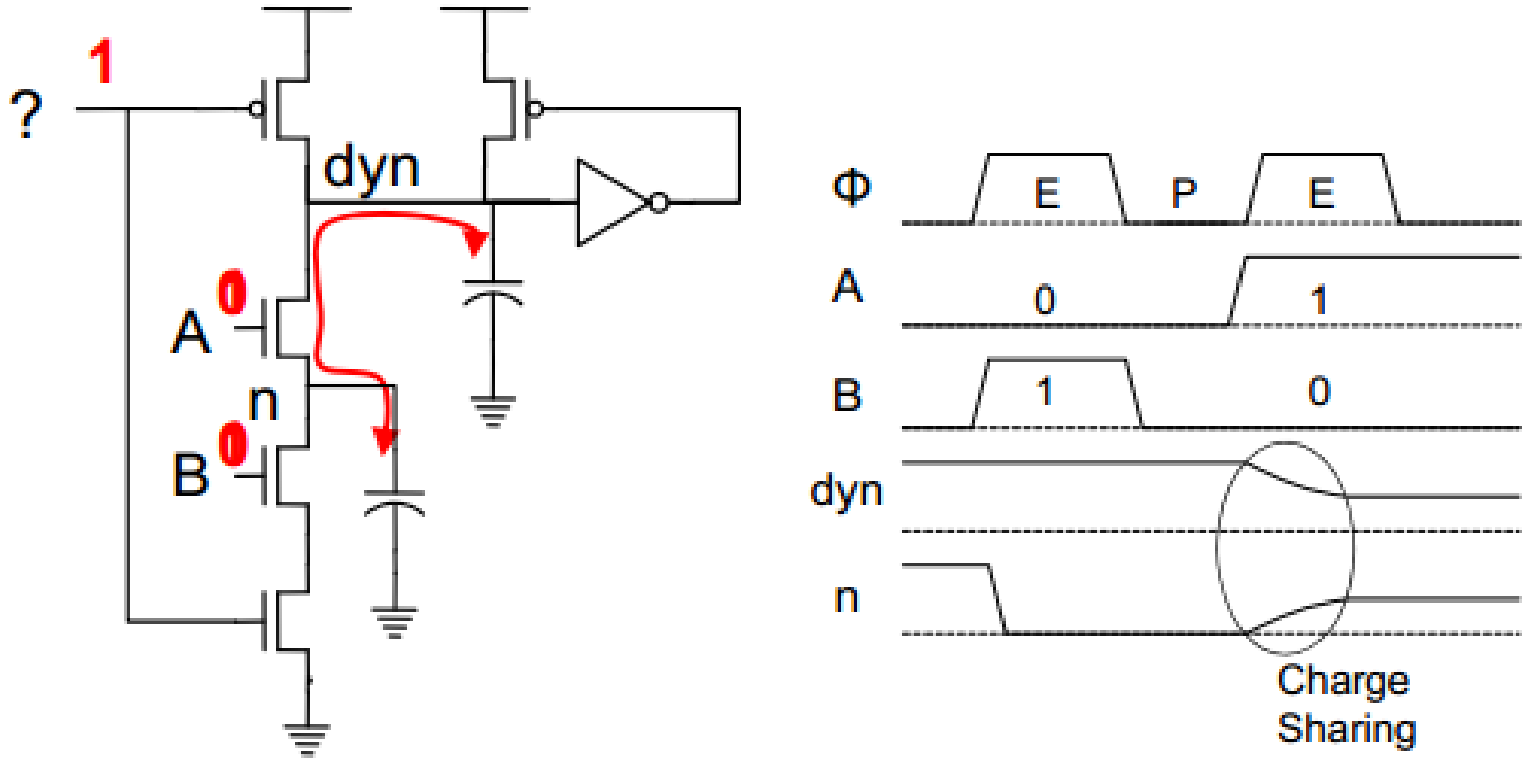


- Half latch devices:
  - Size PMOS to replenish the leakage current
  - Limits width OR gates

Domino – with and without keeper



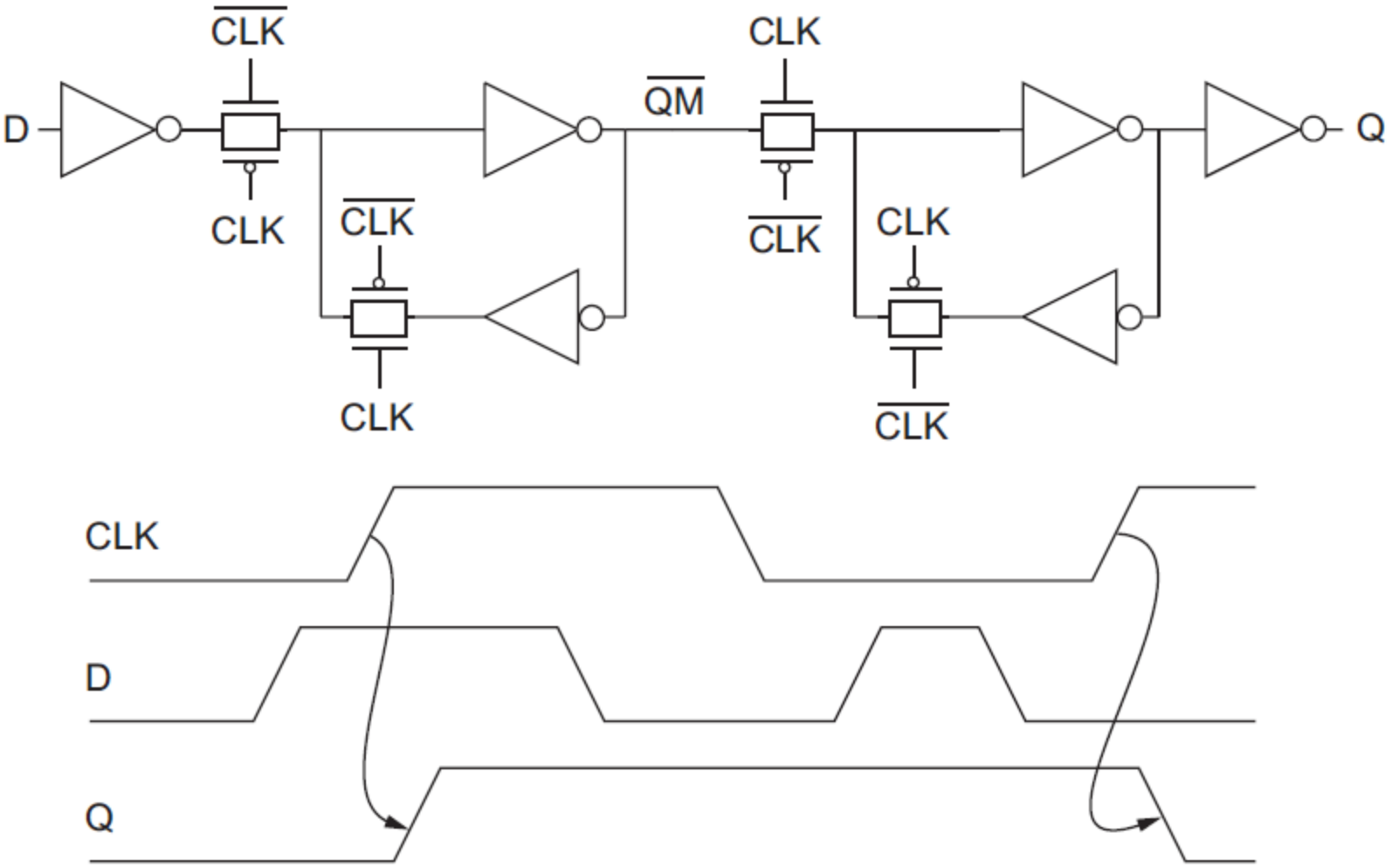
Issues: Charge sharing



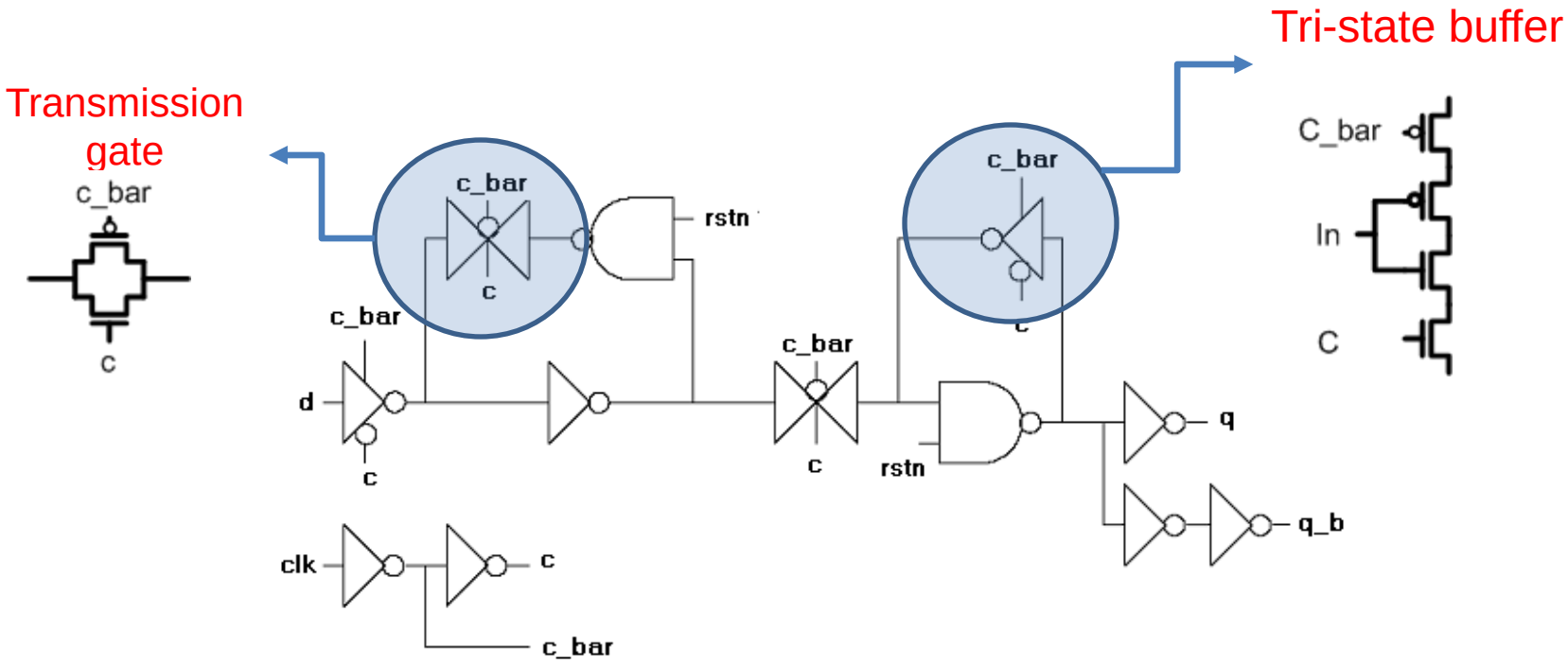
- In evaluate, dynamic node charge is shared with internal node caps
- Node was discharged in previous cycle

Sequential Logic

Flip-flop (Basics)



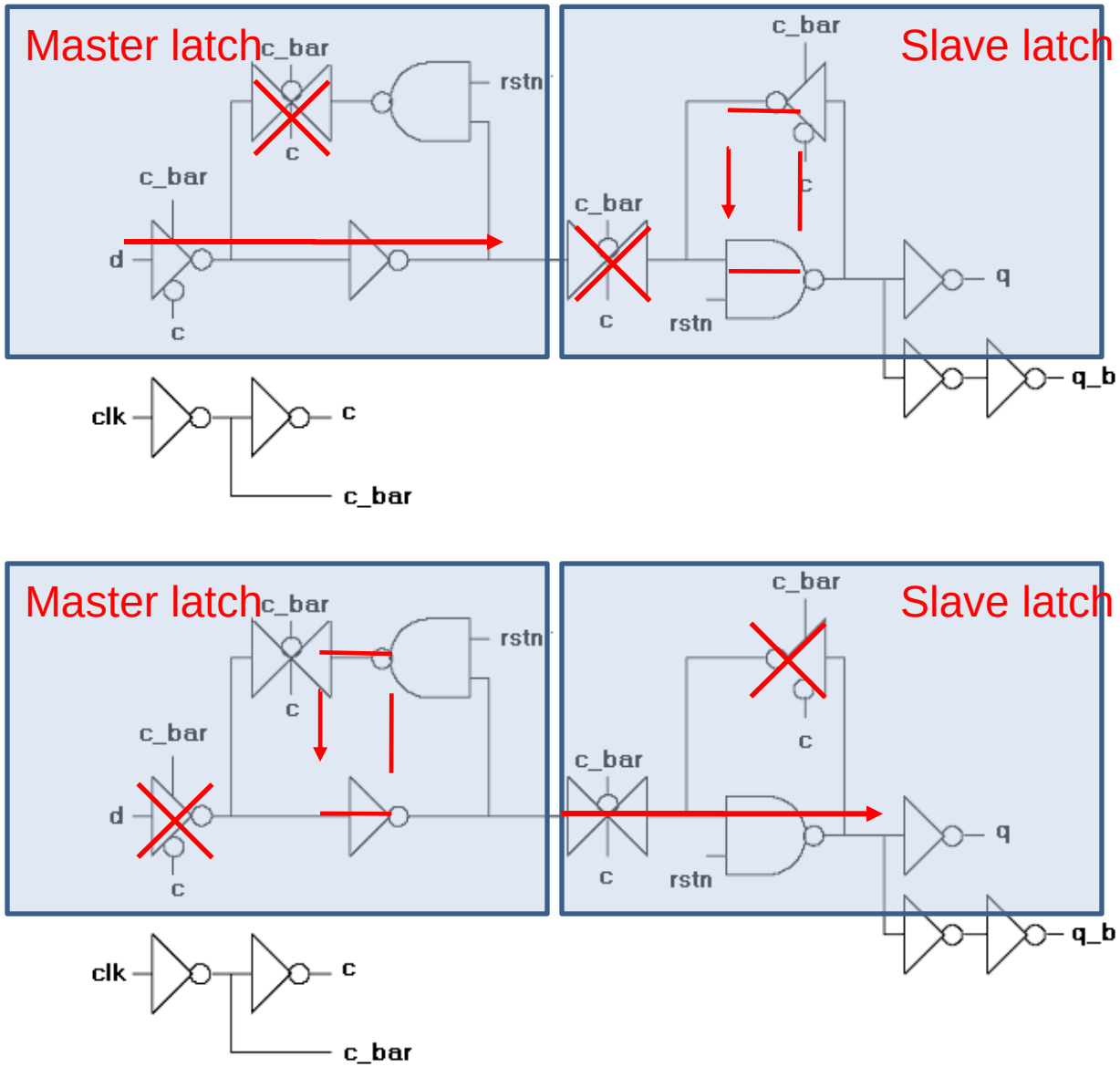
Flip-flop



- Flip Flop with Asynchronous Reset

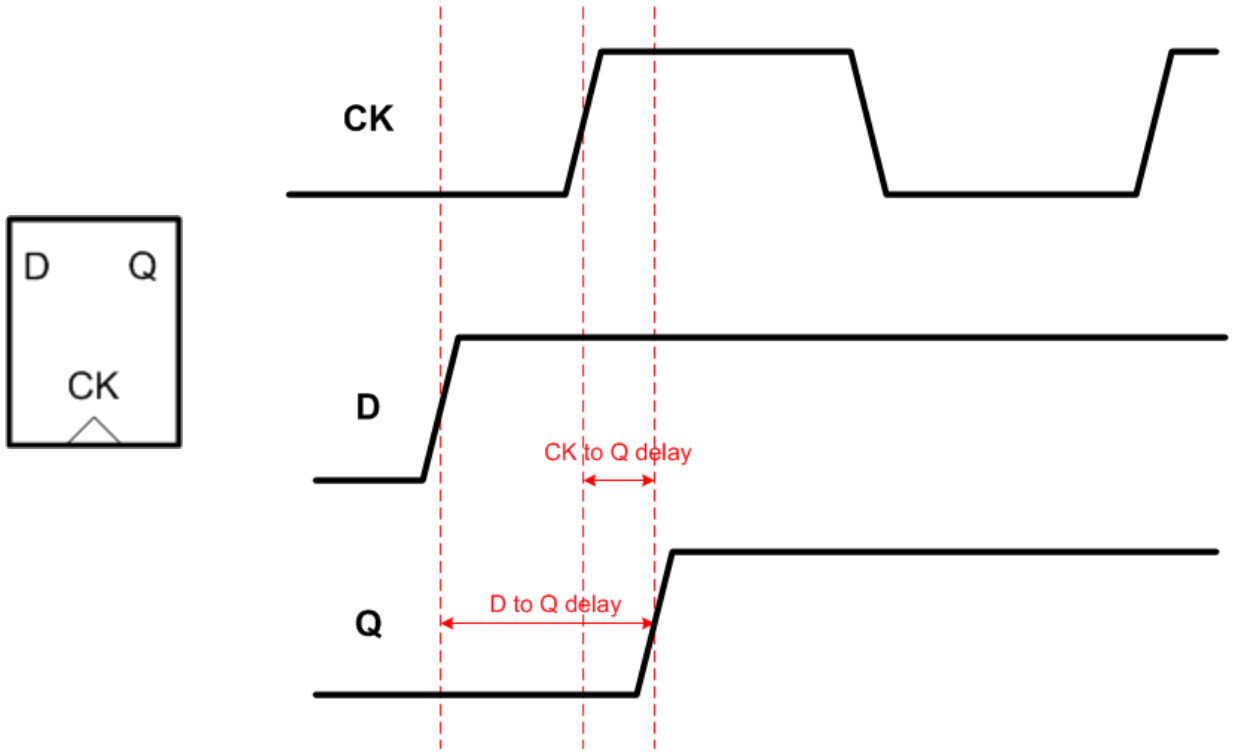
Flip-flop

- How it works
  - Divided flip flop into 2 latches (master and slave)
  - When master is transparent, slave holds.
  - When master holds, slave is transparent
  - Capture data at the rising edge of clock



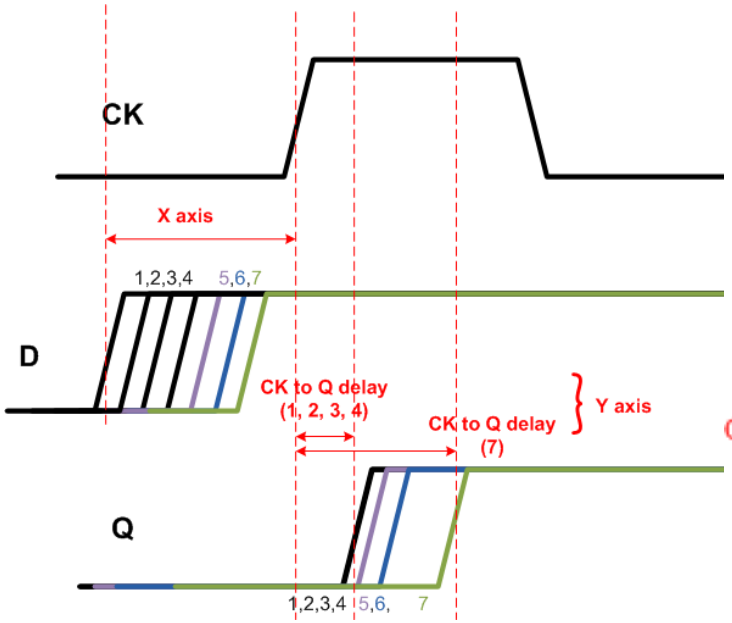
Flip-flop (continued)

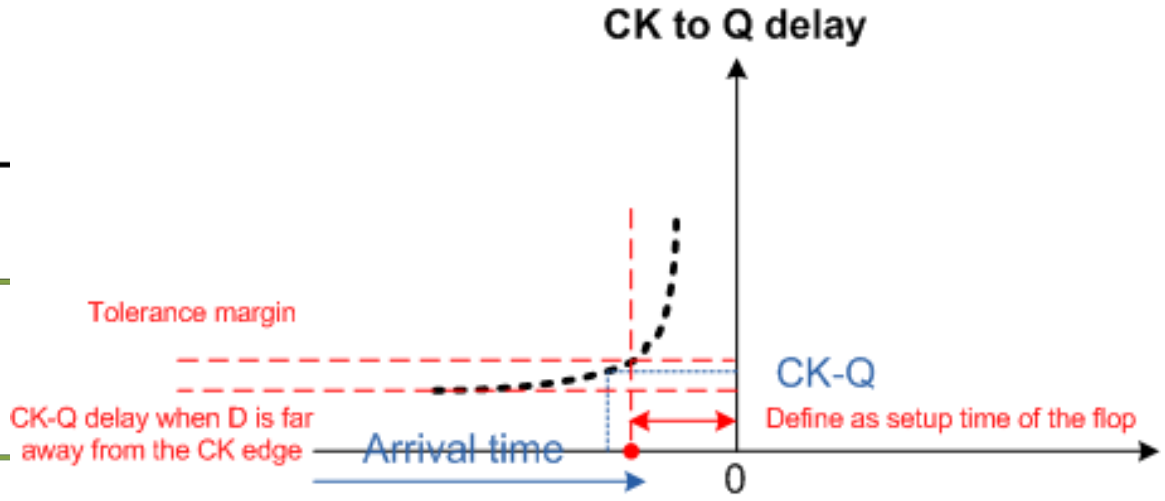
- Important terms : C-Q delay, D-Q delay



Flip-flop (continued)

- Setup Time
  - As D approaches to CK edge, C-Q delay goes up



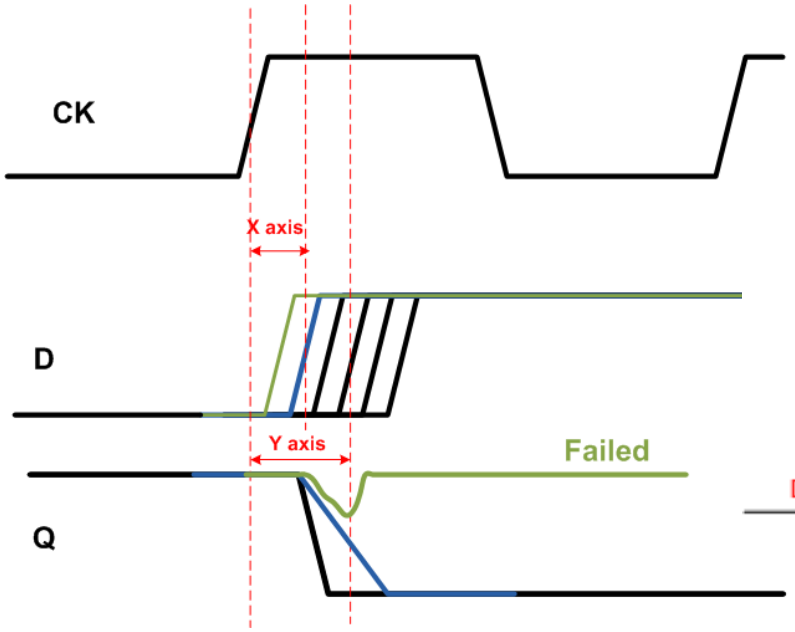


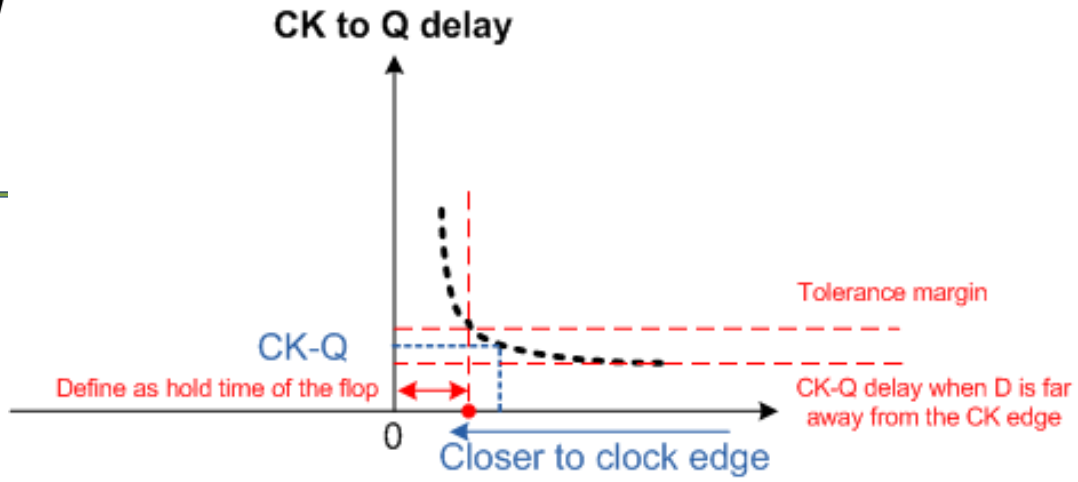
When D arrives after the setup time point, we call it setup time violation

Setup-Time : Point at which CLK-Q delay rises 5% beyond nominal

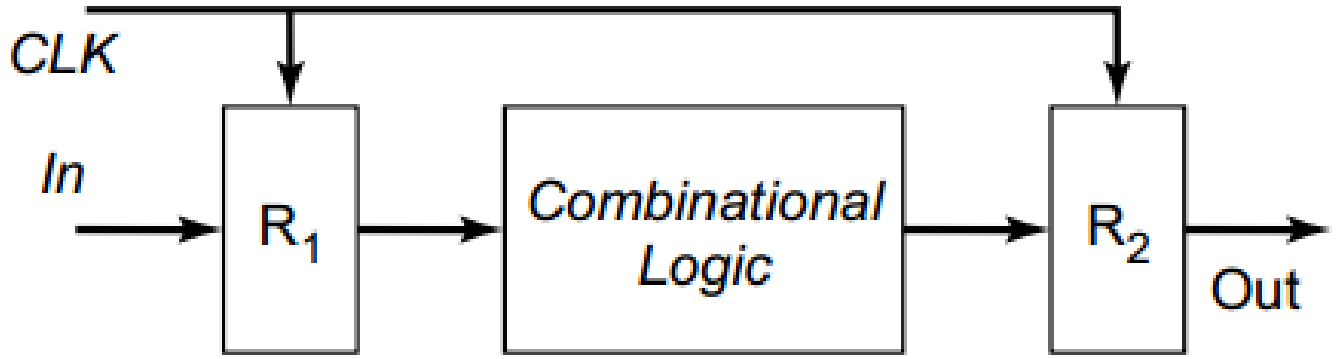
Flip-flop (continued)

- Hold Time
  - Input should be stable for a period of time after the clk edge

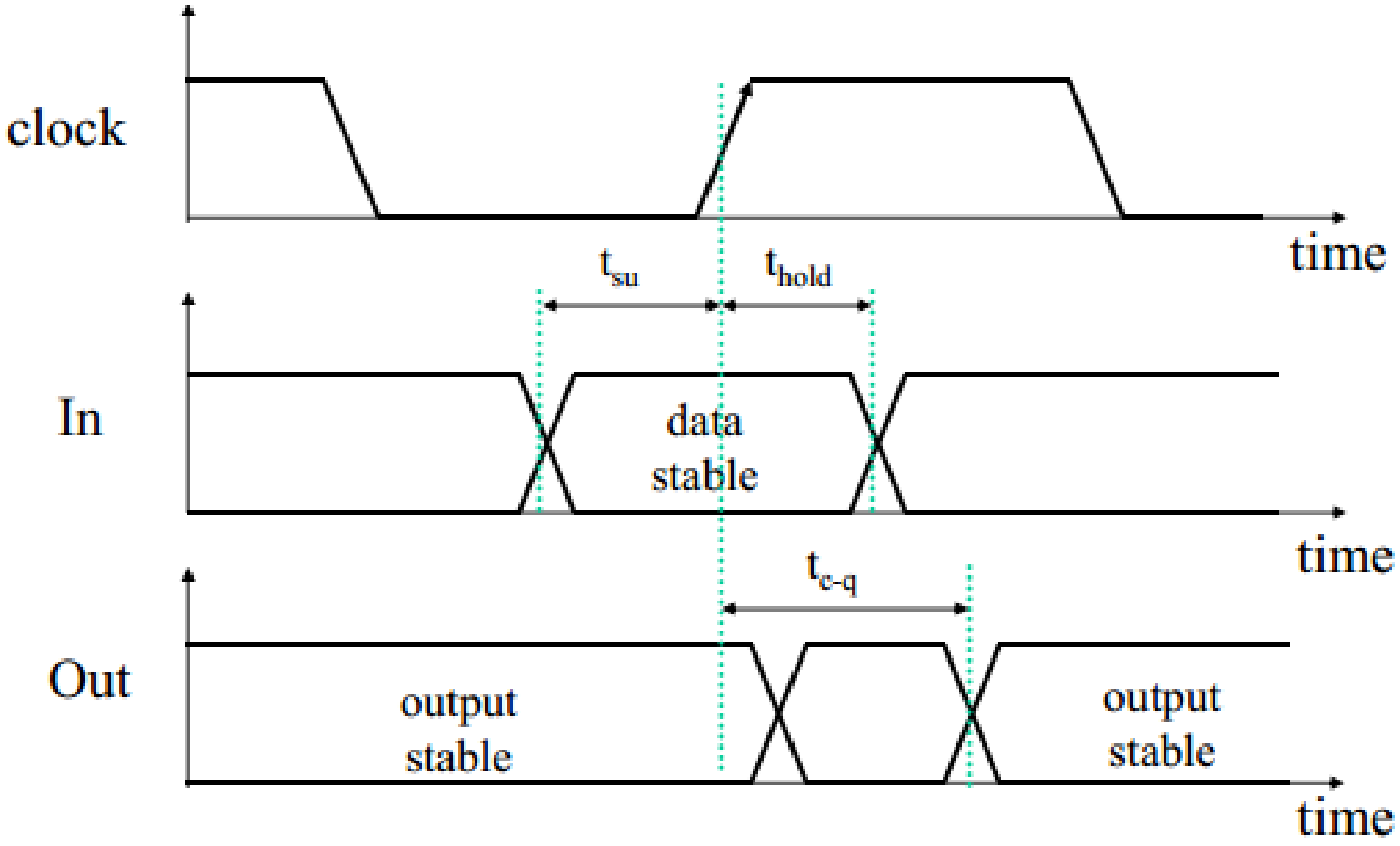




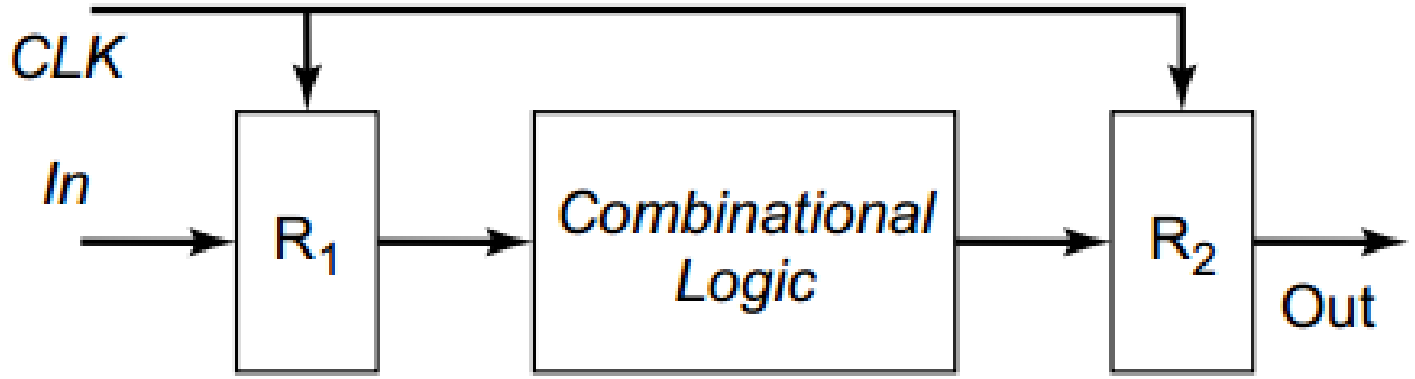
Synchronous Timing



Timing Metrics



Synchronous Timing



$$T_{c\text{-}q} + t_{plogic,min} \geq t_{hold}$$

$$T \geq t_{c\text{-}q} + t_{plogic,max} + t_{su}$$

SRAM & DRAM

- Office Hour

Review 1

- MOSFET Transistor
- CMOS Gate
- Power
- Diode Behavior and equation
- Transistor Behavior and equation
- RC Delay
- Capacitance
- Size Single Gate

Review 2

- Logic Effort
- Static Logic Family
- Dynamic Logic Family
- Sequential Logic
- Synchronous Timing
- SRAM & DRAM