EECS 312 Discussion 2

09/13

Shengshuo Lu

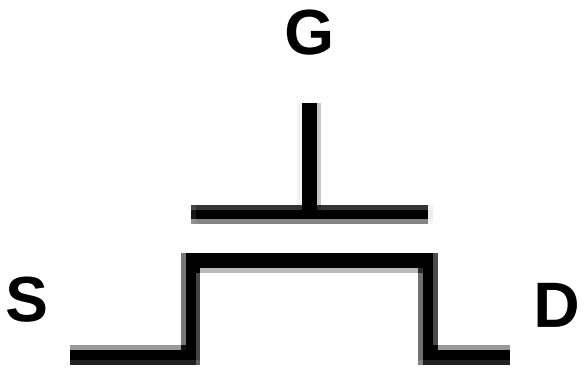
(luss@umich.edu)

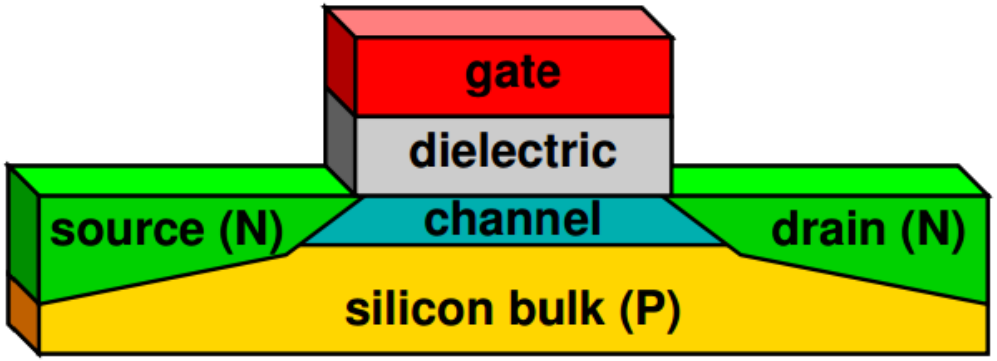
Overview

- Reminder
  - Lab 1: Due Sep 17
  - Special Topics Sign up sheet
  - VNC

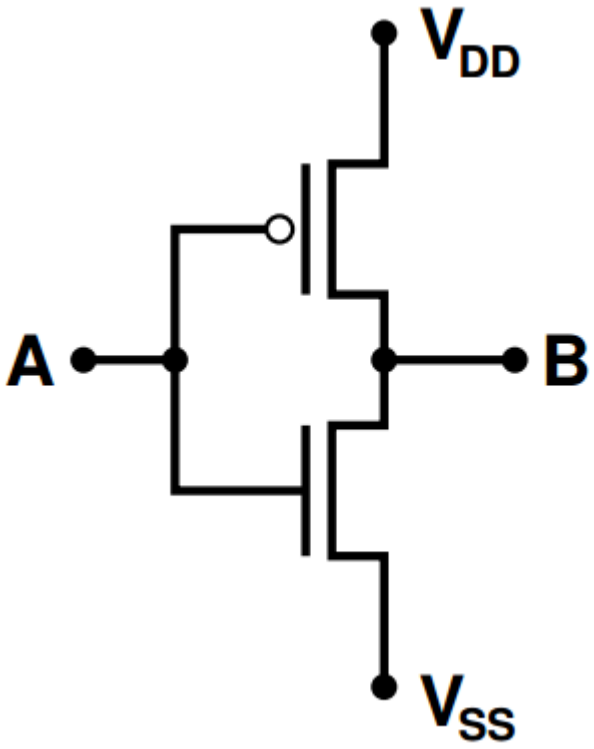
- Logic Gates
- Power
- Diode

NMOS





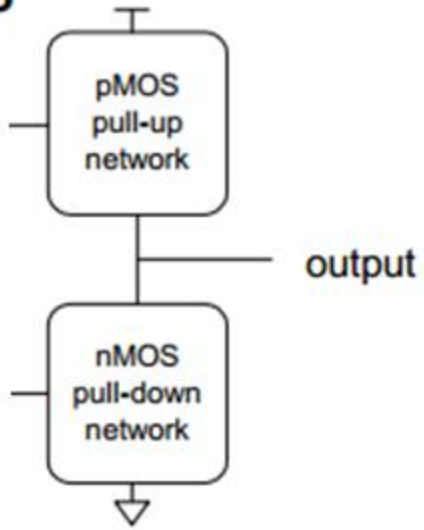
Logic Gates



Inverter

Complementary CMOS

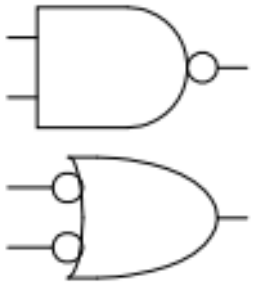
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - Also called static CMOS

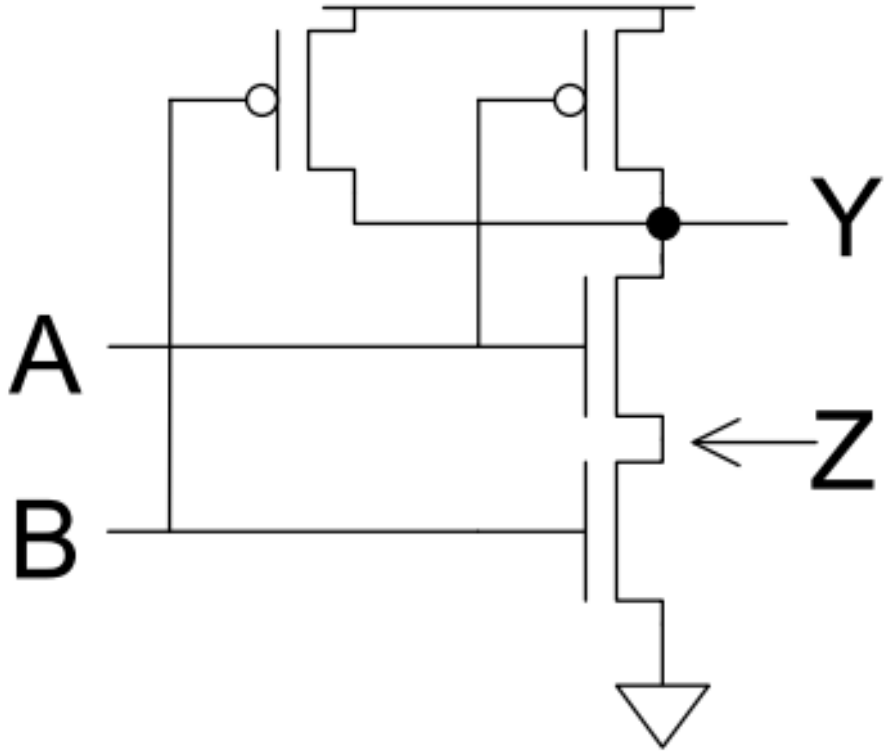


	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

CMOS NAND Gate

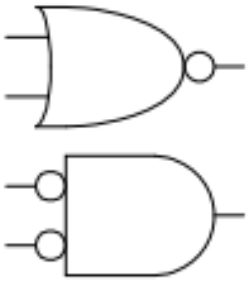
A	B	Y	Z
0	0	1	~100mV
0	1	1	0
1	0	1	VDD-Vth
1	1	0	0

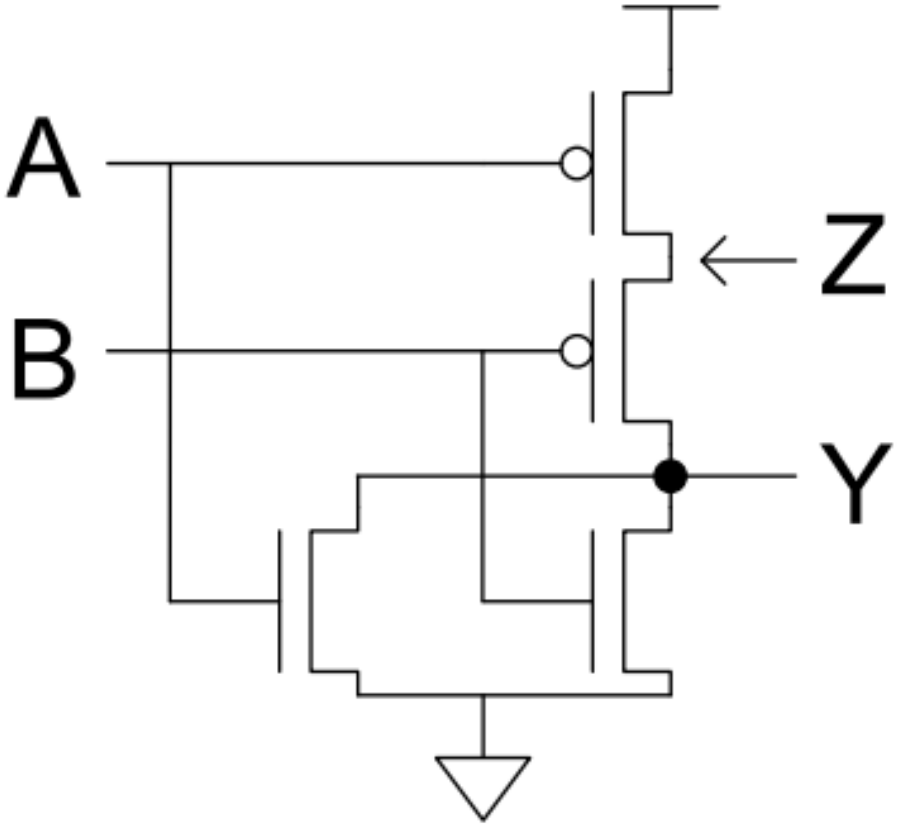




CMOS NOR Gate

A	B	Y	Z
0	0	1	1
0	1	0	1
1	0	0	Vth
1	1	0	~VDD-100mV

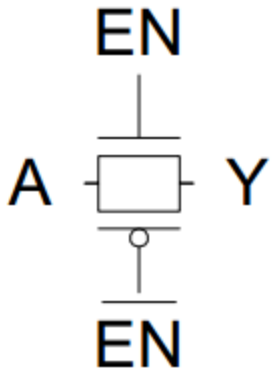


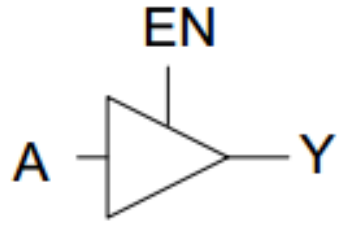


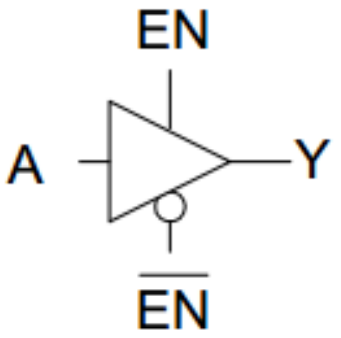
Tristates

- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

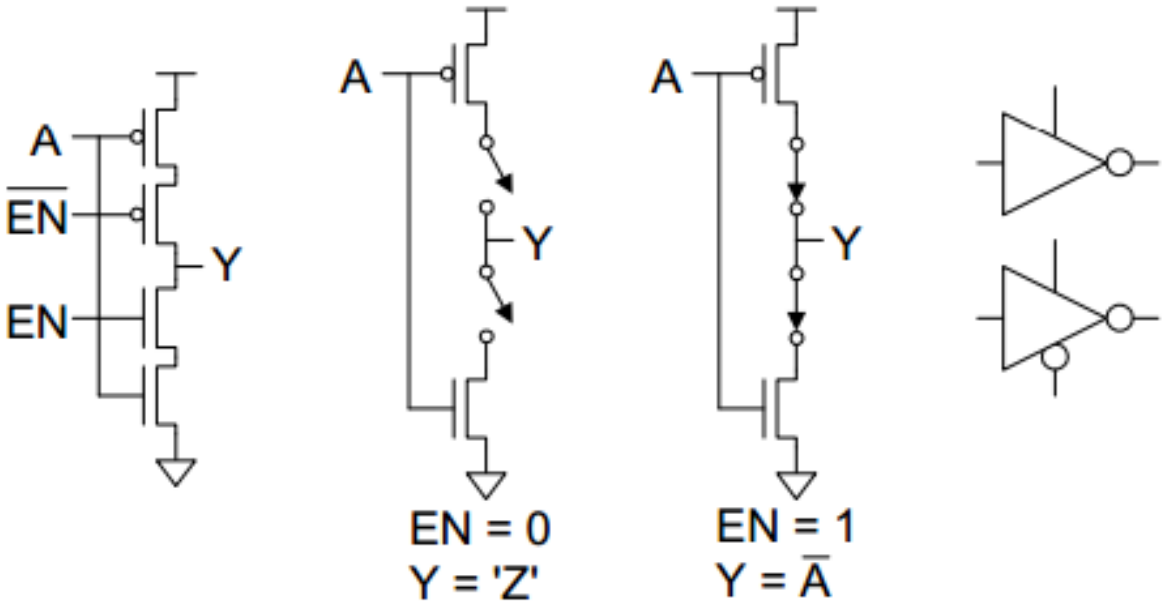






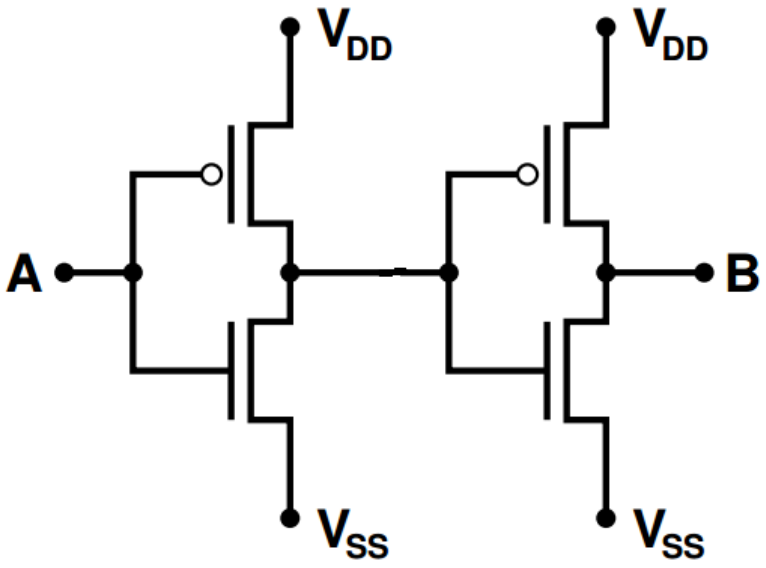
Tristate Inverter

- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output



Power

- Dynamic Power
- Static Power
- Short-Circuit Power *



Power

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot {V_{DD}}^2 \cdot f \cdot A$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance

V_{DD} : high voltage

f : switching frequency

A : switching activity

b : MOS transistor gain

V_T : threshold voltage

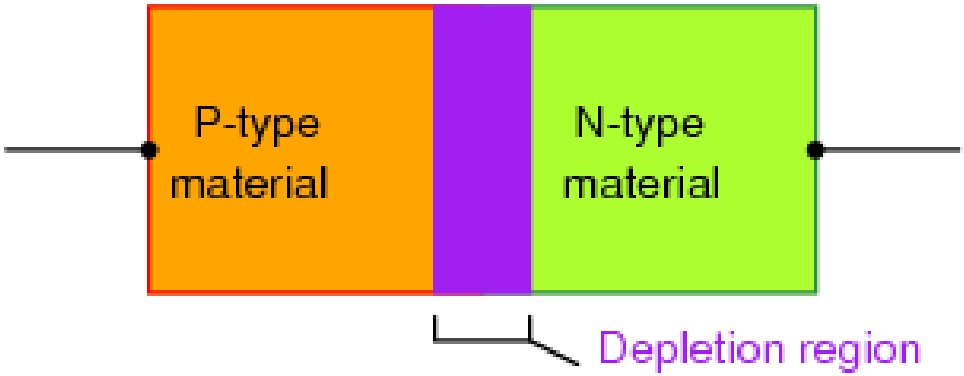
t : rise/fall time of inputs

$\dagger\ P_{SHORT}$ usually $\leq 10\%$ of P_{SWITCH}

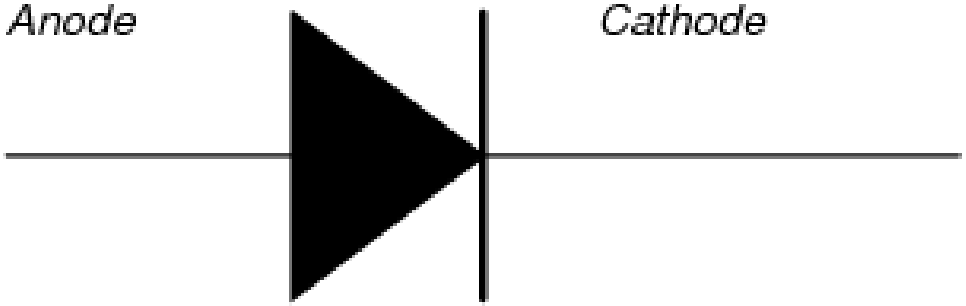
Smaller as $V_{DD} \rightarrow V_T$

$A < 0.5$ for combinational nodes, 1 for clocked nodes.

Diode

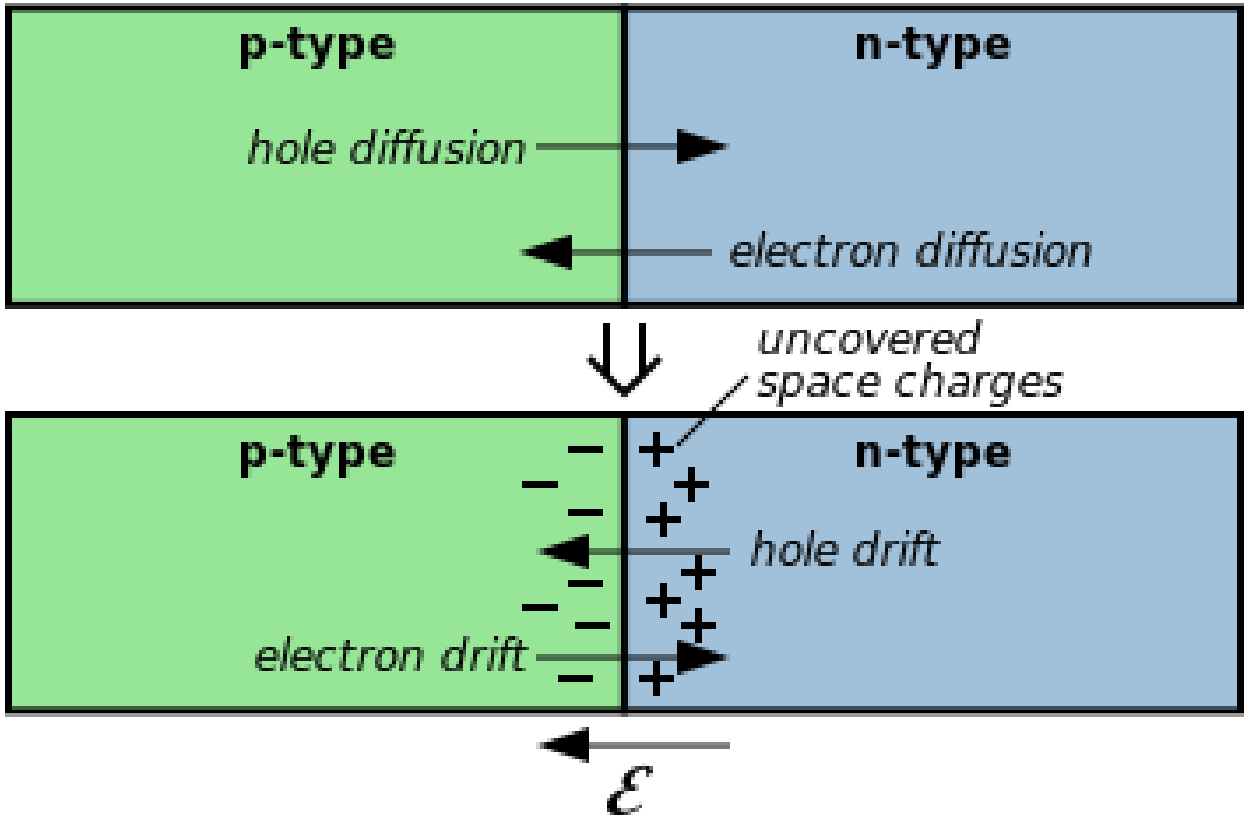


P-N junction representation



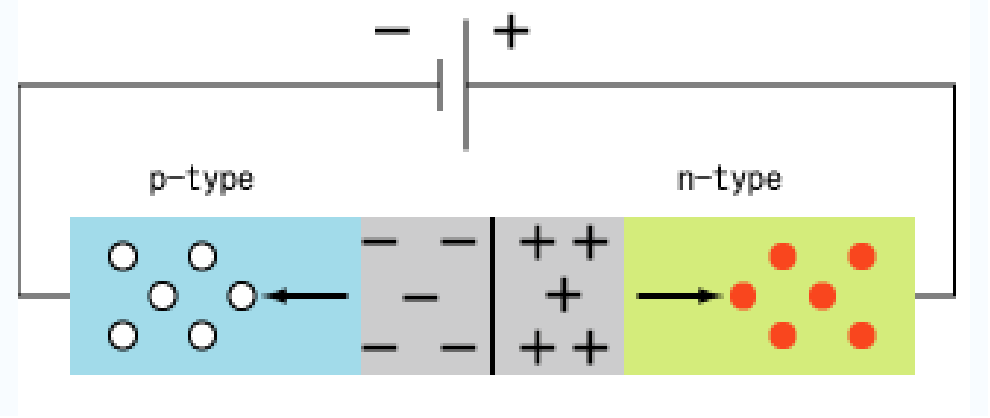
Schematic symbol

Diode

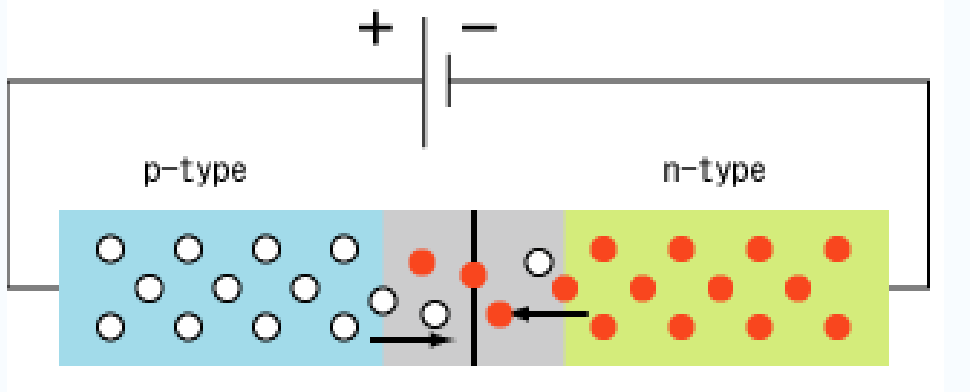

p-type
n-type
hole diffusion
electron diffusion
uncovered
space charges
p-type
n-type
hole drift
electron drift
ε

Diode

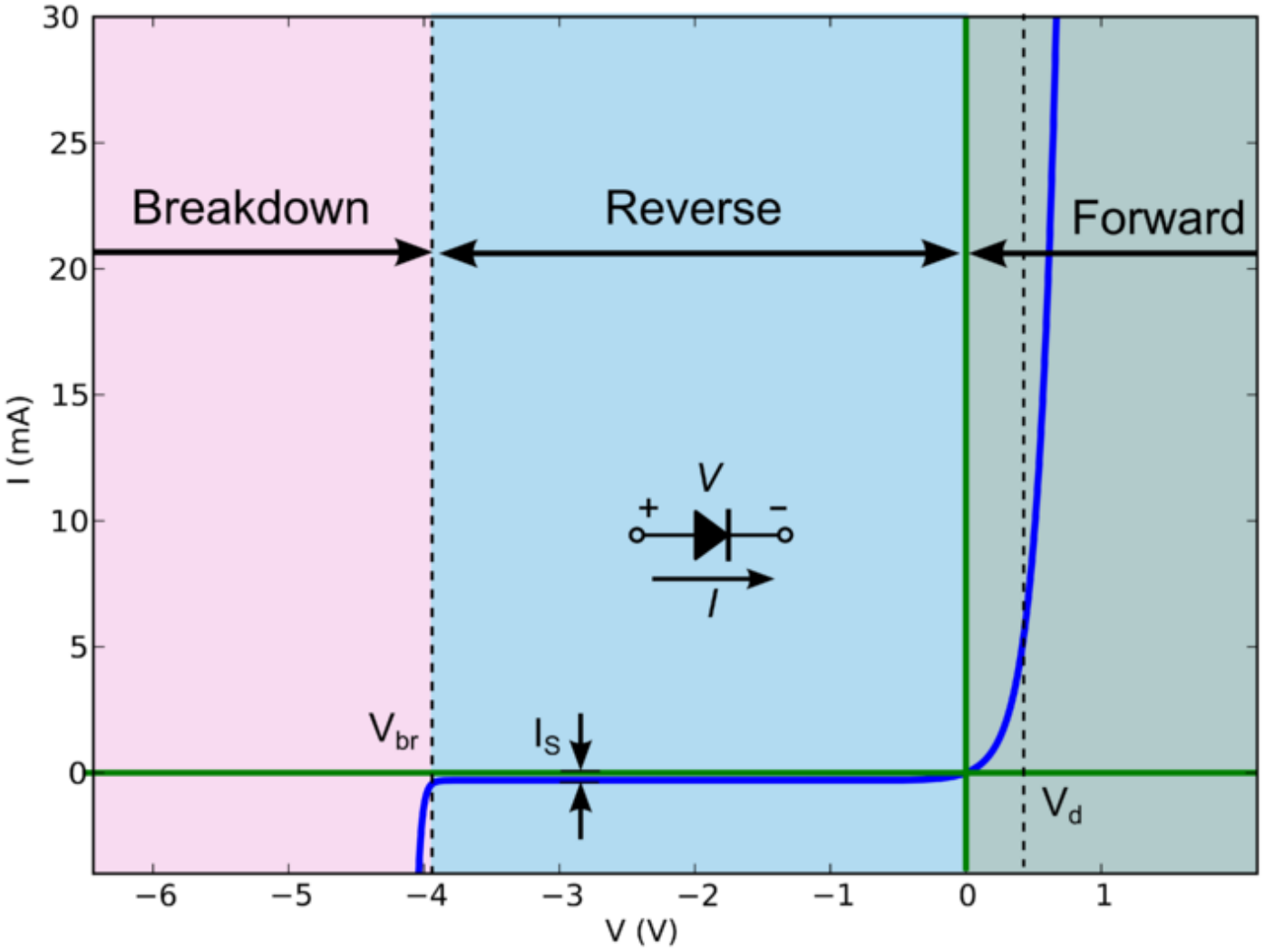
- Reverse Bias



- Forward Bias



Diode


Breakdown
Reverse
Forward
I (mA)
V (V)
30
25
20
15
10
5
0
−6
−5
−4
−3
−2
−1
0
1
V
+
−
I
V_{br}
I_S
V_d