EECS 312 Discussion 3

09/20

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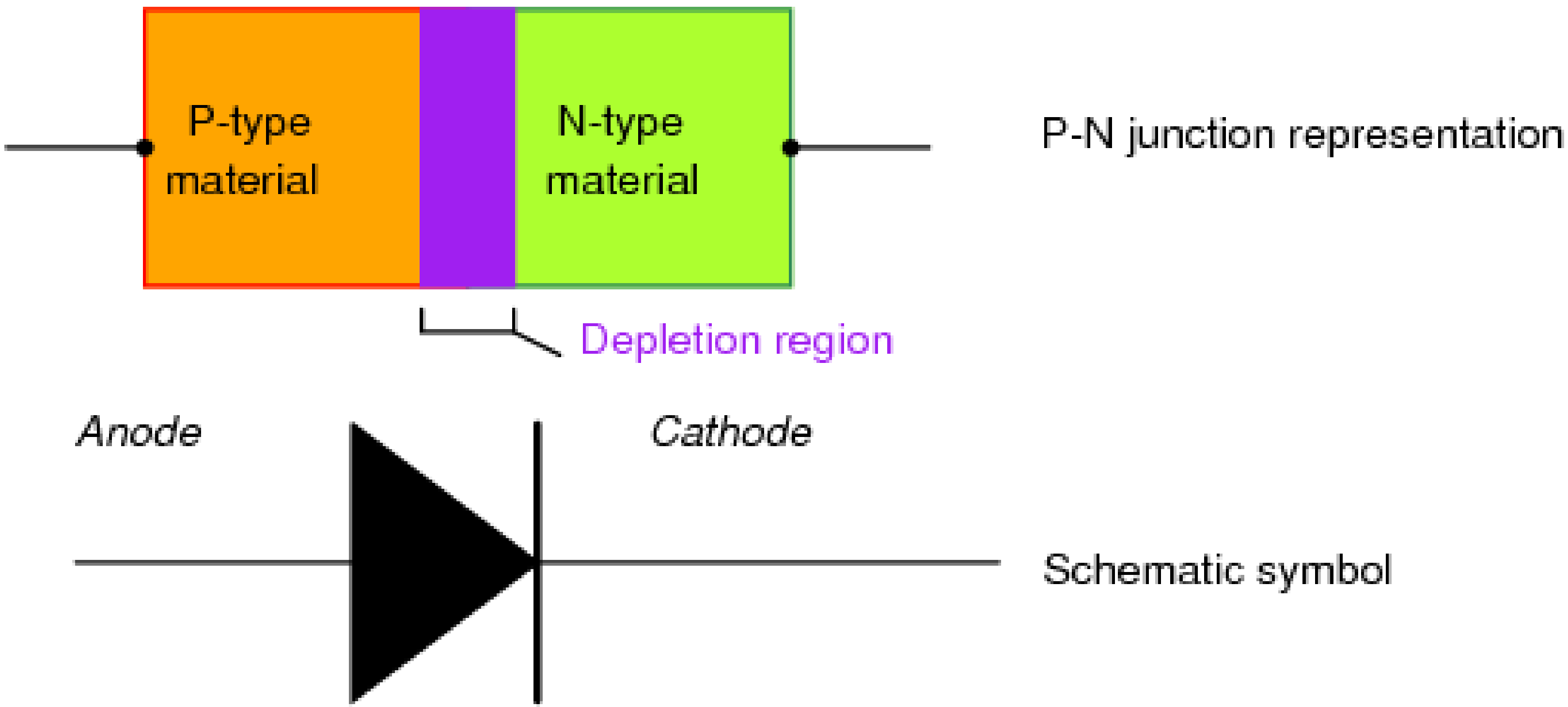
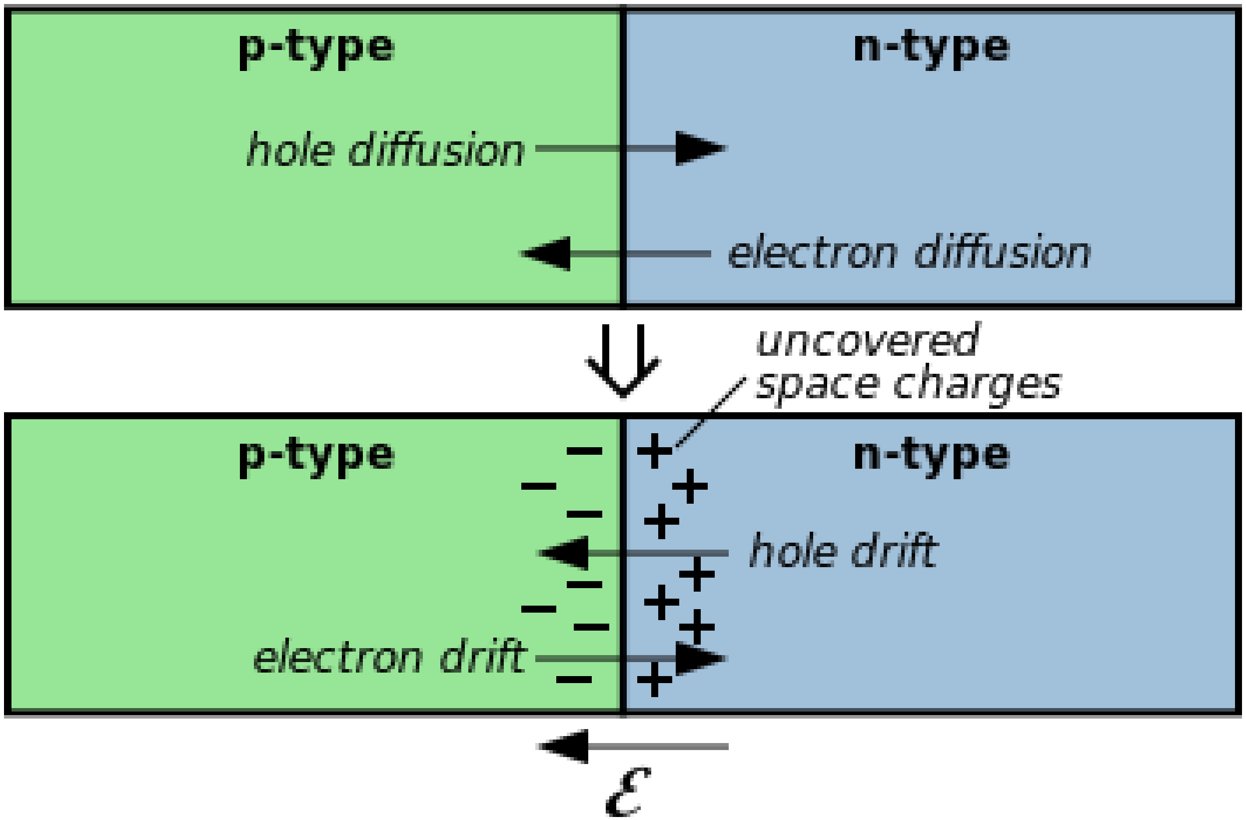
Overview

- Reminder
  - HW 1: Due Sep 24
- Diode
- Transistors

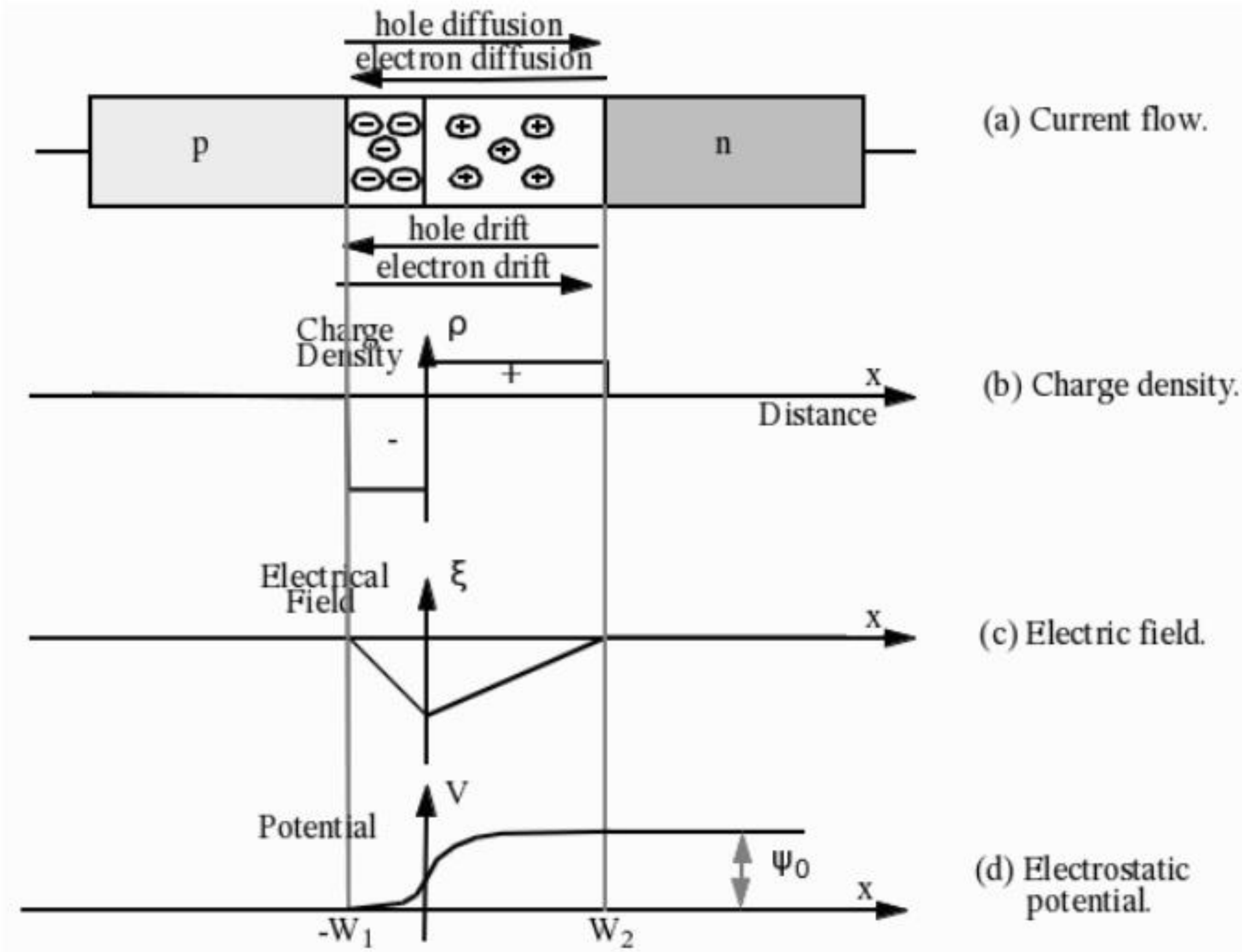
Diode


P-type
material
N-type
material
P-N junction representation
Depletion region
Anode
Cathode
Schematic symbol

Diode


p-type
n-type
hole diffusion
electron diffusion
uncovered
space charges
p-type
n-type
hole drift
electron drift
$\mathcal{E}$

Diode



hole diffusion
electron diffusion
p
n
hole drift
electron drift
(a) Current flow.
Charge Density
ρ
+
-
x
Distance
(b) Charge density.
Electrical Field
ξ
x
(c) Electric field.
V
Potential
ψ0
x
-W1
W2
(d) Electrostatic potential.

Built-in Potential
Depletion Region Width

$$\Phi_0 = \Phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

$$\Phi_T = \frac{kT}{q}$$

$$W \approx \left[\frac{2\epsilon_r\epsilon_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\Phi_0\right]^{\frac{1}{2}}$$

- n_i: intrinsic charge carrier concentration.
- N_x: acceptor and donor concentrations.
- k: Boltzmann constant
- T: temperature
- q: elementary charge

Diode Current

$$I_D = I_S \left(e^{\frac{V_D}{\phi_T}} - 1 \right)$$

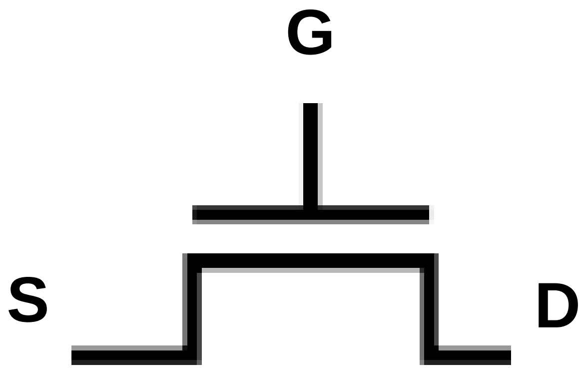
- I_D: diode current
- V_D: diode voltage
- I_S: saturation current constant
- $\phi_T = \frac{kT}{q}$: thermal voltage
  - k: Boltzmann constant
  - T: temperature
  - q: elementary charge

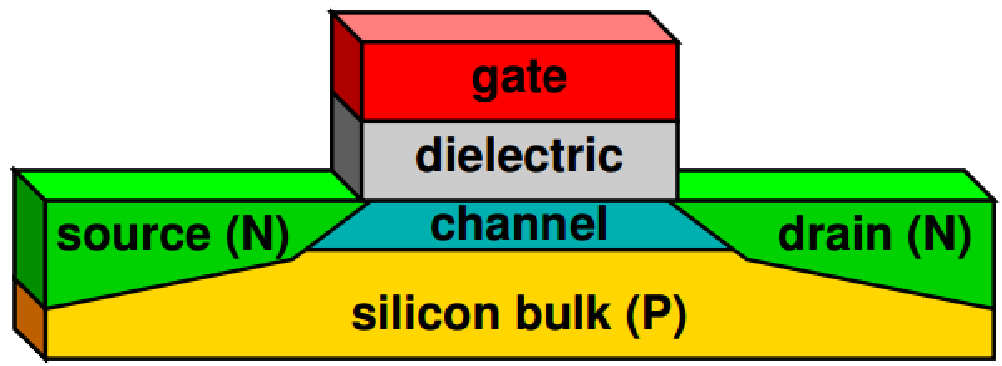
Diffusion capacitance

$$C_{J0} = A_D \sqrt{\frac{\epsilon_{Si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{\phi_0}}$$

- A_D: area of diode
- ϵ_{Si}: permittivity of silicon
- N_X: carrier density
- $\phi_0 = \phi_T \ln \frac{N_A N_D}{n_i{}^2}$
  - $\phi_T = \frac{kT}{q}$
  - n_i: intrinsic carrier concentration

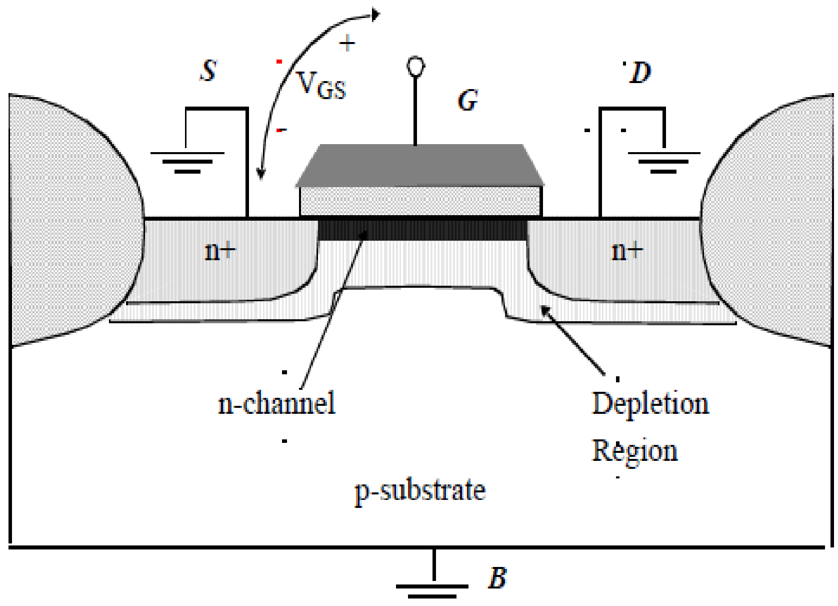
NMOS



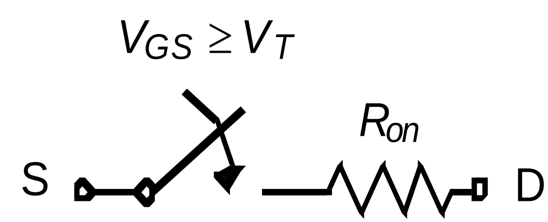


Threshold Voltage

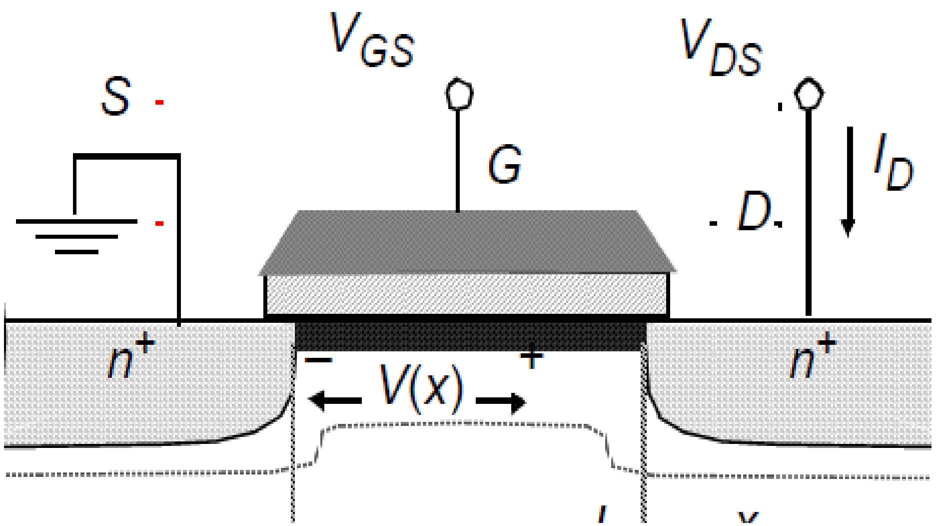
- $0 < V_{GS} < V_T$
  - Repel mobile holes and accumulation of electron beneath the gate oxide



- $V_{GS} > V_T$
  - Surface is as strongly n-type as the substrate is p-type



Operation Regions – Linear (lab 2)



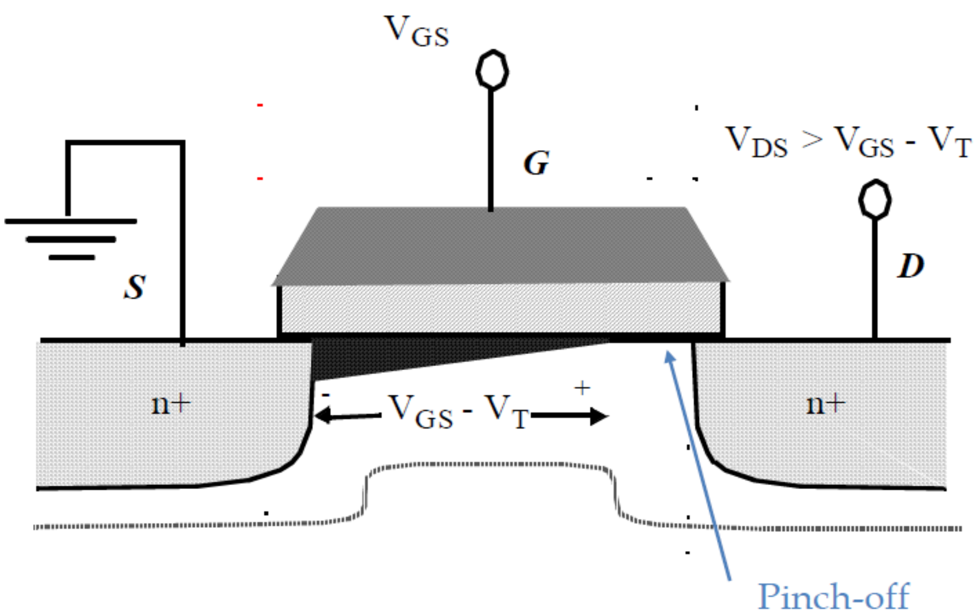
1. $V_{GS} > V_T$
2. $V_{GS} - V_T > V_{DS}$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

3. Linear contribution of V_{GT} to I_D
4. $k'_n = \mu_n C_{ox}$

In case of a P-type MOSFET, the inequalities used above should be directed opposite

Operation Regions – Saturation (lab 2)



1. $V_{GS} > V_T$
2. $V_{GS} - V_T \leq V_{DS}$

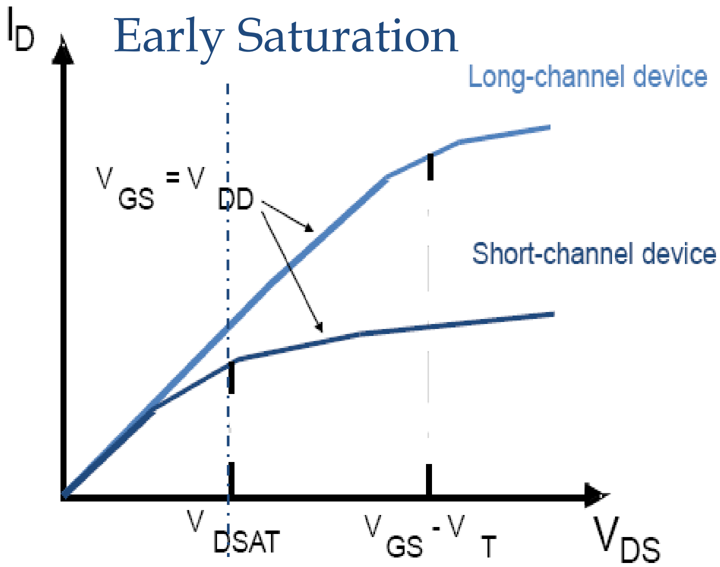
$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

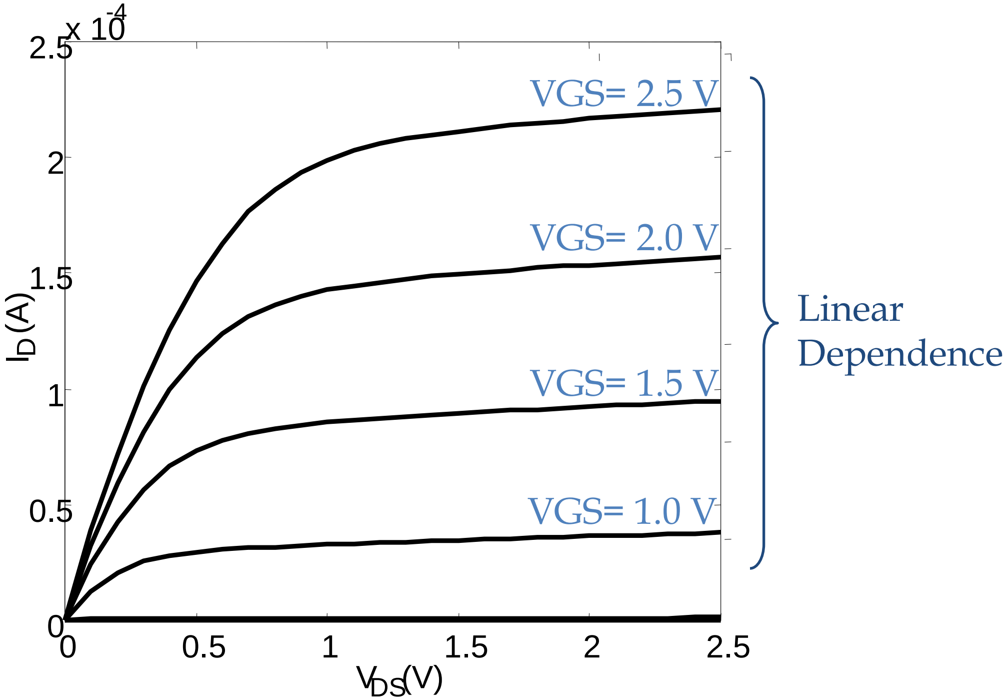
3. Quadratic contribution of V_{GT} to I_D
4. λ channel-length modulation parameter

In case of a P-type MOSFET, the inequalities used above should be directed opposite

Operation Regions – Velocity Saturated

Short Channel Effects

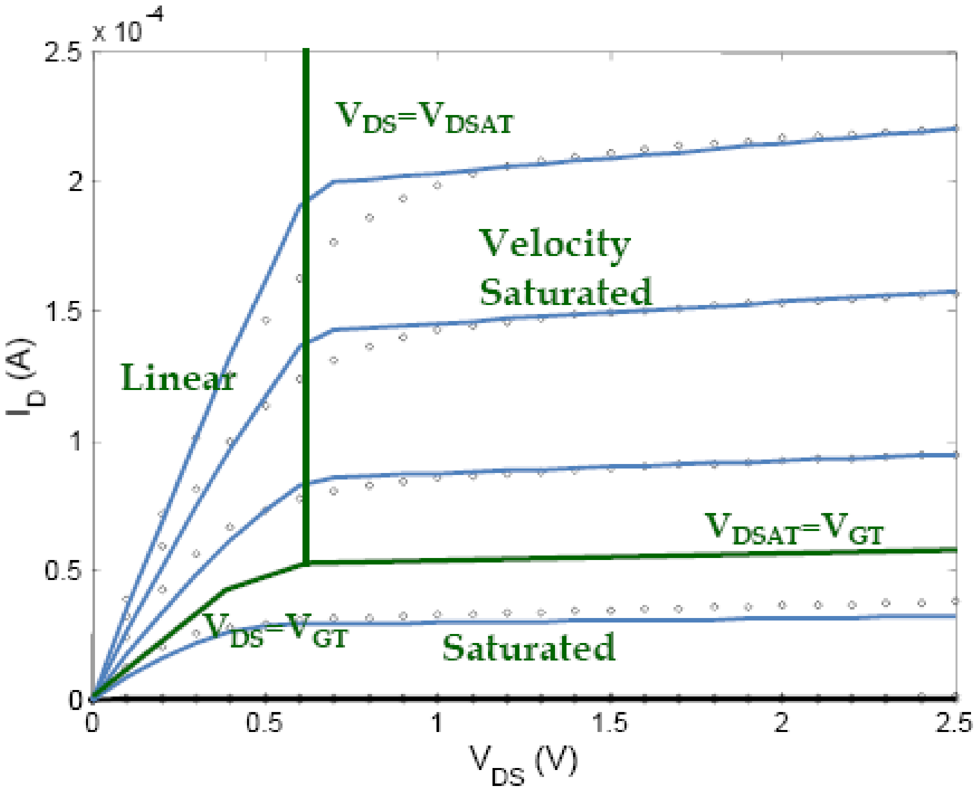




Strong electric field causes carrier mobility degradation

: Compared to feature scaling, voltage scaling is lagging behind

A unified model



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

1. If V_{DS} is minimum:
   Linear region

2. If V_{GT} is minimum:
   Saturation Region

3. If V_{DSAT} is minimum :
   Velocity saturated region