EECS 312 Discussion 5

10/4

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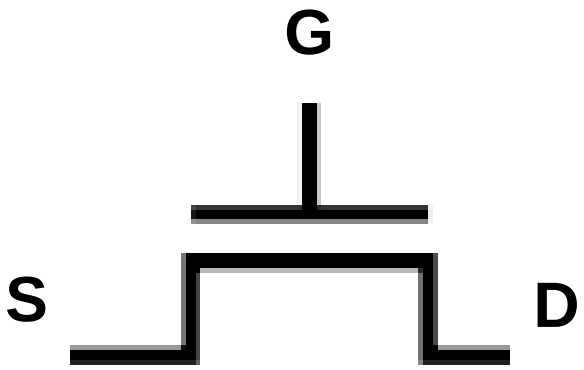
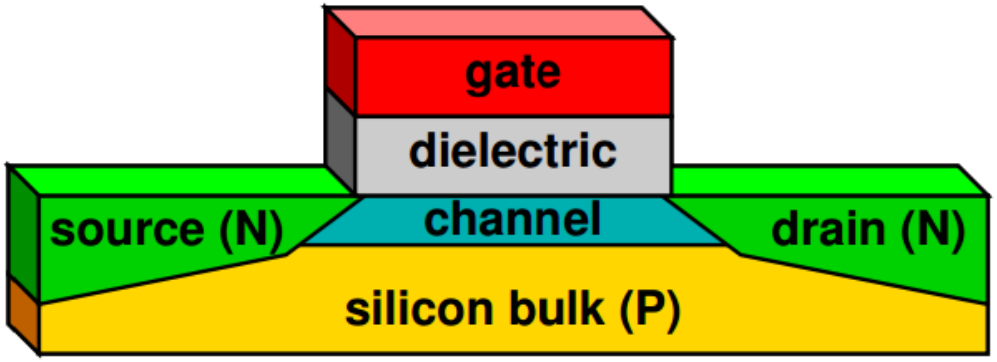
Overview

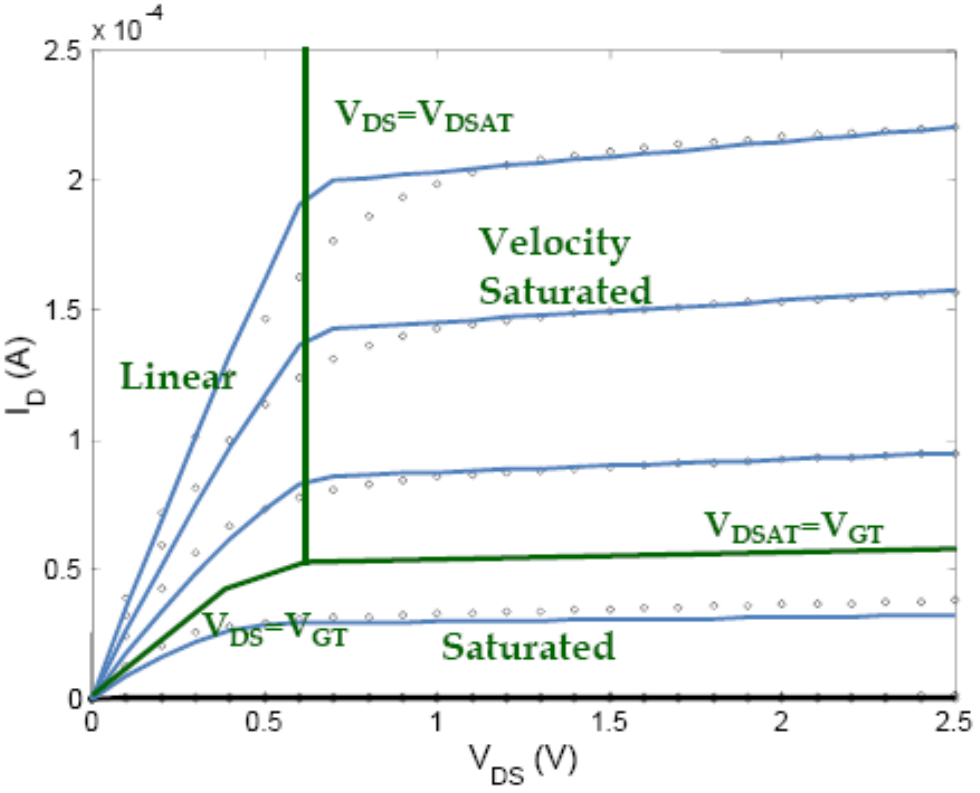
- Reminder
  - HW 2: Due Oct 10
  - Midterm: 8 October 19:00–20:30 in 1670 BBB
  - Close book. One sheet note.

NMOS





A unified model



$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

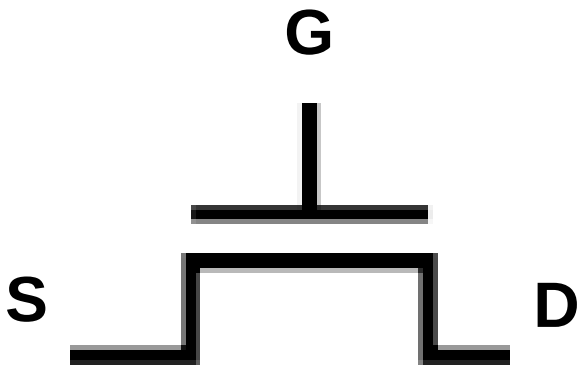
- $2\phi_F$ is negative in NMOS and positive in PMOS
- Υ is positive in NMOS and negative in PMOS
- If $V_{SB}=0$, simply $V_T=V_{T0}$

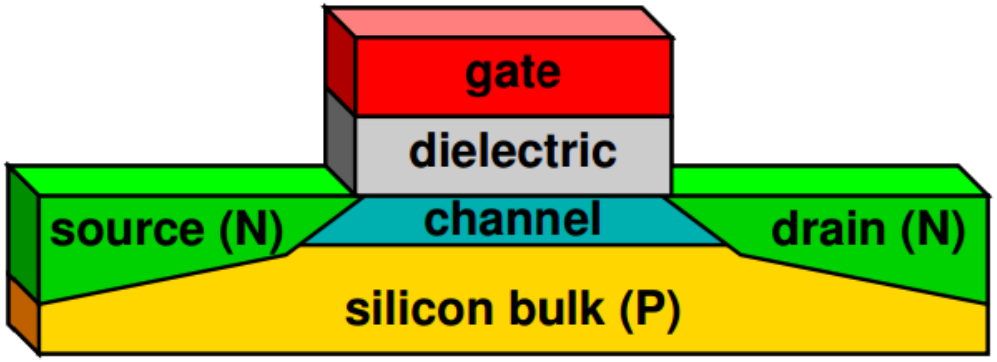
1. If V_{DS} is minimum:
   Linear region

2. If V_{GT} is minimum:
   Saturation Region

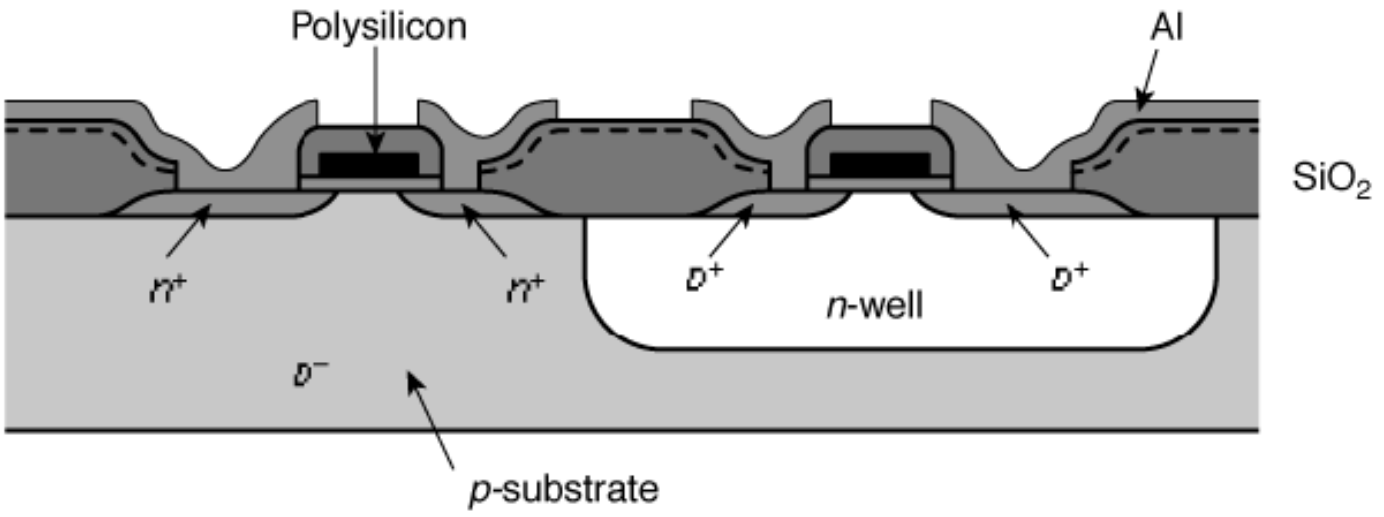
3. If V_{DSAT} is minimum :
   Velocity saturated region

NMOS

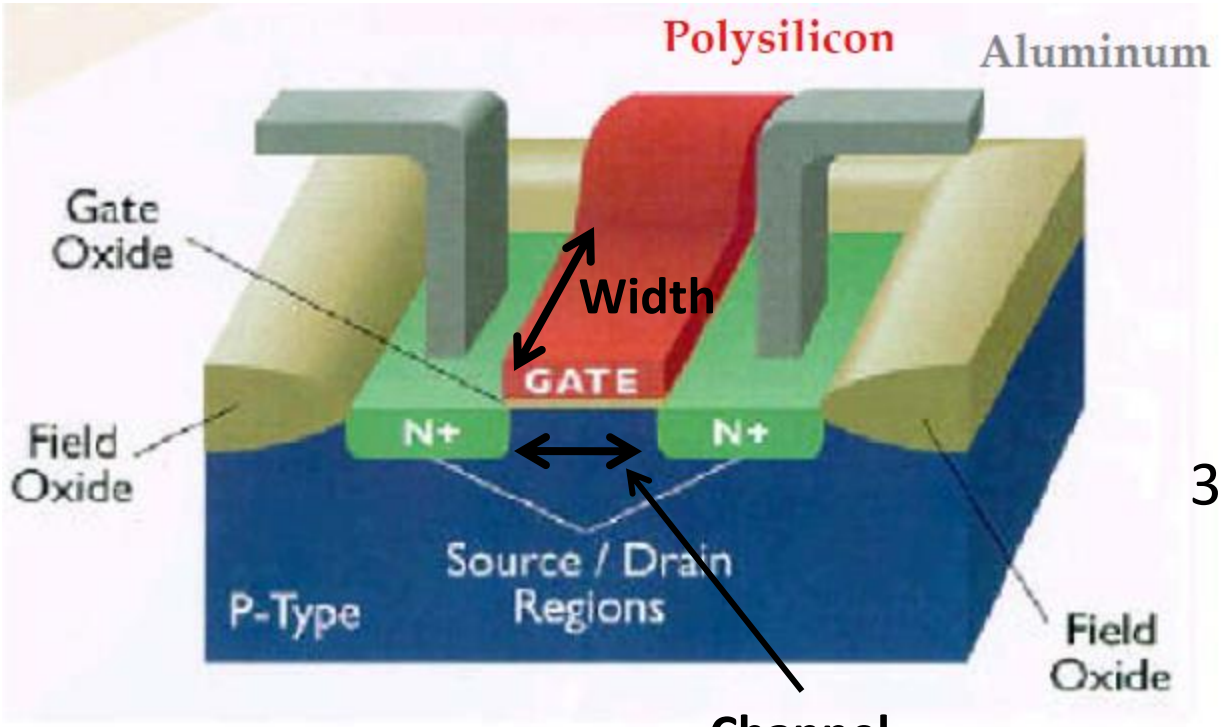




CMOS Process

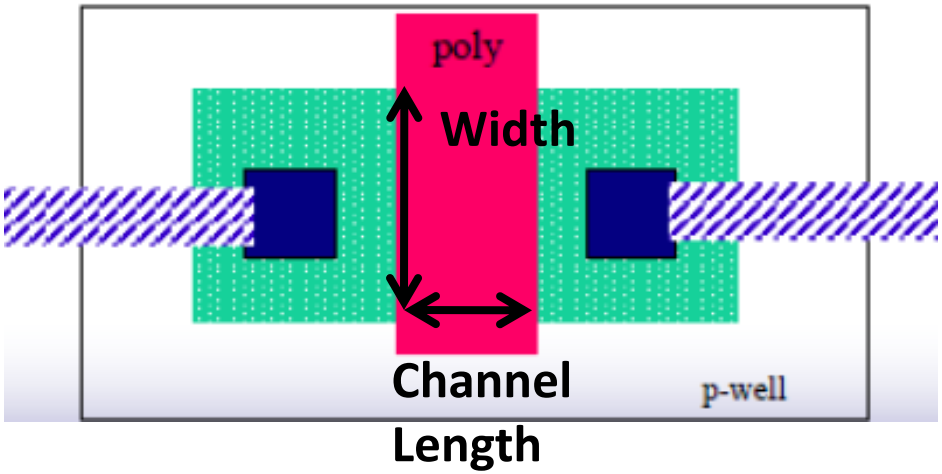


Cross-Sectional View

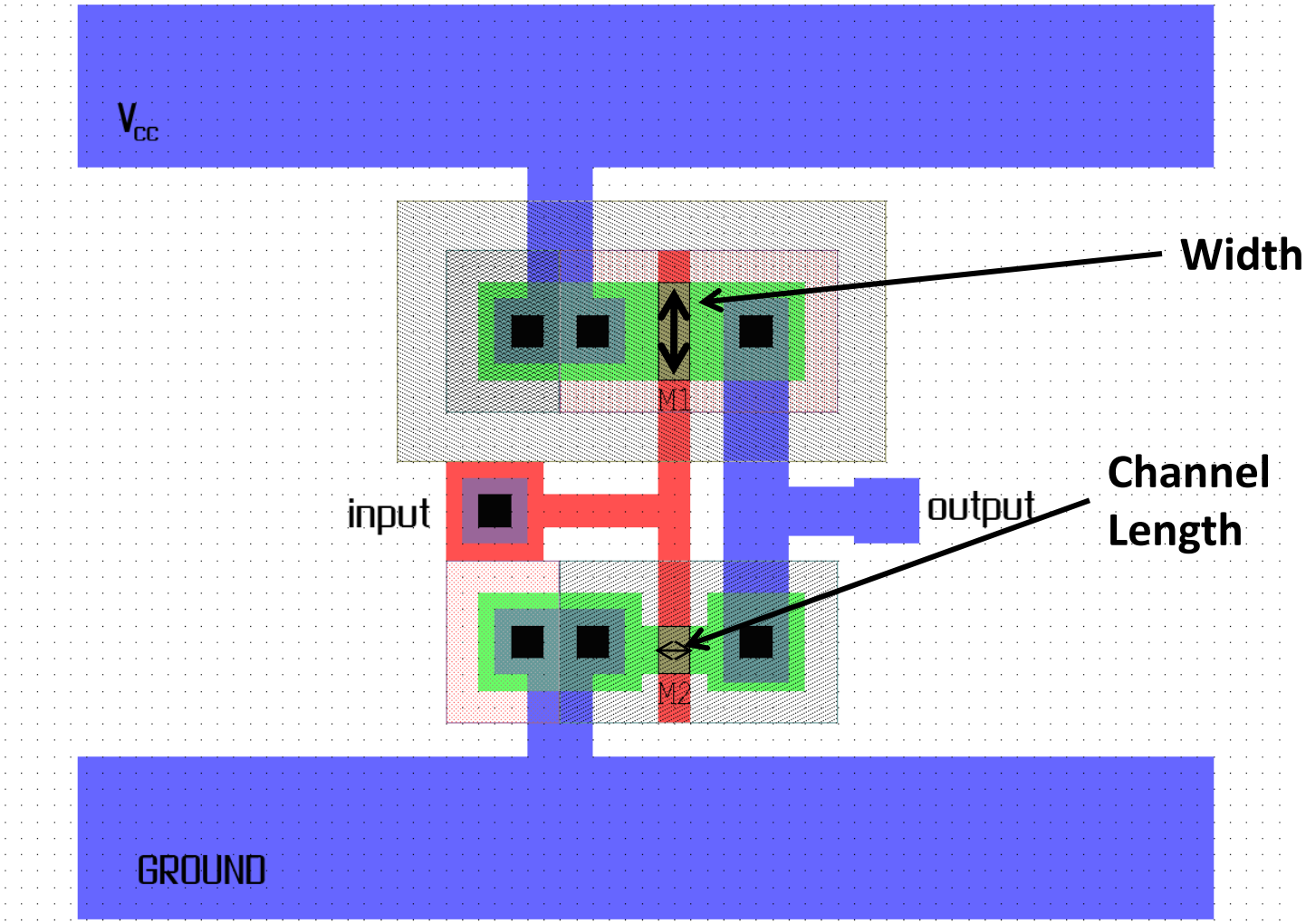


3 Dimensional View

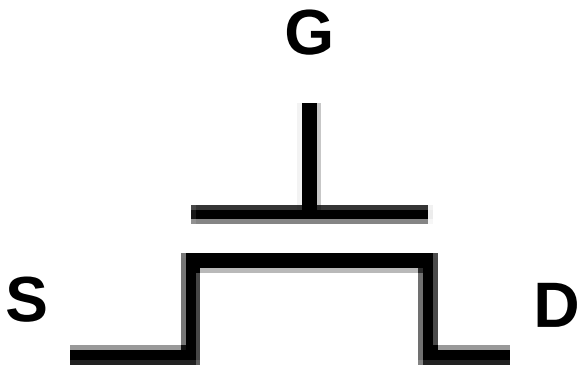
Layout View

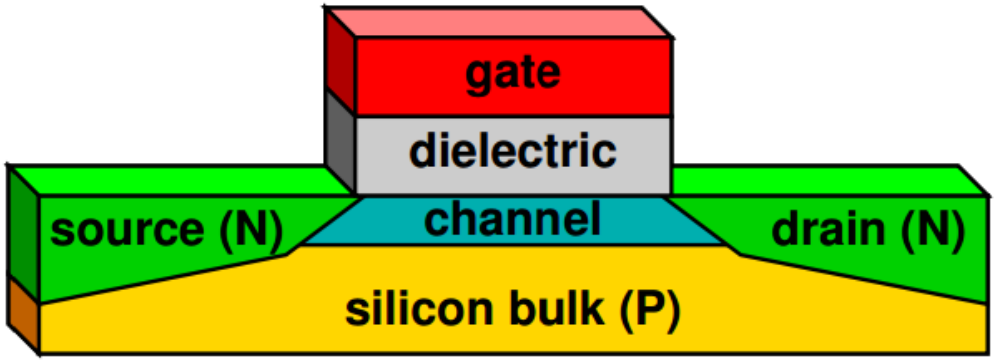


Inverter Layout

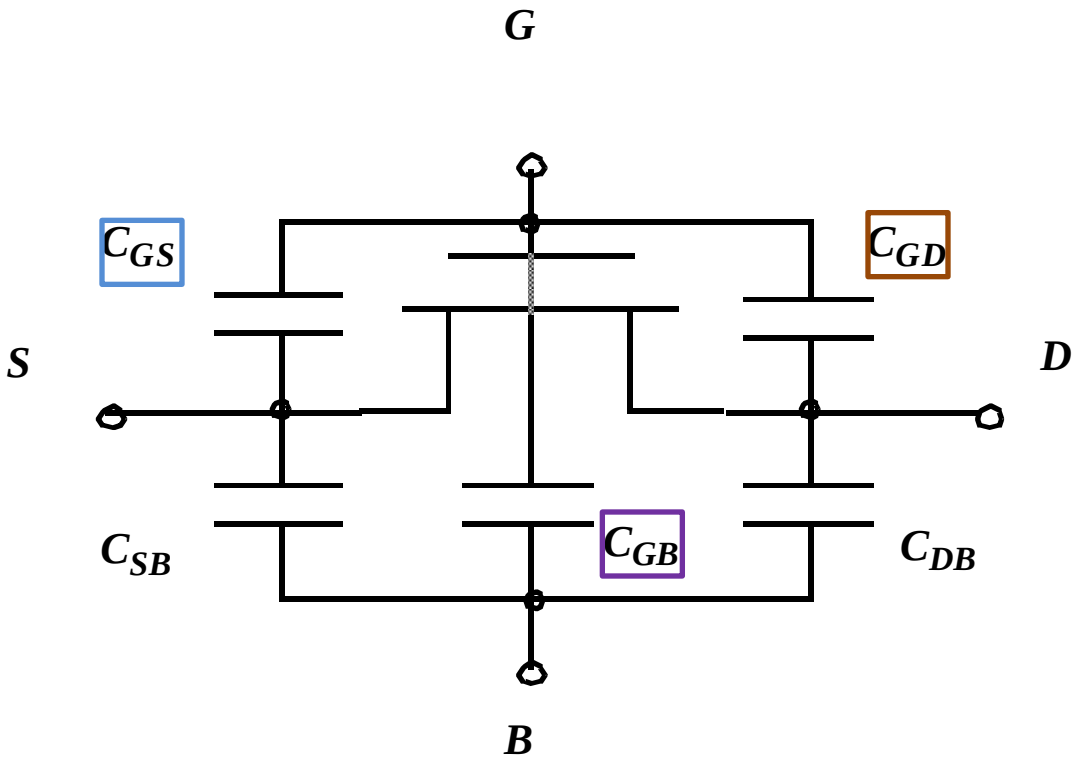


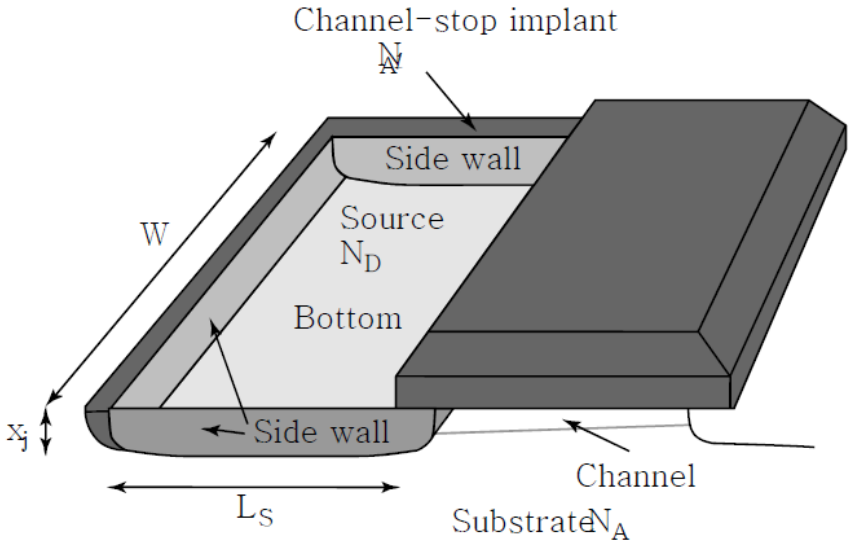
NMOS



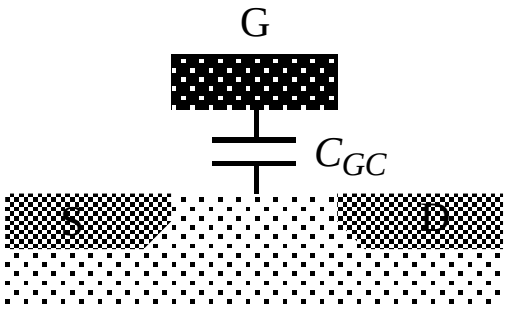


5 Important MOSFET Capacitances

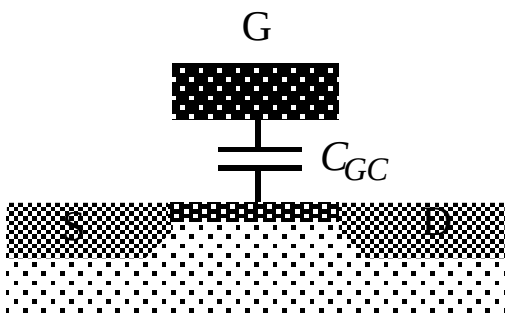




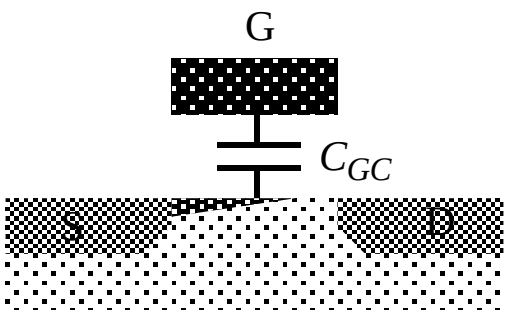
Gate-to-channel Capacitance (C_{GC})



Cut-off



Resistive



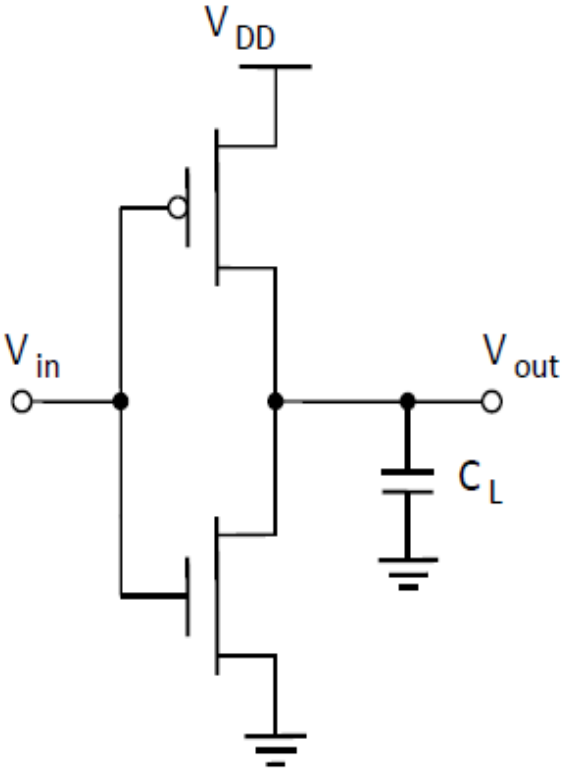
Saturation

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

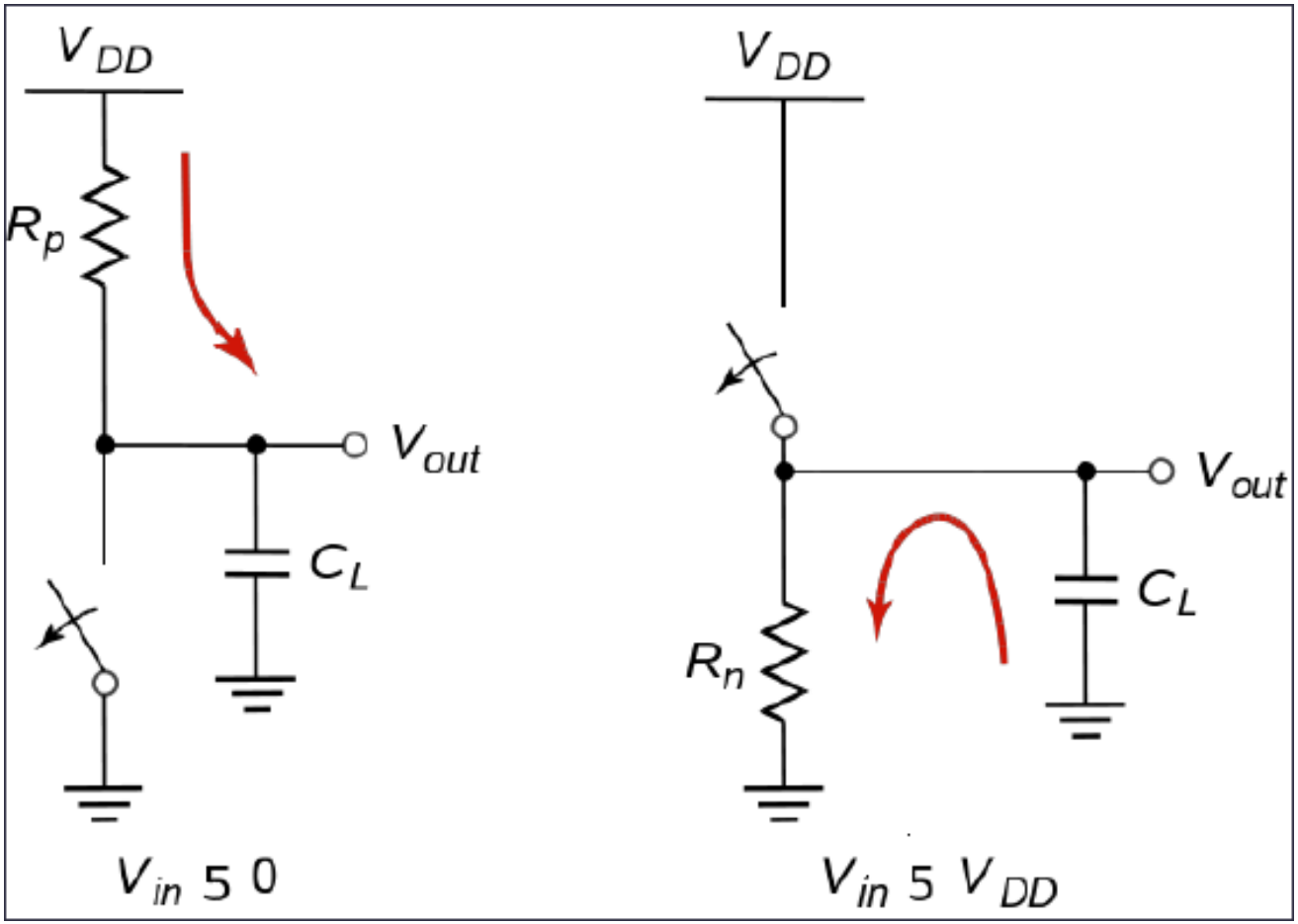
Most important regions in digital design: saturation and cut-off

Properties of Static CMOS gates

- Voltage swing=supply voltage (full swing)
- Logic level is not dependent upon the relative device sizes (ratioless)
- A path with finite resistance between the output and V_{DD} or GND
- Input resistance is extremely high
- No direct path exists between supply and ground under steady-stage

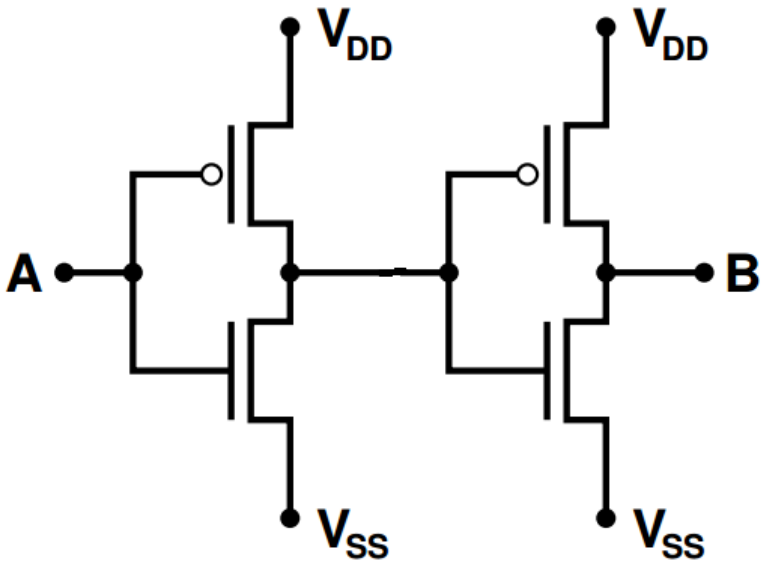


CMOS inverter- Intuitive Perspective



Power

- Dynamic Power
- Static Power
- Short-Circuit Power *



Power

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot {V_{DD}}^2 \cdot f \cdot A$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance

V_{DD} : high voltage

f : switching frequency

A : switching activity

b : MOS transistor gain

V_T : threshold voltage

t : rise/fall time of inputs

$\dagger\ P_{SHORT}$ usually $\leq 10\%$ of P_{SWITCH}

Smaller as $V_{DD} \rightarrow V_T$

$A < 0.5$ for combinational nodes, 1 for clocked nodes.