EECS 312 Discussion 6

10/11

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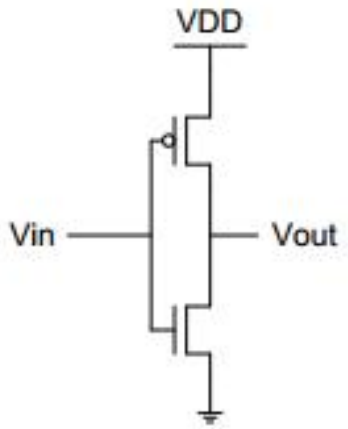
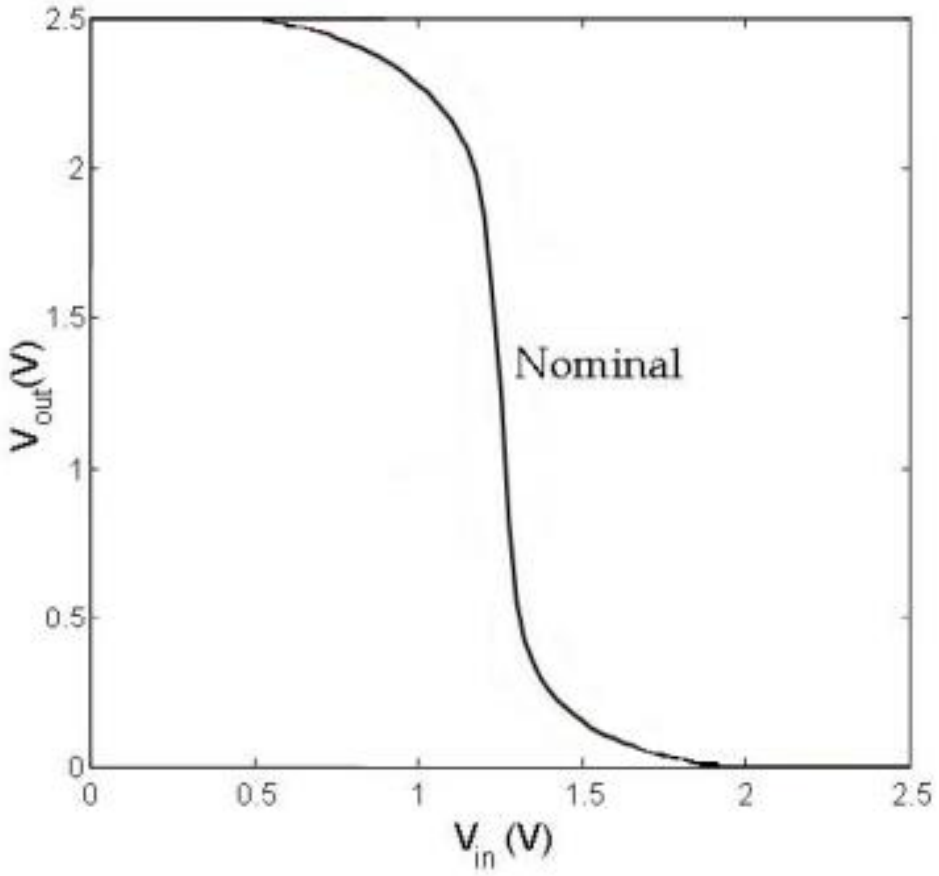
Overview

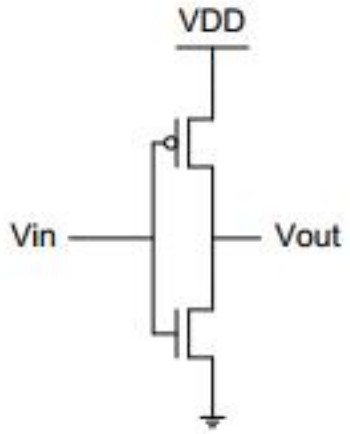
- Reminder
  - Lab 3: Due Oct 25

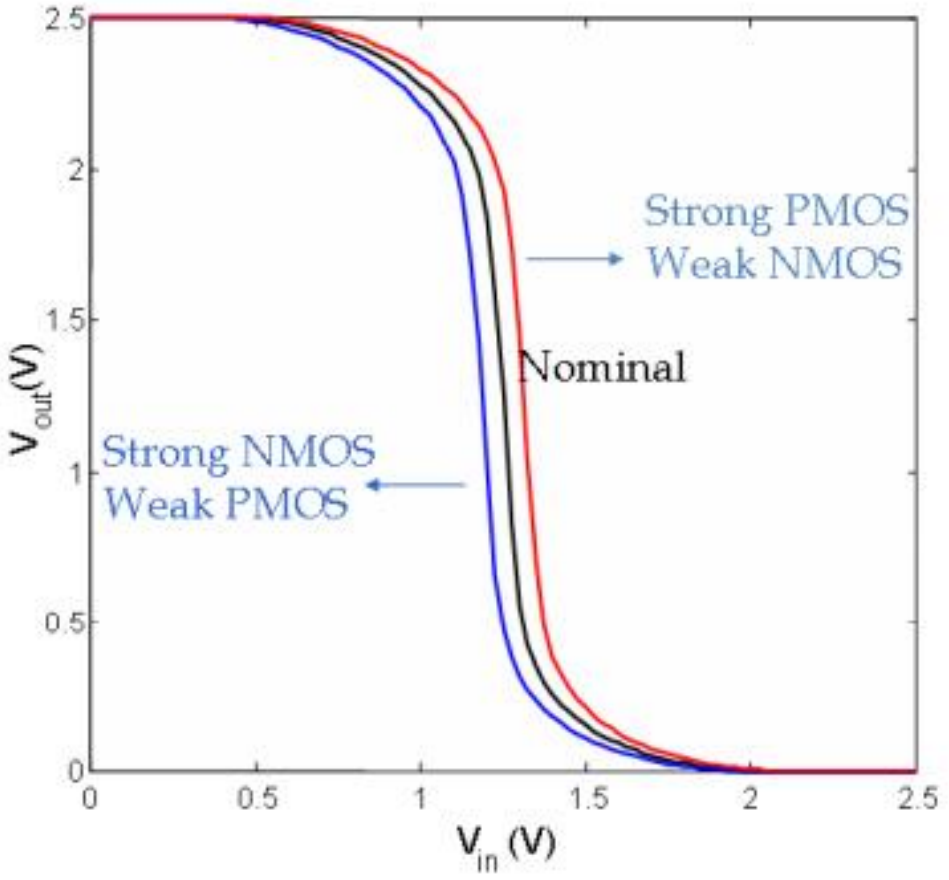
CMOS Inverter



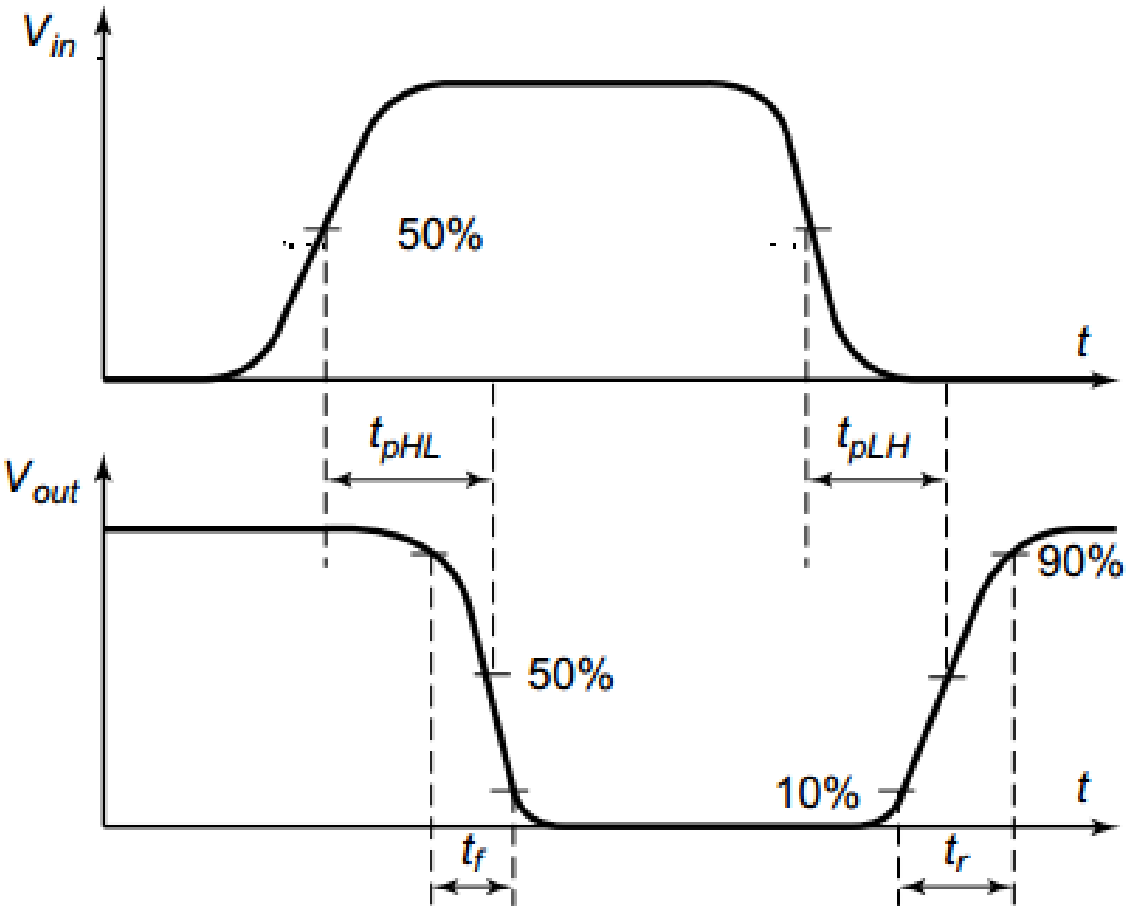


CMOS Inverter

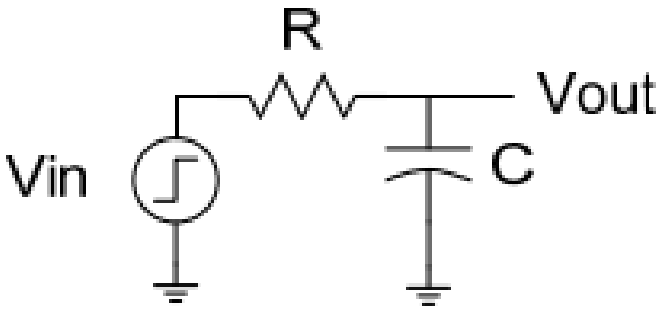




Delay Definition



A Frist-Order RC Network

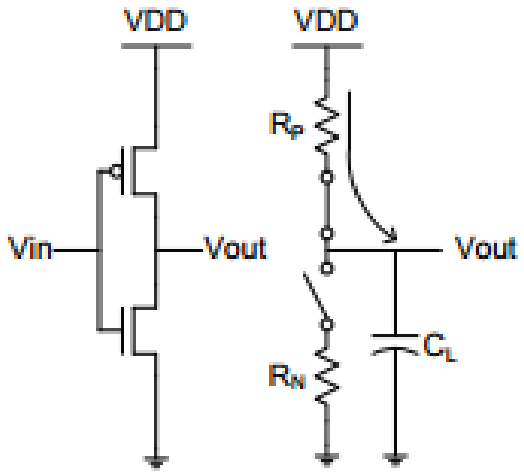


$$V_{out}(t) = (1 - e^{-t/\tau})V$$

$$\tau = R \times C$$

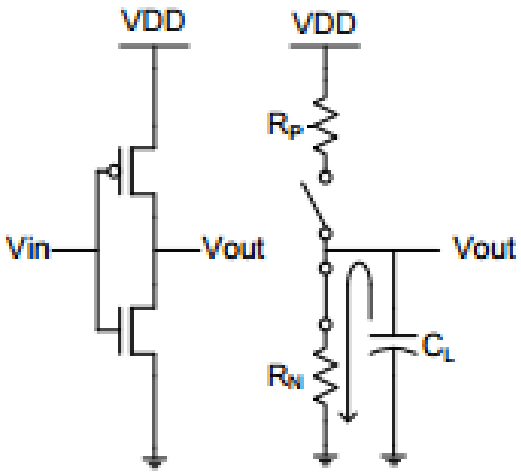
$$t_p = \ln(2)\tau = 0.69R \times C$$

CMOS Inverter: Transient Response



$V_{in} = 0$

(a) Low-to-high



$V_{in} = V_{DD}$

(b) High-to-low

$$t_{pHL} = f(R_N \times C_L)$$

$$t_{pHL} = 0.69 R_N \times C_L$$

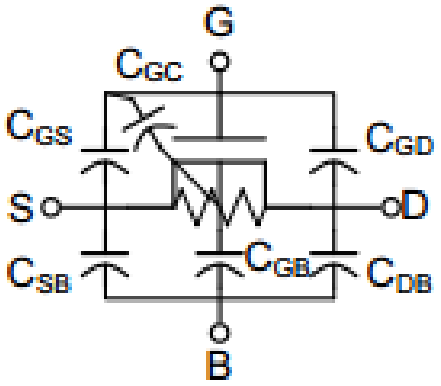
$$t_{pLH} = 0.69 R_P \times C_L$$

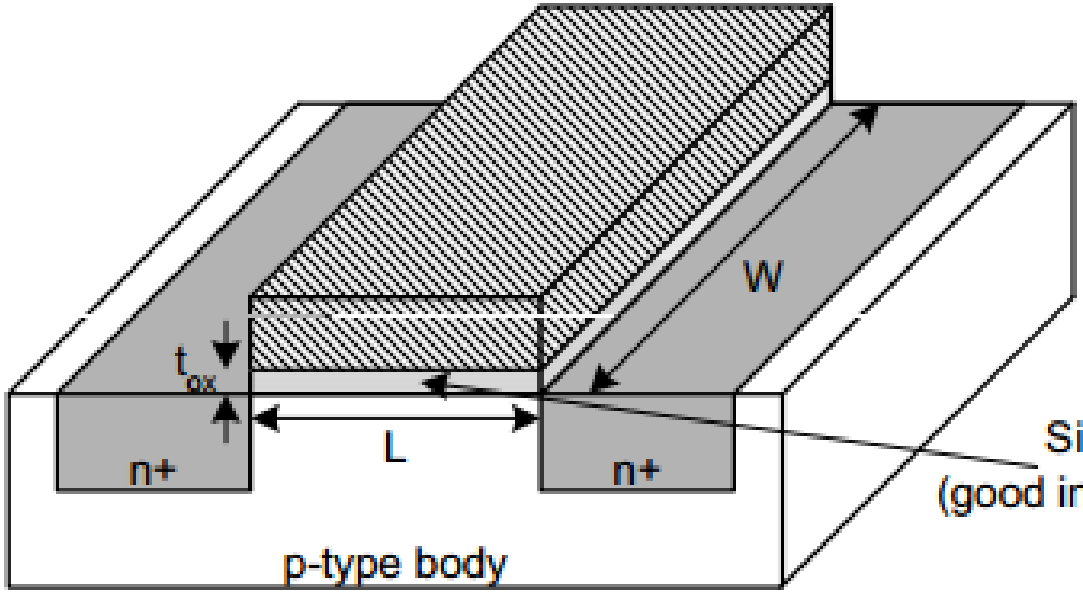
Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

- Gate capacitance can be complex, but we will use a simple model
- $C_{GC} = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{per\_micron} W$

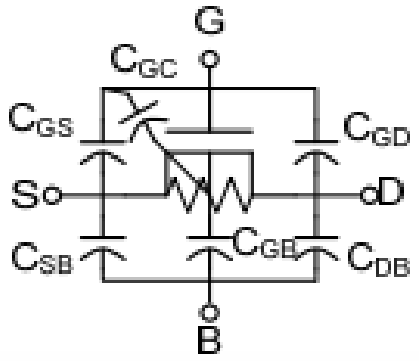


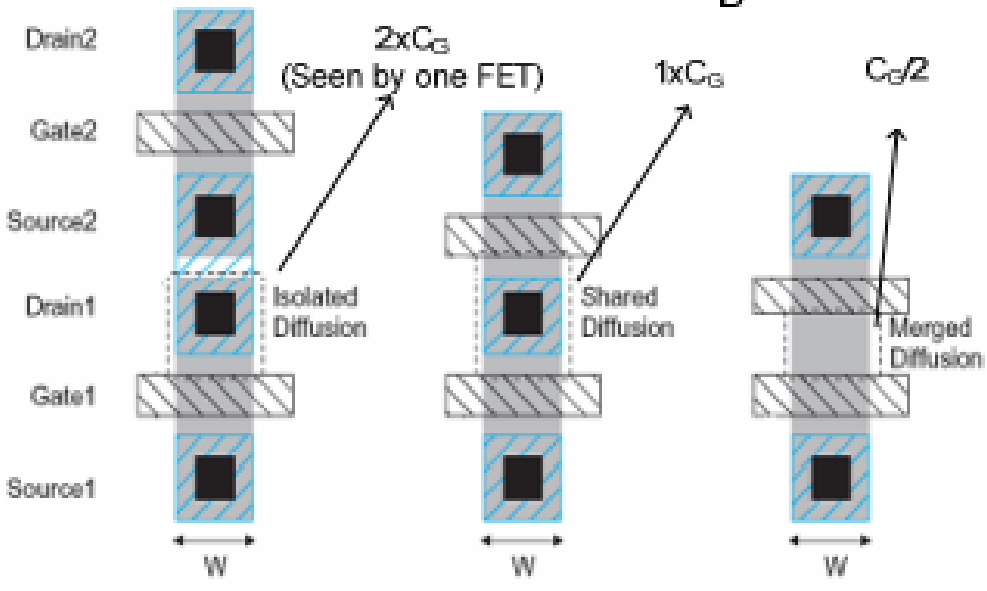


SiO_2 gate oxide
(good insulator, $\varepsilon_{ox} = 3.9\varepsilon_0$)

Diffusion Capacitance

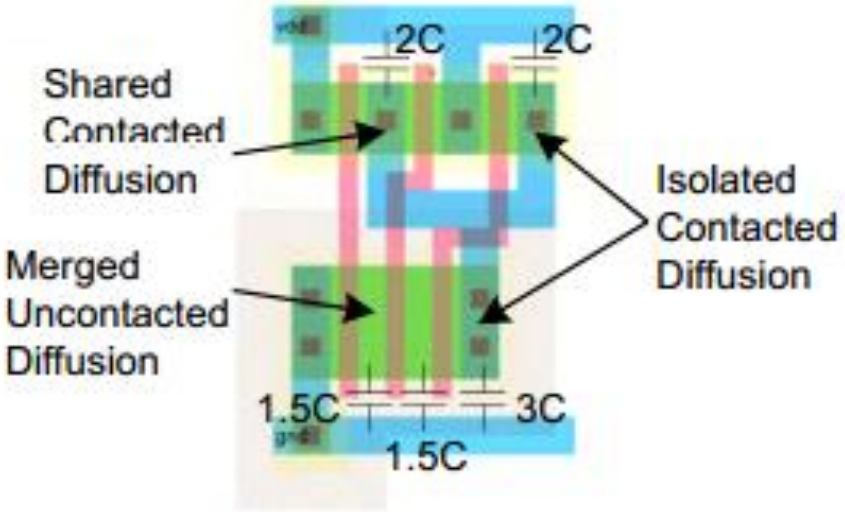
- C_{SB}, C_{DB}
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to C_G for contacted diff
  - ½ C_G for uncontacted
  - Varies with process

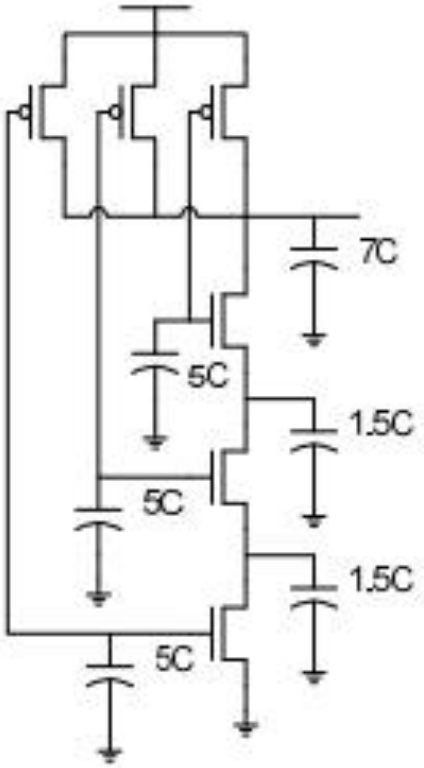




Diffusion Capacitance: Example

- Easiest to assume a contacted diffusion on every source/drain
- BUT: Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion helps also

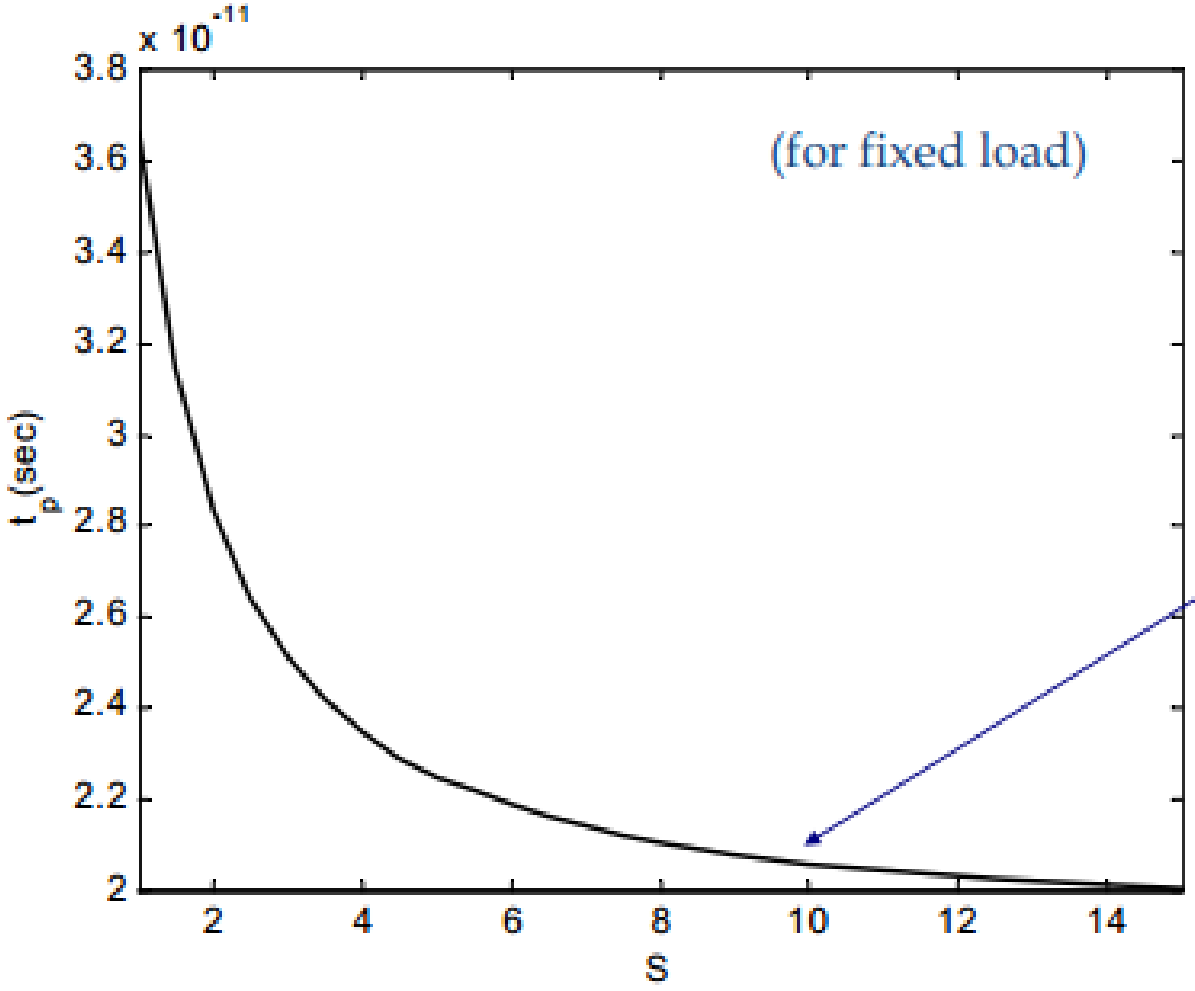


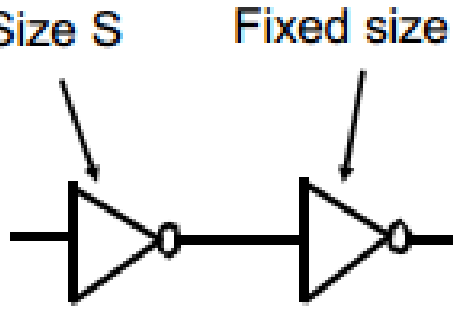


Design for Performance

- Keep capacitances small – lower C
  - Compact layout, good placement (short wires & no diffusion routing)
- Increase transistor sizes – lower R
  - Watch out for self-loading! – parasitic C increases!
- Increase V_{DD}
  - Not usually possible due to reliability and power penalties

Device Sizing

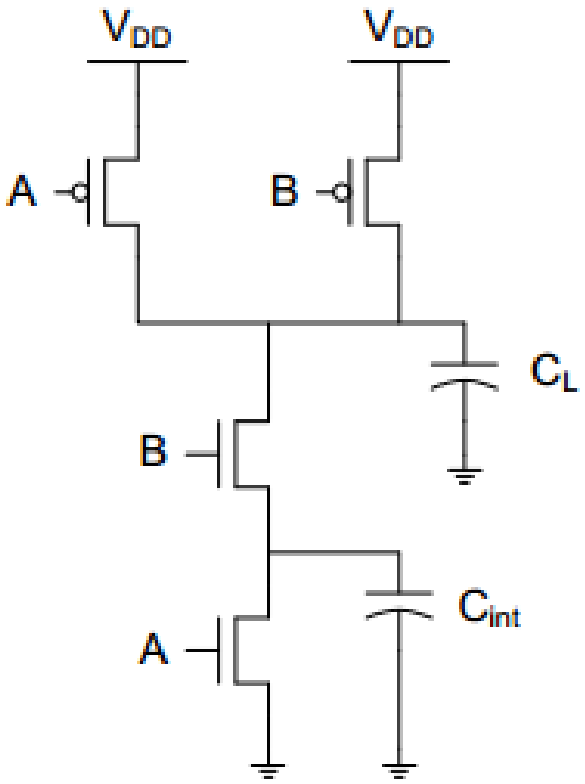




Increasing device width
Leads to self-loading:
Intrinsic capacitances
dominate

S = Wp/Wp_min = Wn/Wn_min

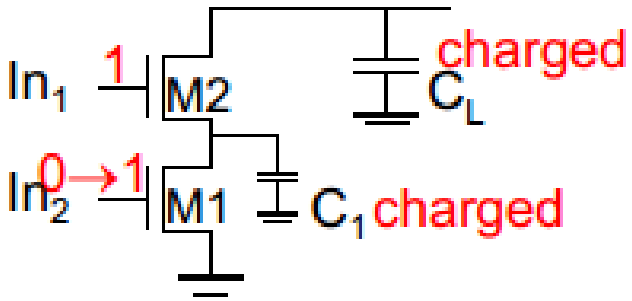
Input Pattern Effects on Delay



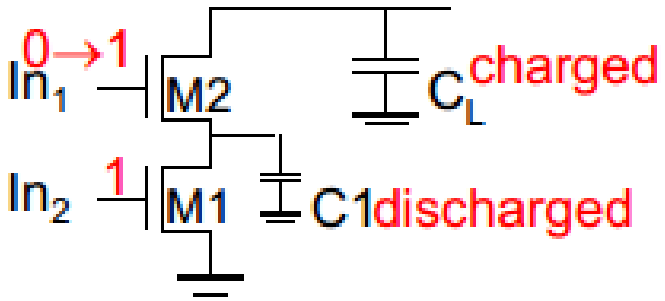
- Delay is dependent on the pattern of inputs
- *Ignore Cint for the moment!*
- Low to high transition
  - both inputs go low
    - delay is 0.69 $R_p/2$ C_L
  - one input goes low
    - delay is 0.69 R_p C_L
- High to low transition
  - both inputs go high
    - delay is 0.69 $2R_n$ C_L

Fast Complex Gates: Design Techniques

- Transistor Ordering

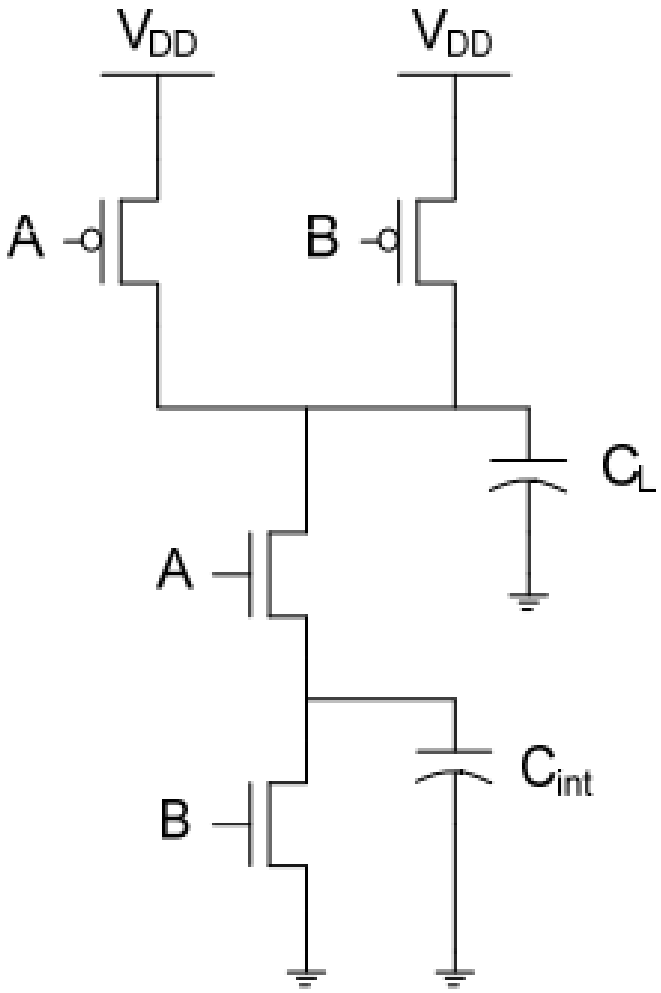


delay determined by time to discharge C_L, C_1



delay determined by time to discharge C_L

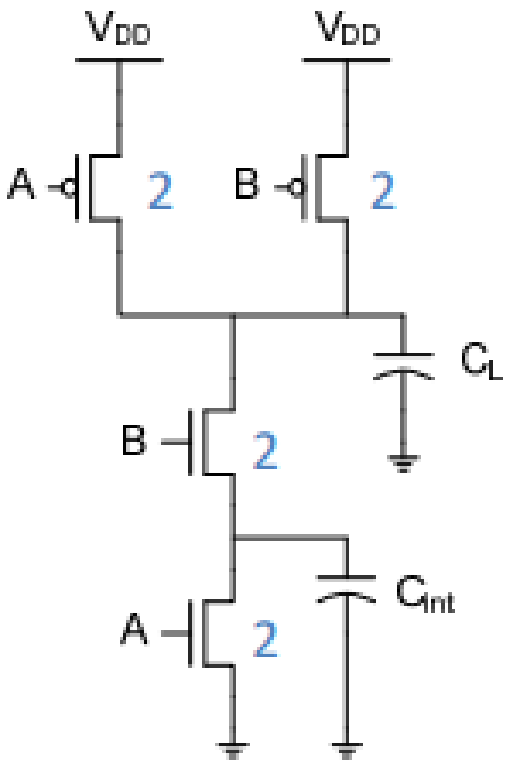
Delay Dependence on Input Patterns

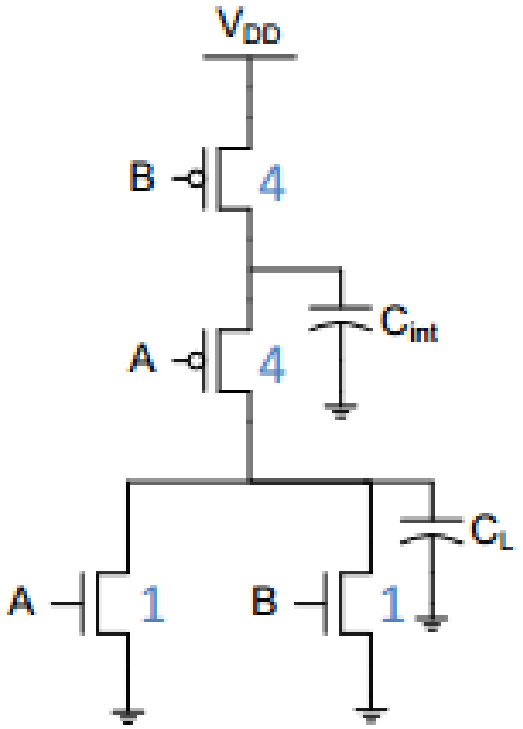


Input Data Pattern	Delay (psec)
A=B=0→1	69
A=1, B=0→1	62
A= 0→1, B=1	50
A=B=1→0	**35**
A=1, B=1→0	**76**
A= 1→0, B=1	57

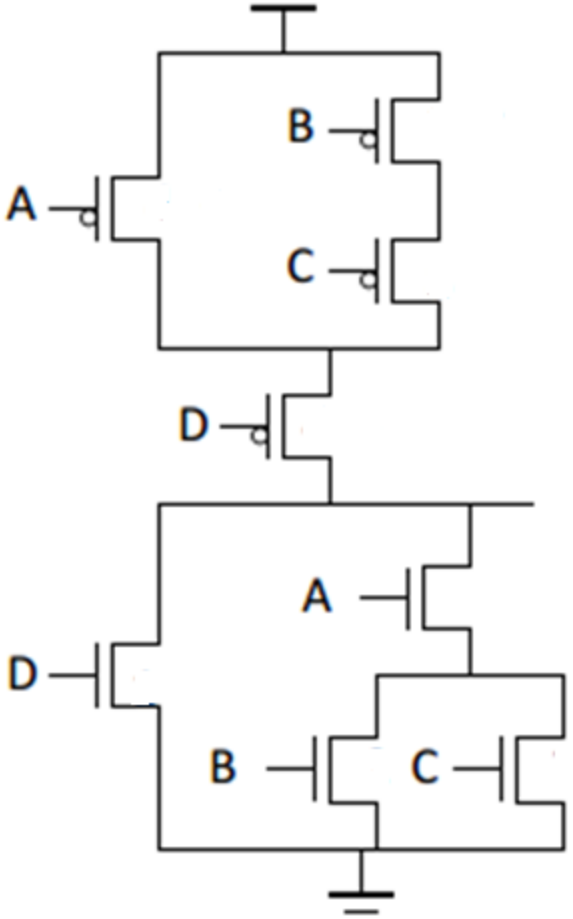
NMOS = 0.5µm/0.25 µm
PMOS = 0.75µm/0.25 µm
C_L = 100 fF

Transistor Sizing



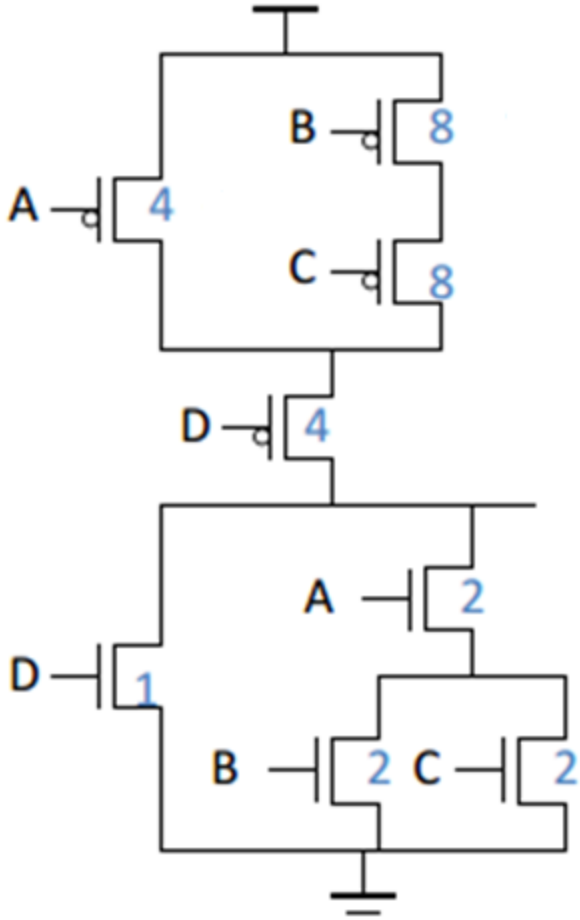


Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$

Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$

Summary

- CMOS delays dictated by device sizing, layout, wires
  - RC model is accurate to first-order
  - Computing delays of complex gates is challenging due to input pattern dependency
  - Watch out for self-loading; size appropriately

HW2 Q6

- Vt of A = -0.4V
- Vt of B = 0.4V
- Vdd = 2.5V