EECS 312 Discussion 7

10/18

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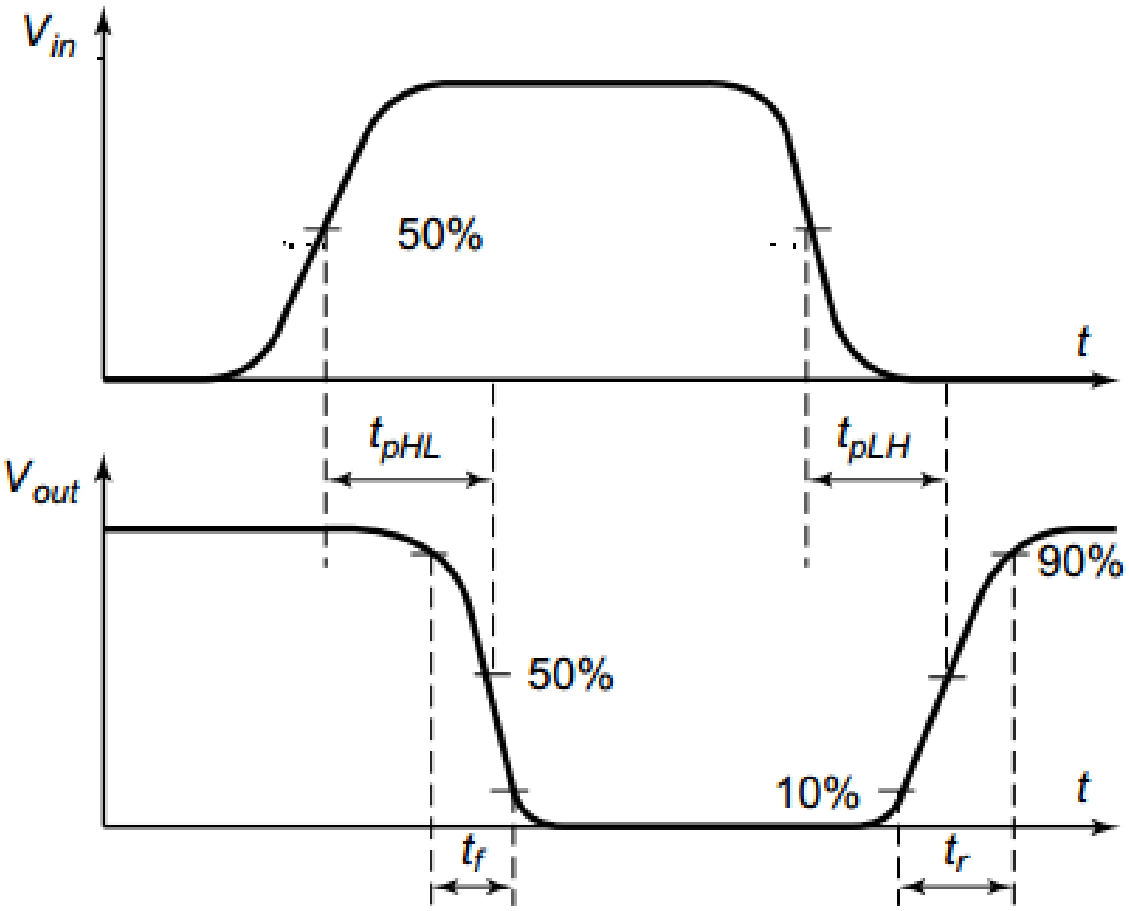
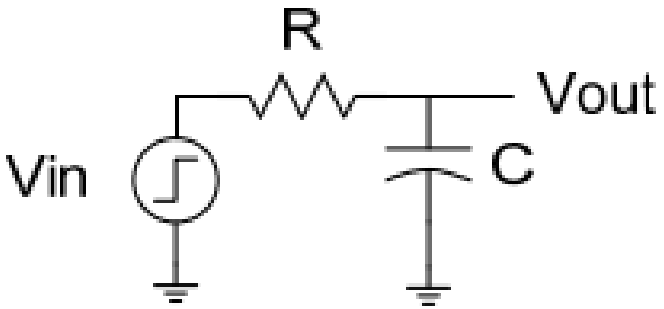
Overview

- Reminder
  - Lab 3: Due Oct 25
- Dis 6 review
- Logic effort
- Midterm review

Delay Definition



A Frist-Order RC Network

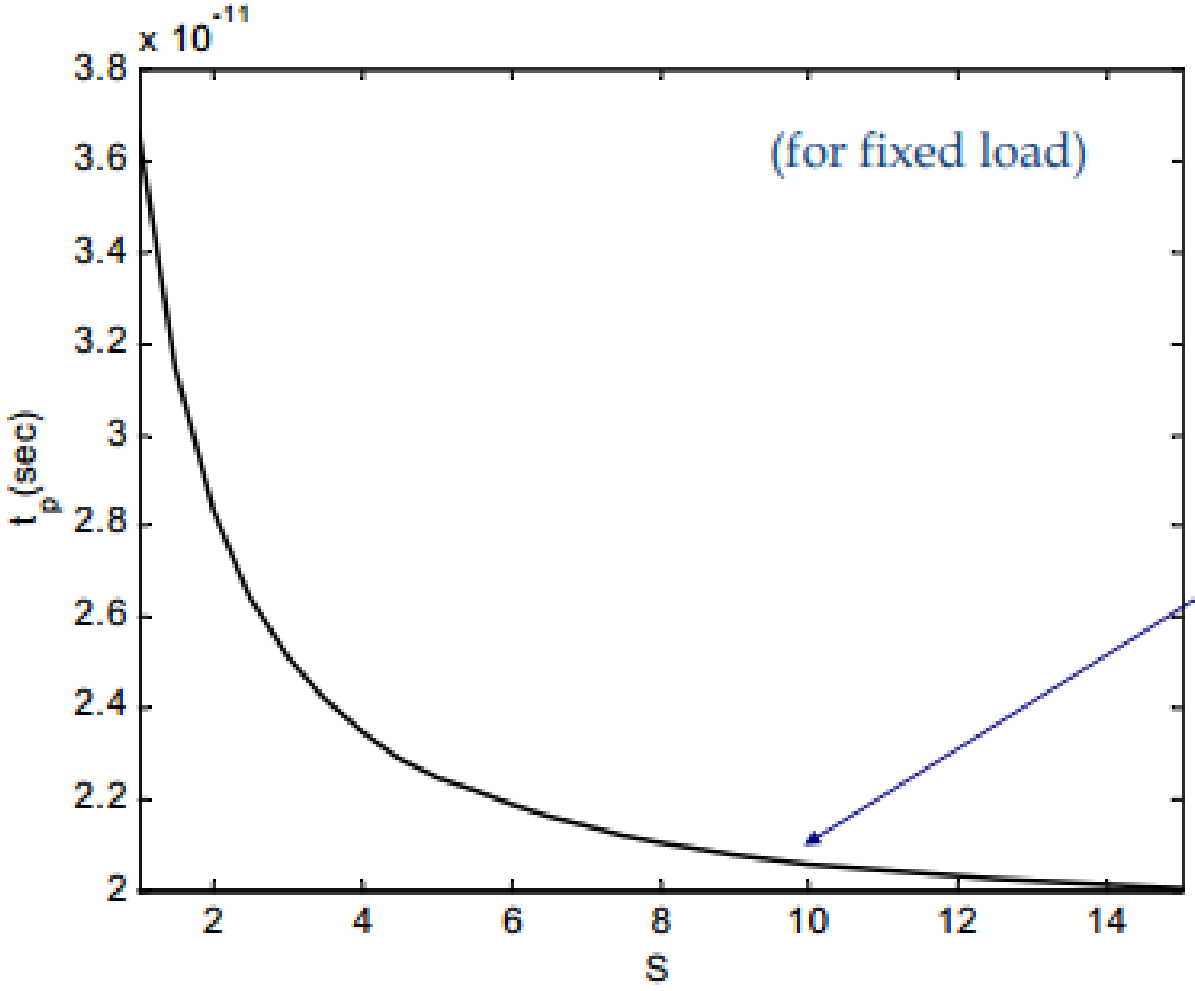


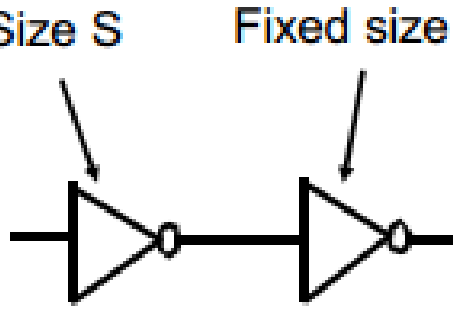
$$V_{out}(t) = (1 - e^{-t/\tau})V$$

$$\tau = R \times C$$

$$t_p = \ln(2)\tau = 0.69R \times C$$

Device Sizing

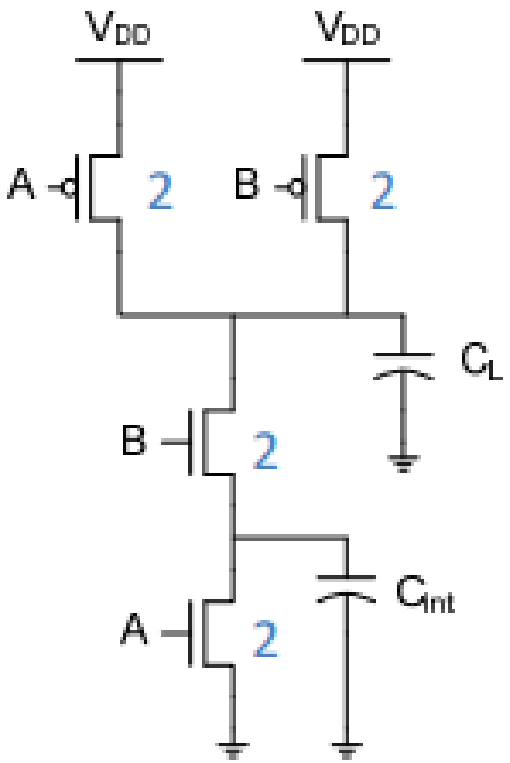


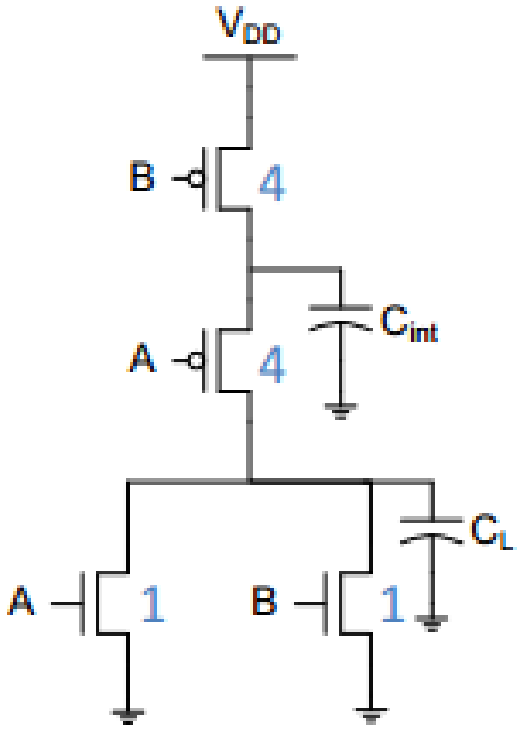


Increasing device width
Leads to self-loading:
Intrinsic capacitances
dominate

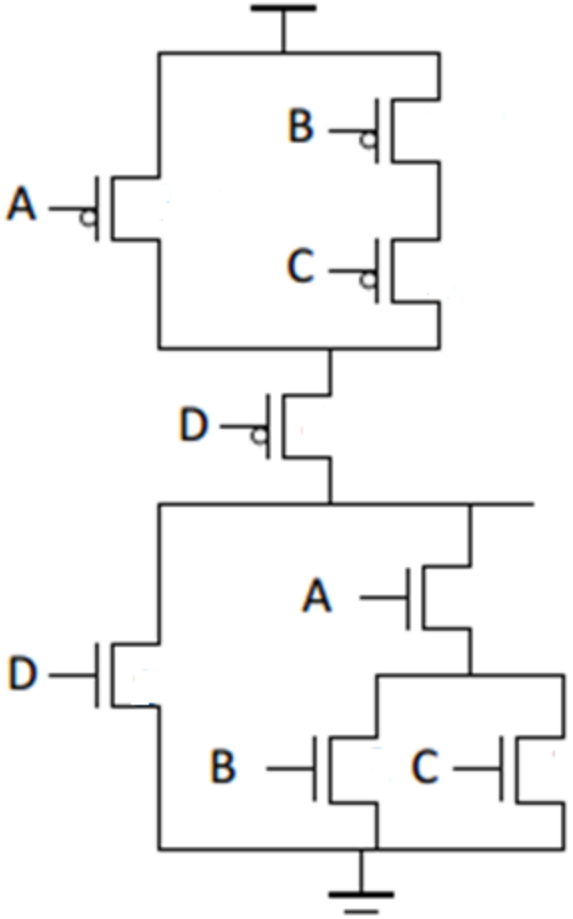
S = Wp/Wp_min = Wn/Wn_min

Transistor Sizing



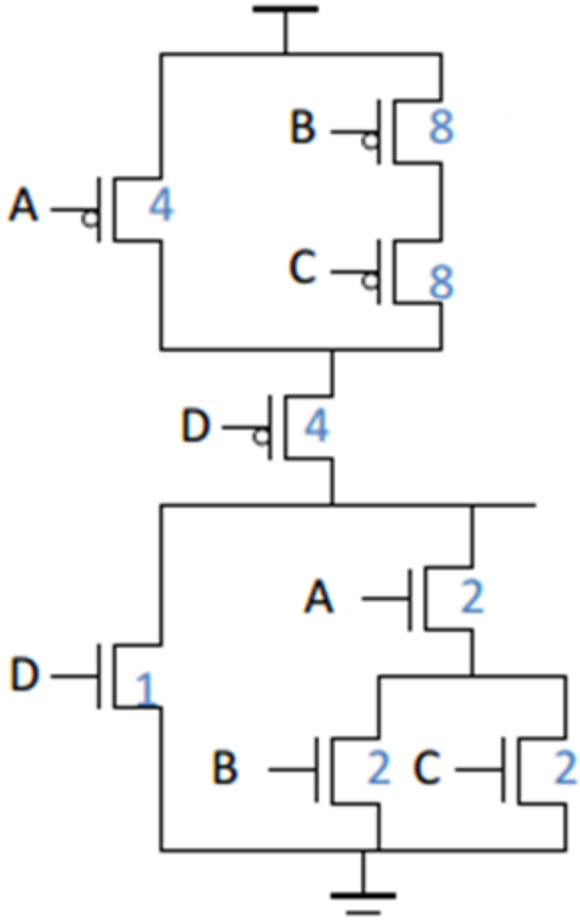


Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$

Transistor Sizing a Complex CMOS Gate



$$OUT = \overline{D + A \bullet (B + C)}$$

Summary

- CMOS delays dictated by device sizing, layout, wires
  - RC model is accurate to first-order
  - Computing delays of complex gates is challenging due to input pattern dependency
  - Watch out for self-loading; size appropriately

Logic Effort

Logical Effort Motivation

- Sizing of a chain of inverters
  - Geometric progression
- How about more complex logic?
- Logical Effort objectives:
  - Quick & dirty, back of the envelope sizing
  - Make trade-off between circuits
  - What is the best circuit topology for a function?
  - How many stages of logic give least delay?
  - How wide should the transistors be?

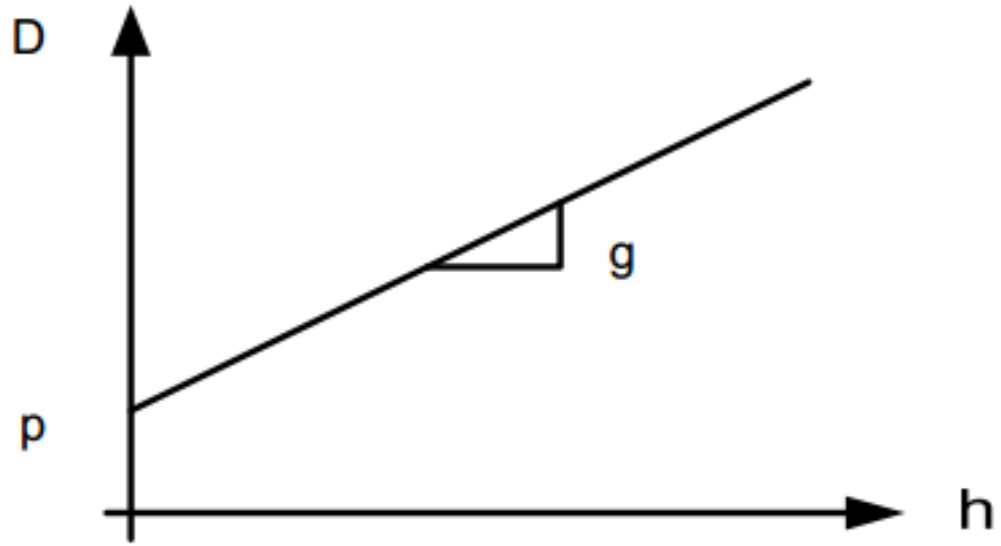
Delay in a Logic Gate

- Express delays in process-independent unit
- Delay has two components:

$$d = f + p$$

- f: *effort delay* = gh (a.k.a. stage effort)
  - Again has two components
- g: *logical effort*
  - Measures relative ability of gate to deliver current
  - $g \equiv 1$ for inverter
- h: *electrical effort* = C_{out} / C_{in}
  - Ratio of output to input capacitance
  - Sometimes called fanout
- p: parasitic delay
  - Represents delay of gate driving no load
  - Set by internal parasitic capacitance

Units of effort



- Reference is the inverter:

$$g_{inv} = 1$$

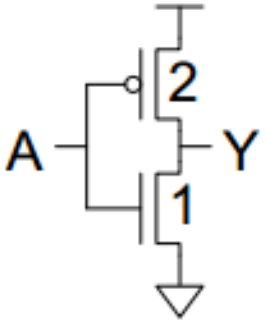
$$p_{inv} = 1\tau$$ 20ps of 250nm

- g is a function of the complexity of a gate, not its size

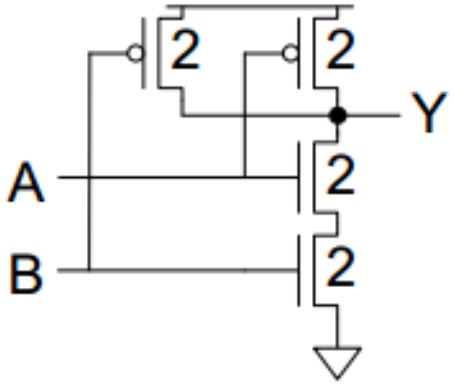
- p is a function of the technology and gate type

Computing Logical Effort

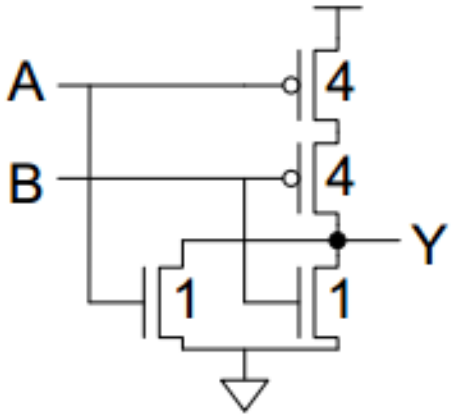
- DEF: *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current (i.e, effort delay under same loading)*.
- Measure from delay vs. fanout plots
- Or estimate by counting transistor widths



C_{in} = 3
g = 3/3



C_{in} = 4
g = 4/3



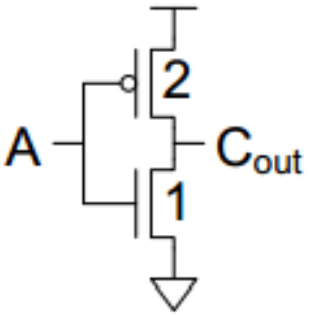
C_{in} = 5
g = 5/3

Logical effort (g)

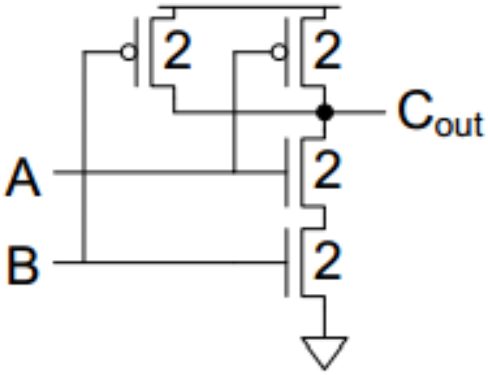
	Number of inputs					
Gate type	**1**	**2**	**3**	**4**	**5**	**n**
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n + 2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3
Multiplexer		2	2	2	2	2

Computing Parasitic Delay

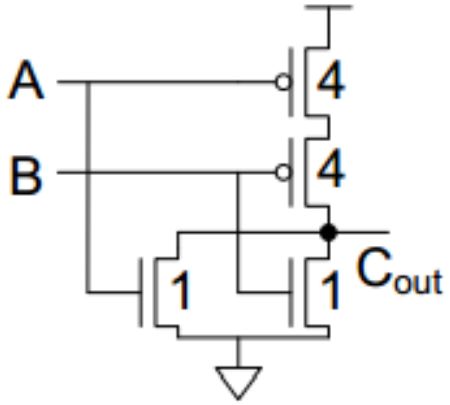
- Measure from delay vs. fanout plots
- Or estimate by counting self loading on output node for sizing with equal output current to inverter
- For simplification, we ignore internal node capacitance



$C_{out} = 3$
$p = 3/3$



$C_{out} = 6$
$p = 6/3 = 2$

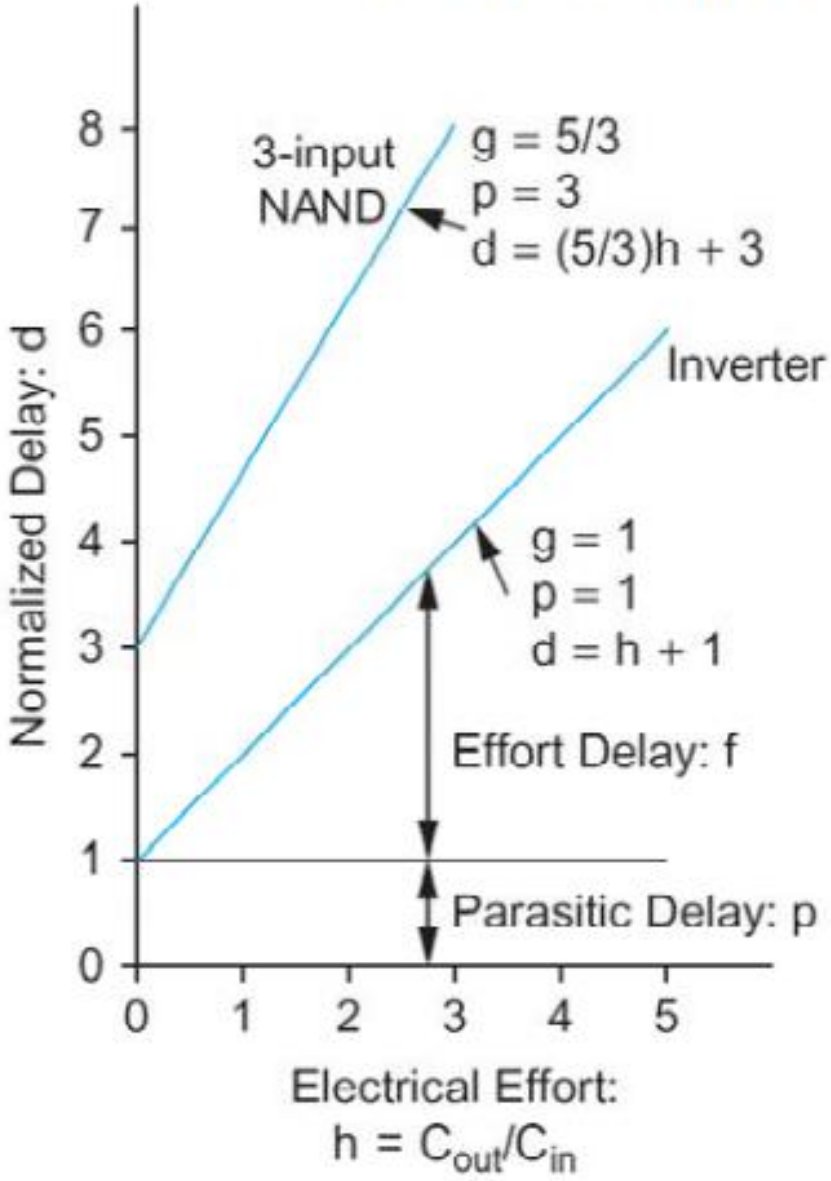


$C_{out} = 6$
$p = 6/3 = 2$

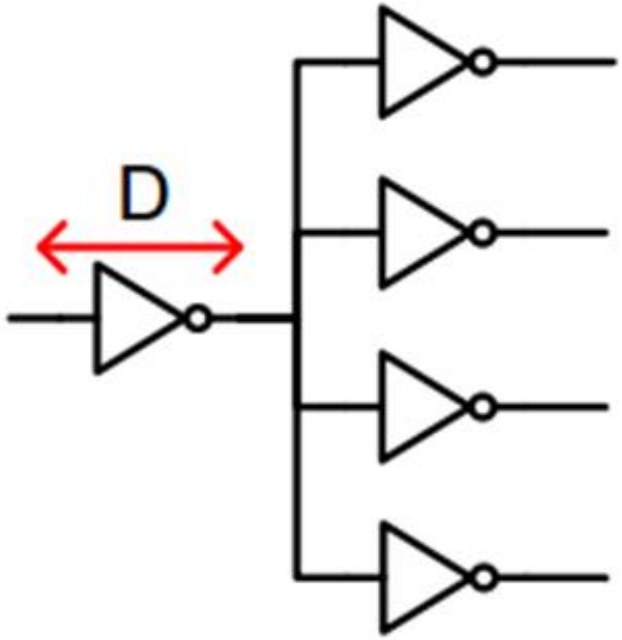
Parasitic Delay (p)

Gate type	Parasitic Delay
Inverter	p_{inv}
n-input NAND	$n.p_{inv}$
n-input NOR	$n.p_{inv}$
n-way multiplexer	$2n.p_{inv}$

Delay components



Fanout 4 Example



$$C_{out} = 4C_{in}$$

$$h = 4$$

$$g = 1$$

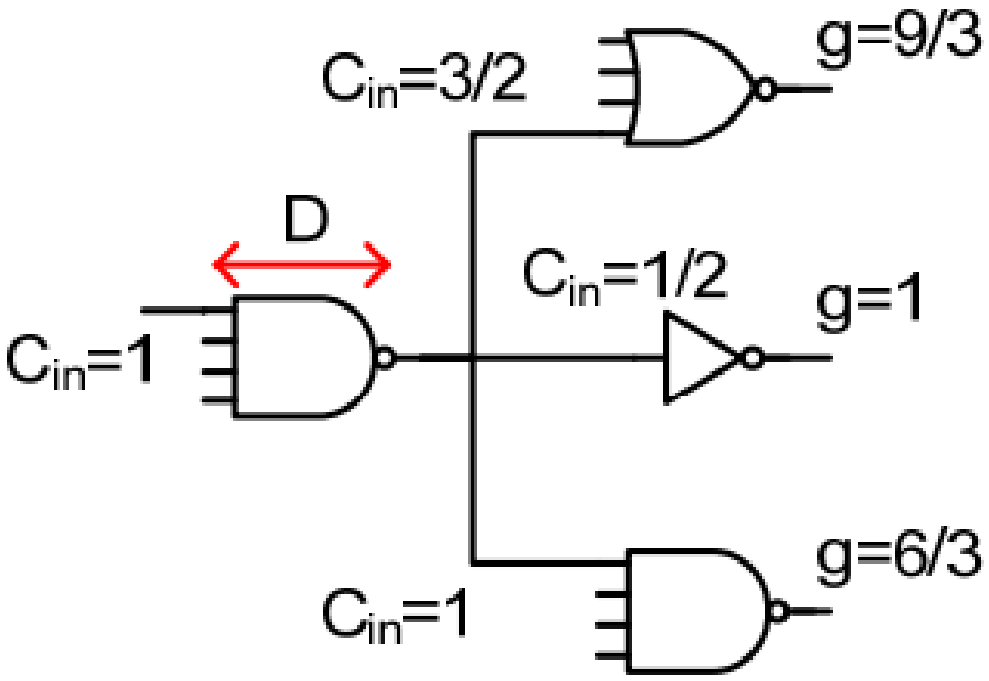
$$p = 1$$

$$D = 4 + 1 = 5\tau$$

FO4 delay

96ps of 250nm

More complex circuit



$$h = 3$$

$$g = \frac{6}{3}$$

$$p = 4 \times 1$$

$$D = 10\tau$$