EECS 312 Discussion 9

11/1

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Overview

- Reminder
  - Lab 4: Due Nov 7

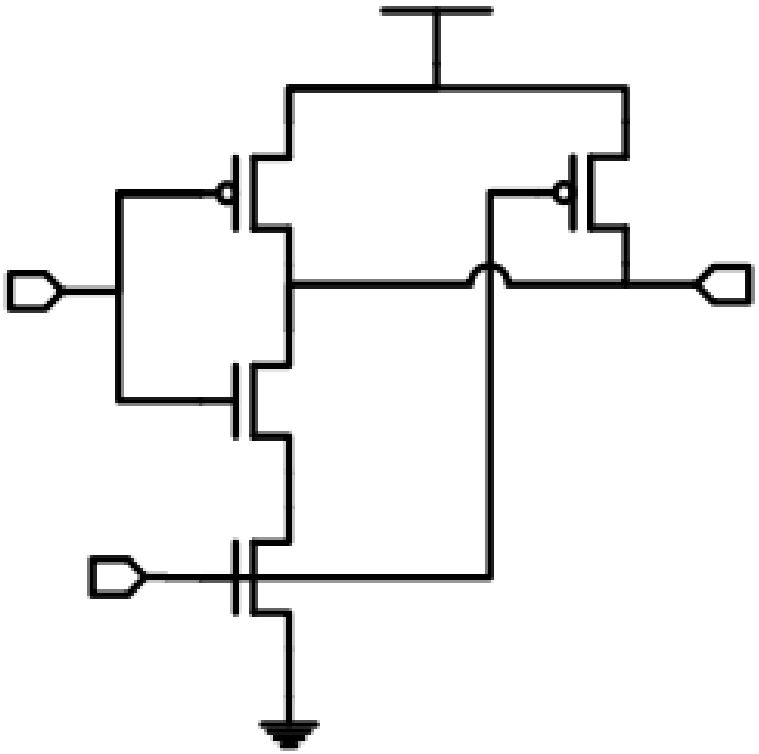
- Classic CMOS gate review
- DCVS (Differential Cascode Voltage Switch)
- Pass Gate Logic

- Dynamic Logic

Static Logic Families

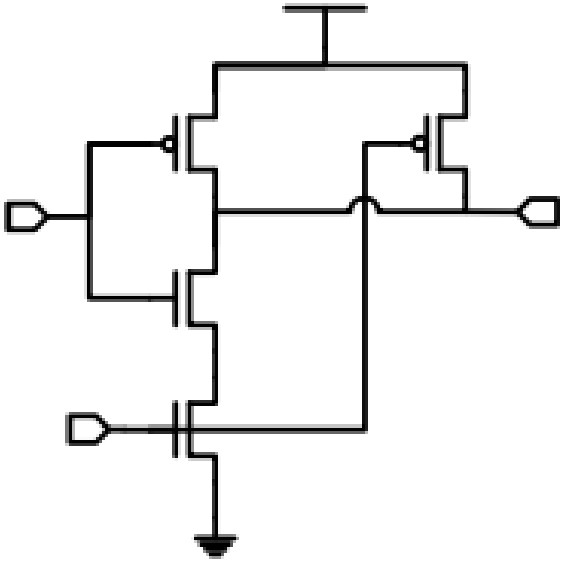
Classic CMOS

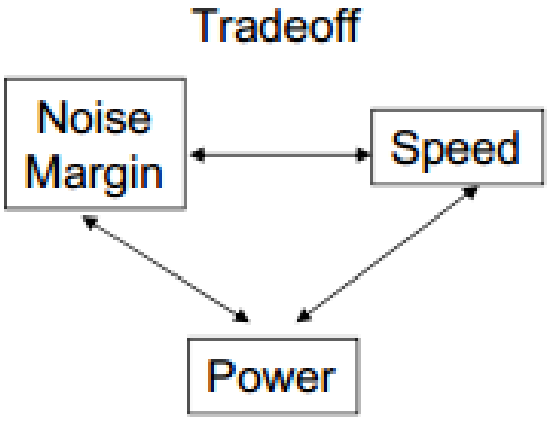
- Advantages:
  - Non-ratioed
  - ~0 static power
  - Low S.C. power ~ 10% of dynamic power
  - Full rail swing
  - Good noise margins
  - True and complement functions



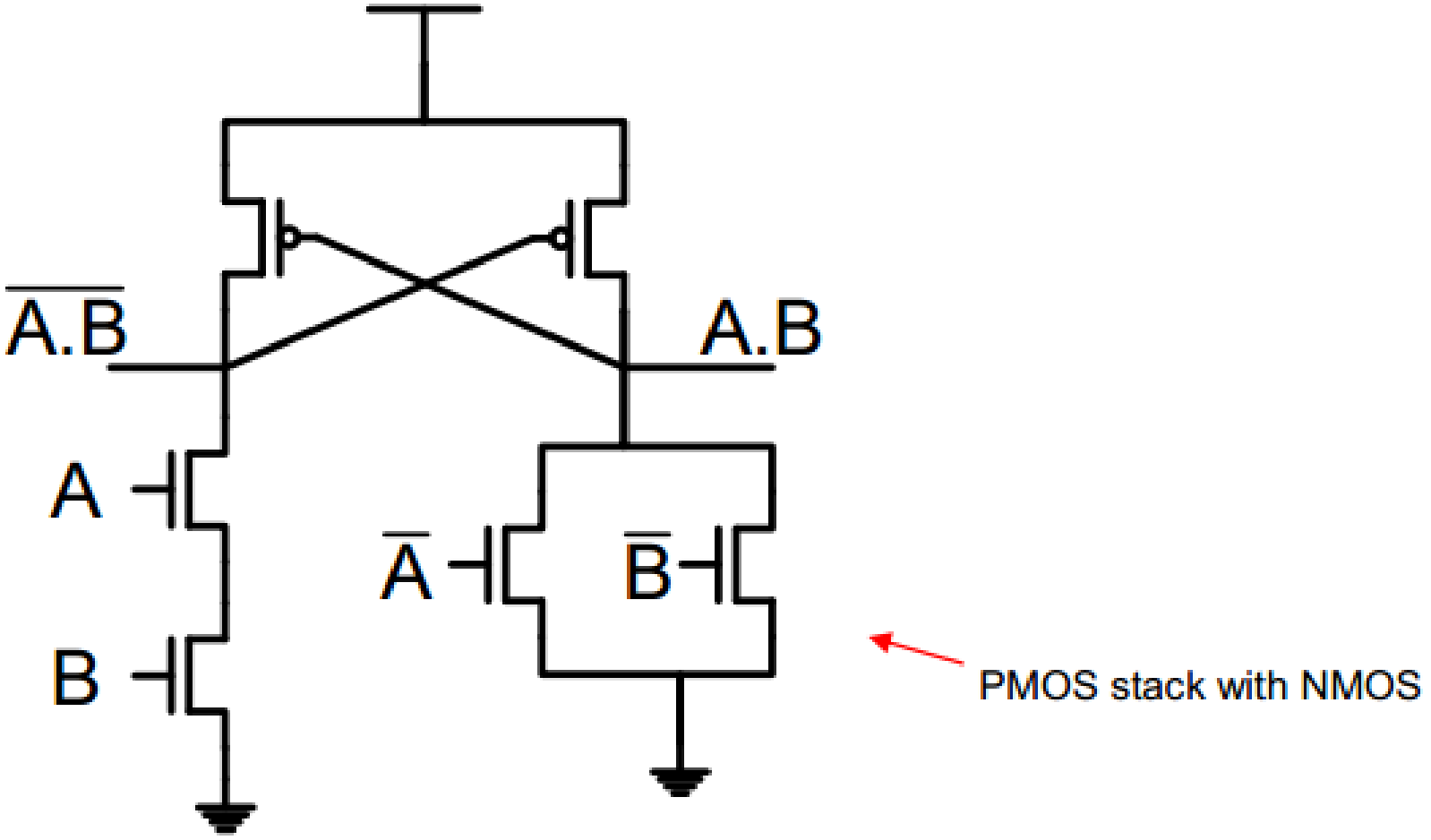
Classic CMOS

- Disadvantages:
  - Large # of transistors, large area
  - Slow
    - PMOS mobility
    - Transistor cap from dual function
  - Increasing static power due to leakage

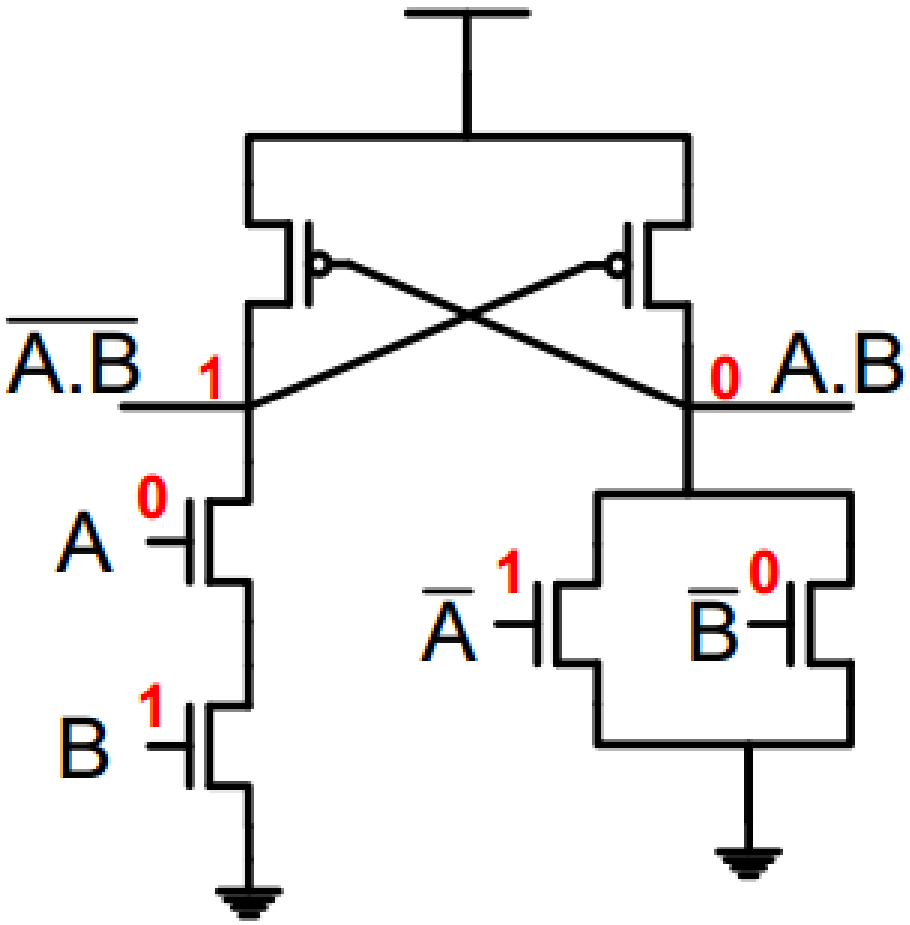




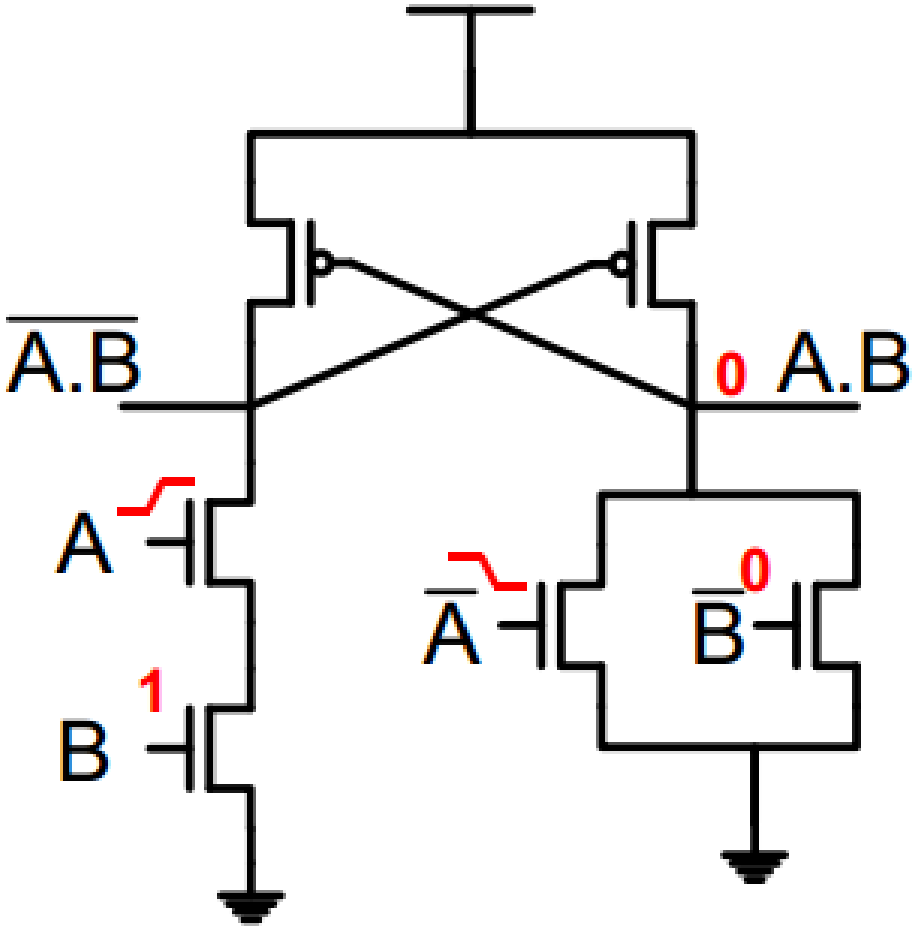
Differential Cascode Voltage Switch DCVS



Differential Cascode Voltage Switch DCVS



Differential Cascode Voltage Switch DCVS



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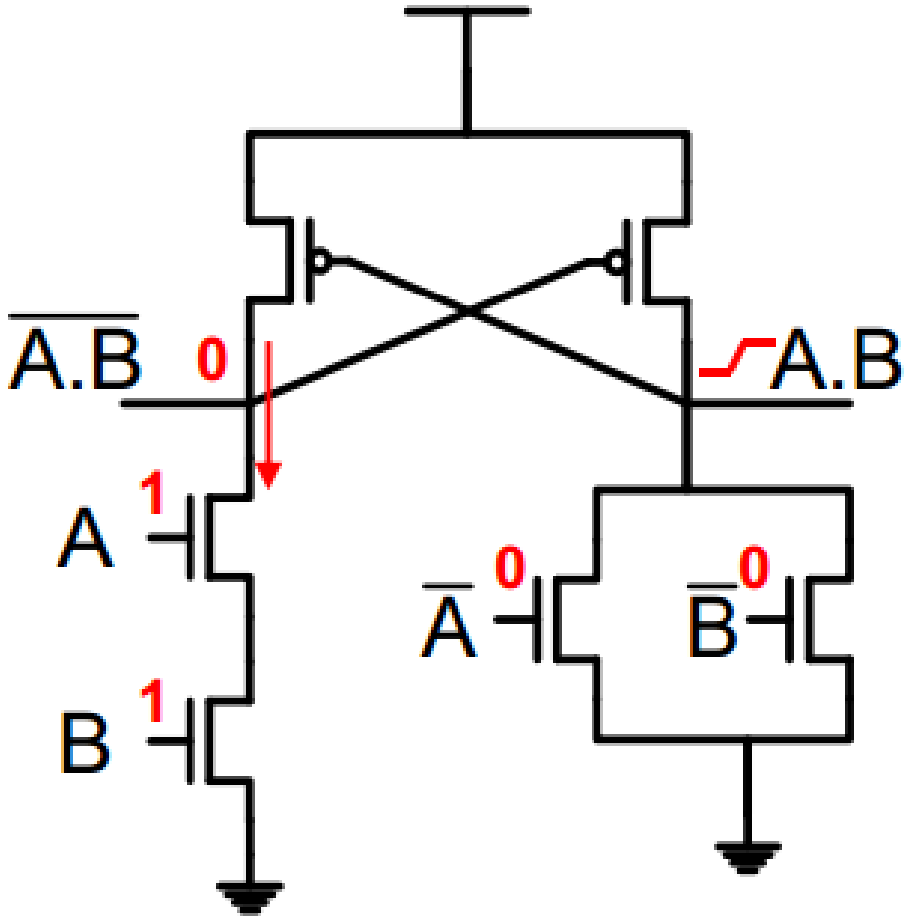
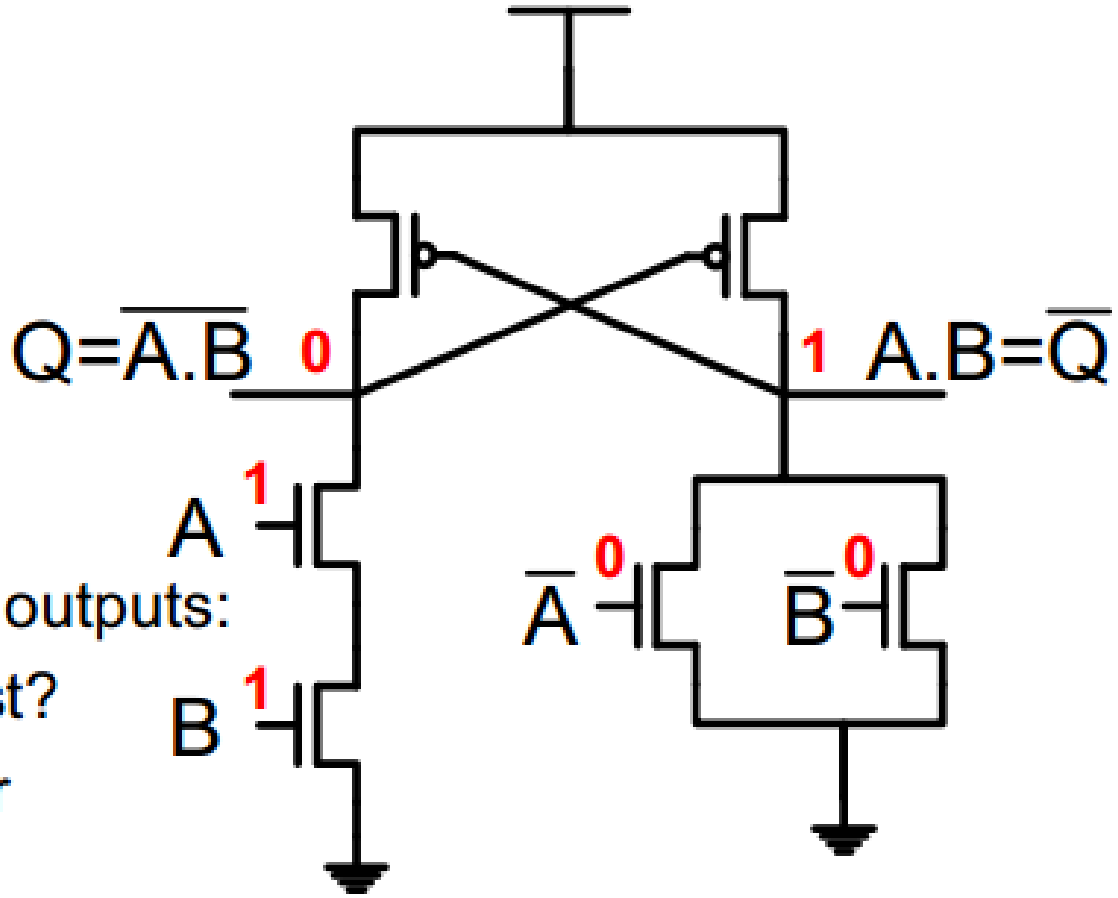


Differential Cascode Voltage Switch DCVS

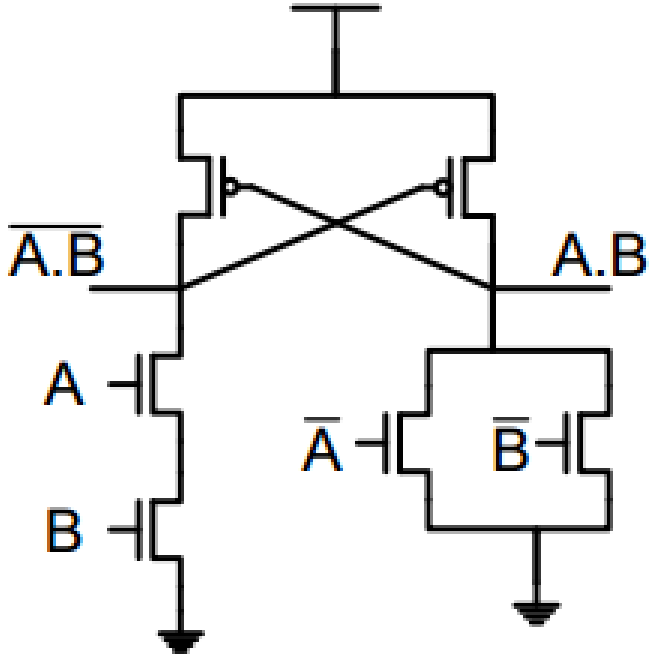


Timing of outputs:

Which first?

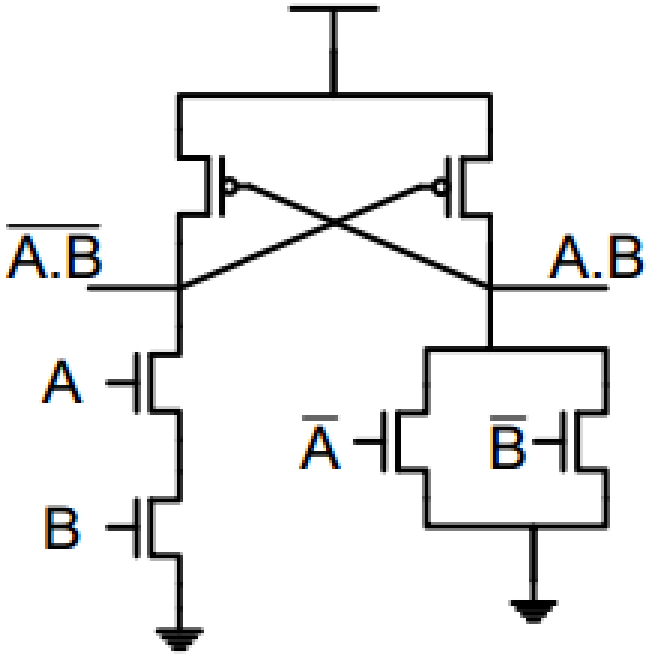
Q or Qbar

Differential Cascode Voltage Switch DCVS



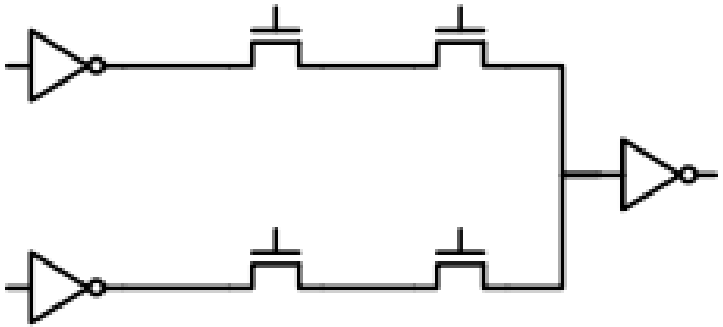
- Advantages:
  - No PMOS duality
    - Lower input cap.
    - Use only NMOS
  - Faster than CMOS
  - Can evaluate complex logic trees in 1 stage

Differential Cascode Voltage Switch DCVS



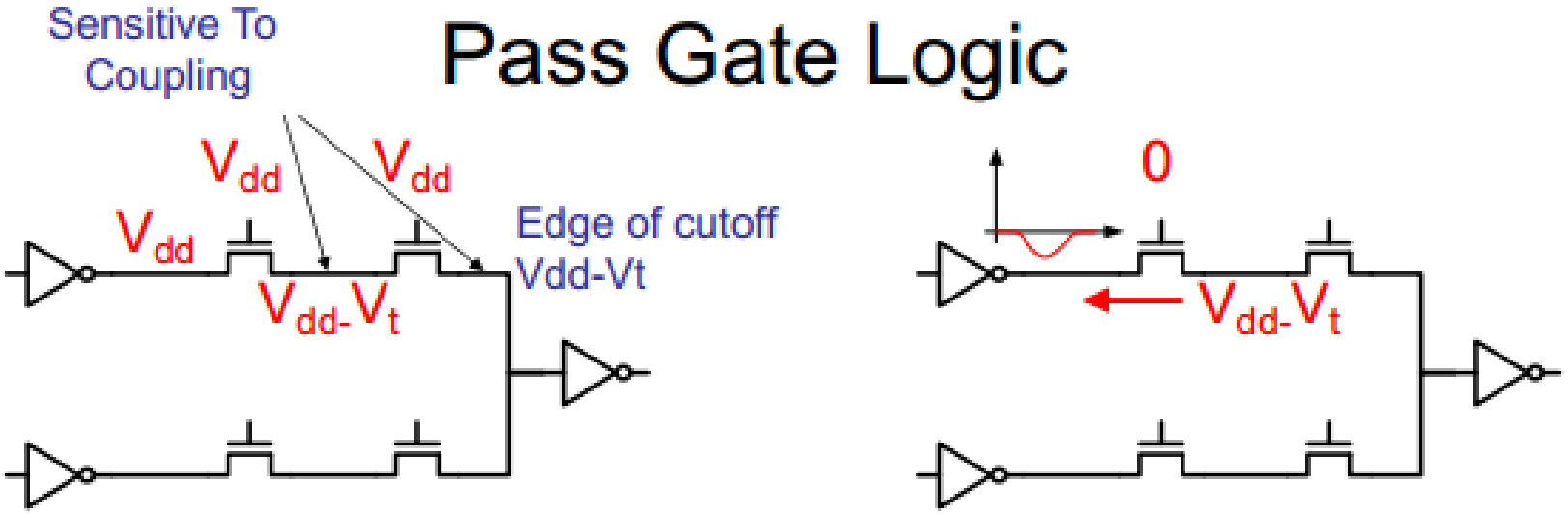
- Disadvantages:
  - Need complementary inputs (dual rail)
  - Cross-bar current
    - Sensitive to input timing
  - Sizing of PMOS is hard
    - Too large → PDN does not switch the output
    - Too small → Slow rise time
- Ratioed Logic?

Pass Gate Logic



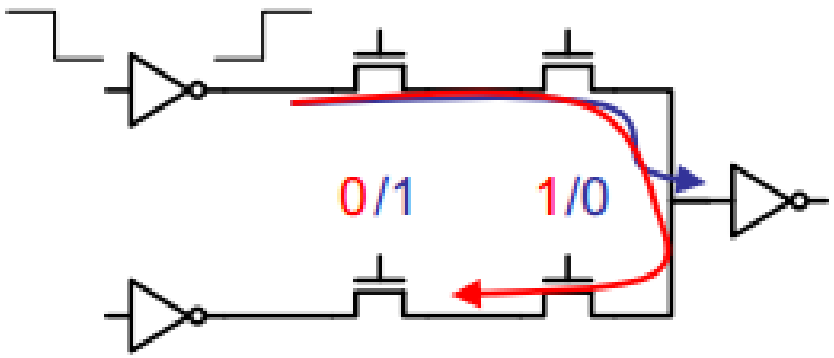
- Advantages:
  - Speed: 20-50% faster (less capacitance)
    - In some circuits, such as XOR/MUX
  - Lower dynamic power

Pass Gate Logic



- Disadvantages:
  - Very sensitive to noise: 2 types
    - Vt drop → must level restore someplace
    - Sensitive to undershot voltage noise on inputs
      - Buffers at inputs suppresses this effect
  - Body effect → limit # of FETs in series

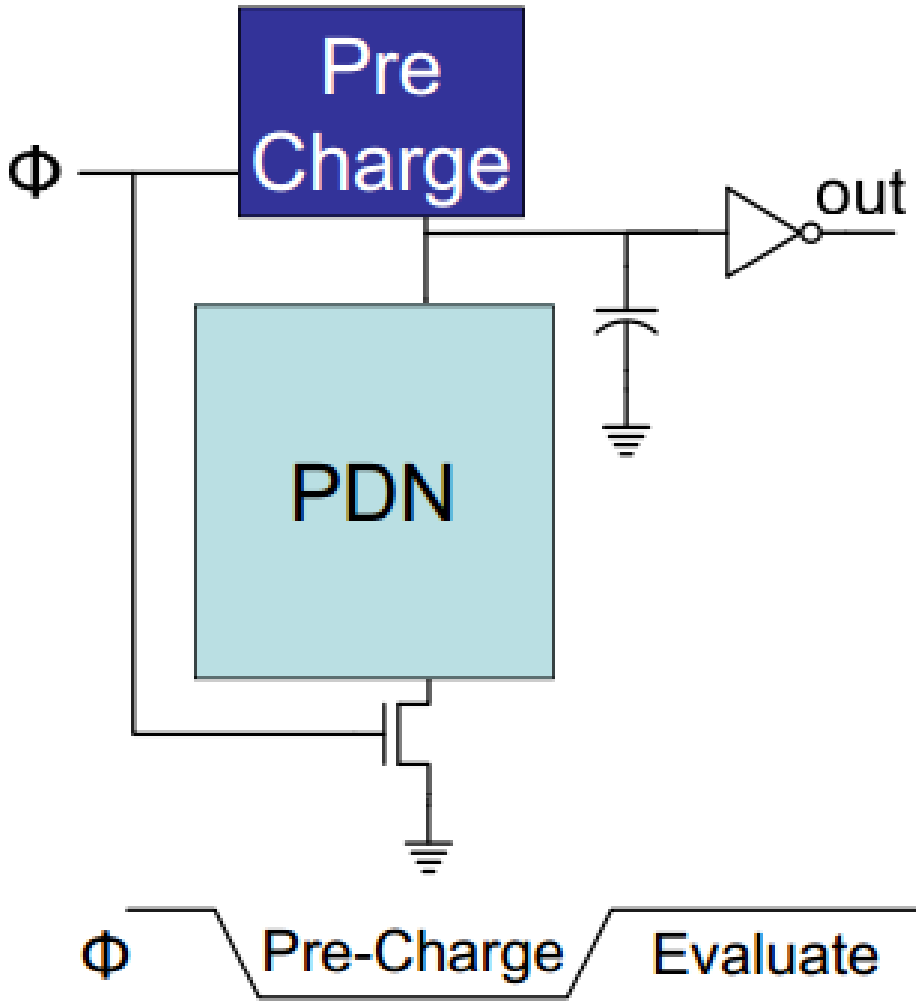
Pass Gate Logic



- Disadvantages:
  - Delay dependence on state
  - Cannot be cascaded without output inverter
  - Added leakage in output inverter

Dynamic Logic Families

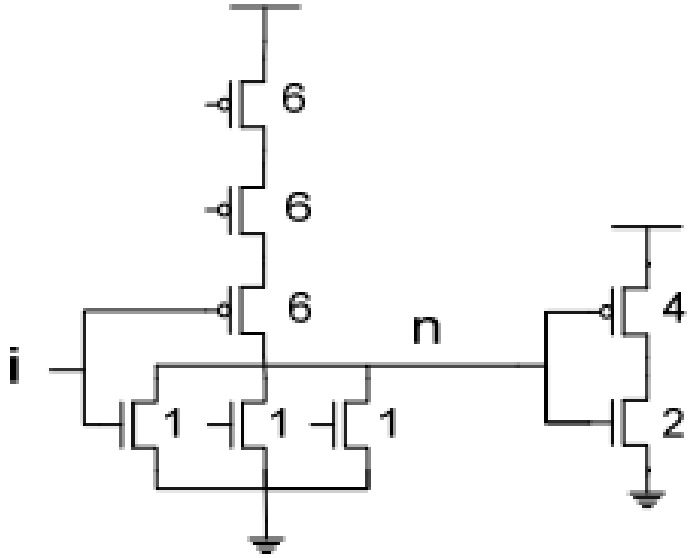
Basic Domino gate

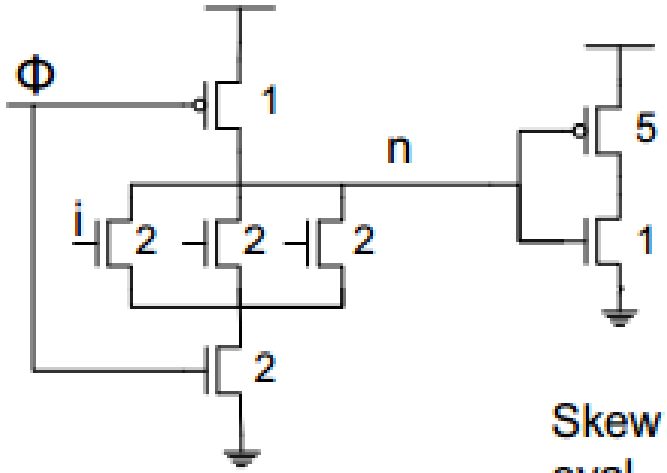


- Divide the clock in 2 phases:
  - Precharge
    - Output Low
    - Dyn. Cap precharge
    - PDN Off
  - Evaluate
    - Conditional discharge
    - Input must be stable and monotonic L→H

Domino / Static C_{in}/C_{out}

3-input OR gate



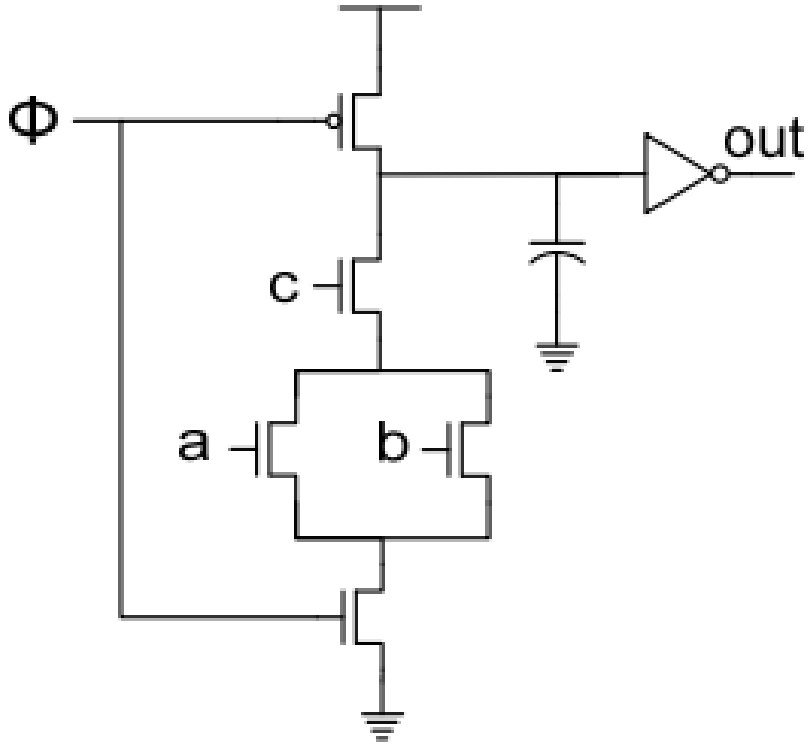


Skew for eval

Static:
$C_i = 7$
$C_n = 9$

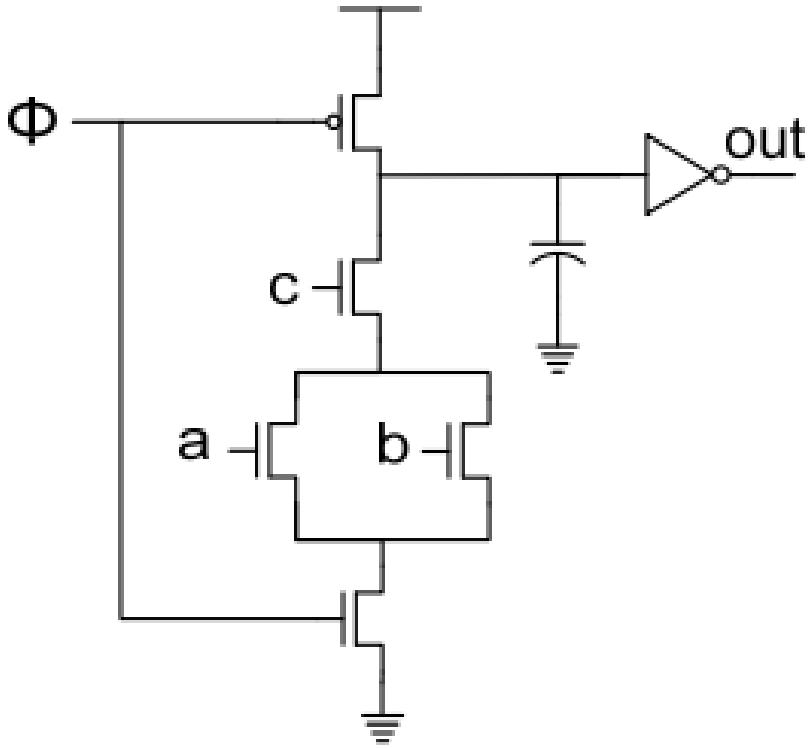
Dynamic:
$C_i = 2$
$C_n = 7$

Basic Domino gate



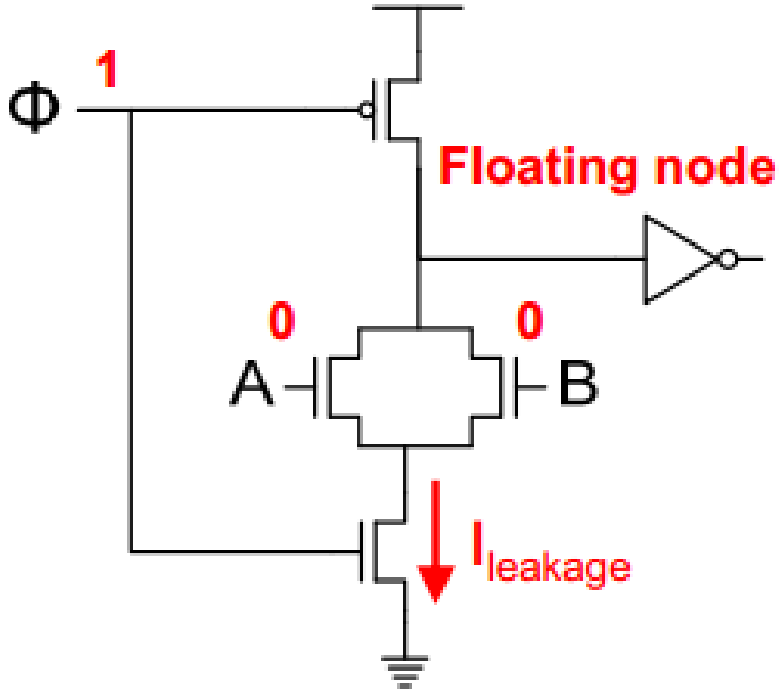
- Advantages:
  - Faster than CMOS
  - Input capacitance is lower
  - Early switch point
  - Inverter P/N > 2 (only rising delay important)

Basic Domino gate



- Disadvantages:
  - Low noise margin
  - Charge sharing
  - Leakage currents
  - Internal capacitance charge sensitive to noise

Issues: Leakage



- Dynamic node is floating during evaluation
  - Leakage current of NMOS can discharge it