Digital Integrated Circuits – EECS 312

http://ziyang.eecs.umich.edu/~dickrp/eecs312/

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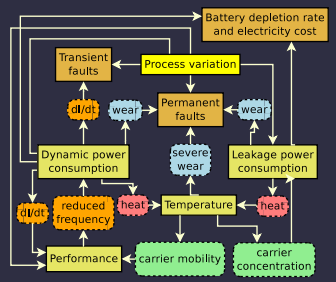
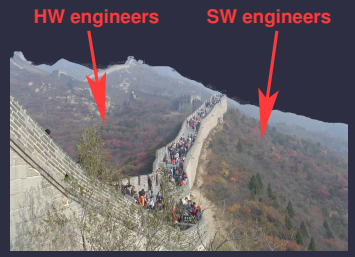
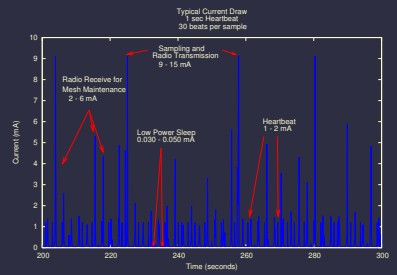
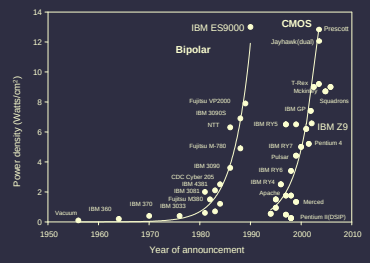
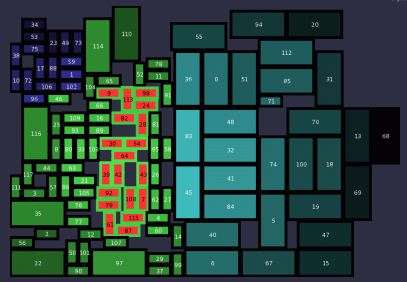










Review

- Design a non-trivial logic gate.
- What happens to inverter delay as the driving MOSFET widths are increased?
- What happens to inverter delay as the driven MOSFET widths are increased?
- What impact does non-instantaneous rise/fall time have on the propagation delay for the subsequent logic stage?

Lab 3

- Input inverters.
- Implications of sizing on energy consumption.

Derive and explain.

Short talks

Speakers and topics

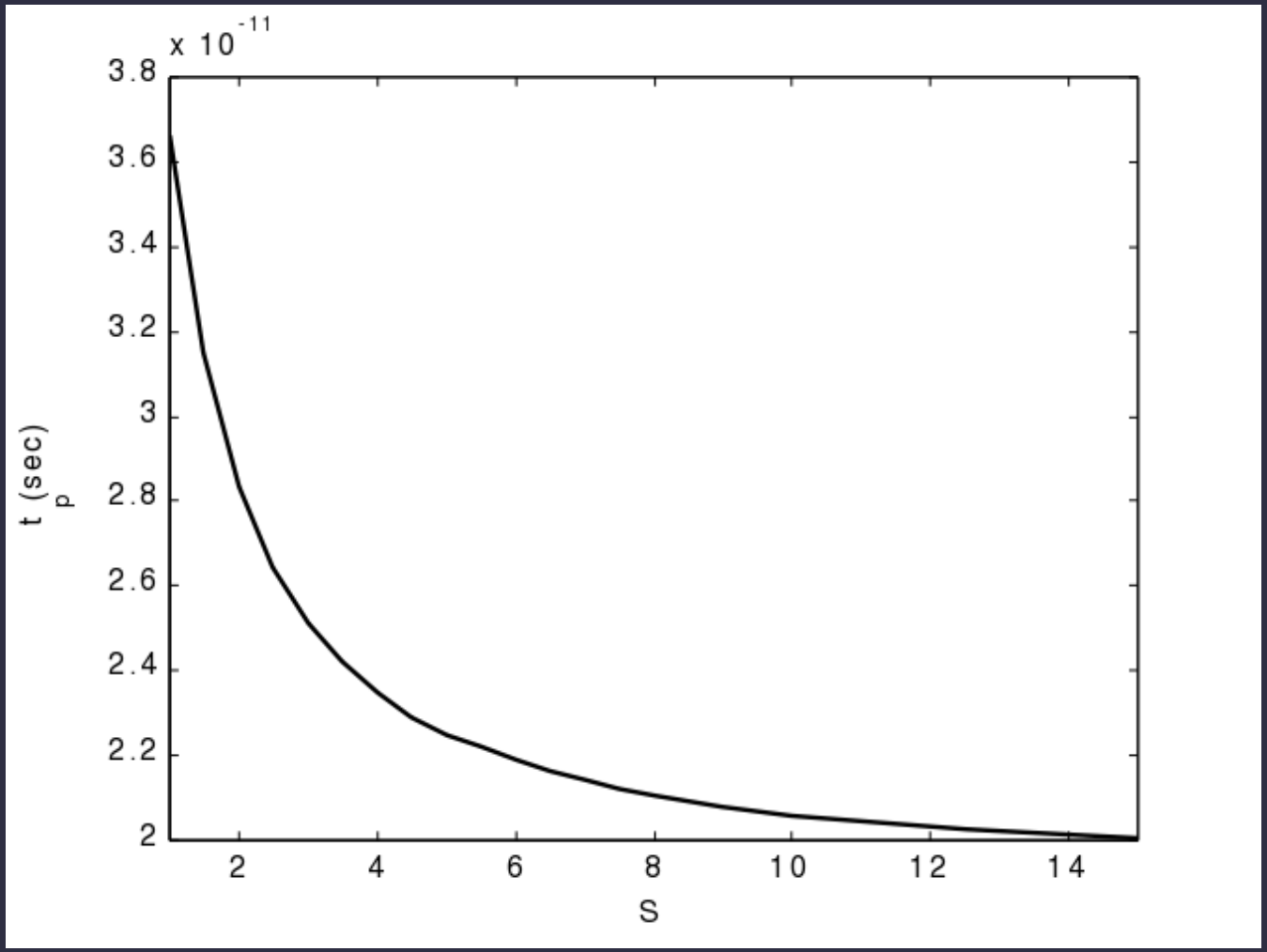
1. Katherine, Olga, and Matt: Atomic layer deposition.
2. Michael and Heesung: Impact of materials on devices and circuits.
3. Haishan and Guanyu: Optical interconnect.
4. Ike and Dan: ALU design alternatives.
5. Tyler and Megan: Subthreshold circuit applications.
6. Sui Yu, Zhenghong, and Wang Yi: FinFETs.

- First talk: 4 November, Thursday.
- Order?

Lecture plan

1. Inverter sizing
2. Homework

Dependence of delay on width (R)



- Fix $R_L C_L$ and vary W.
- Eventually, self-loading dominates.

Inverter chain delay optimization

Given

- Size (width) of first inverter in chain,
- Driven load,
- Transistors are minimal length, and
- $W_p/W_n = 2$ approximately balances t_{pHL} and t_{pLH}.

Find

- Optimal number of inverters in chain and
- Optimal size (width) of each inverter

to minimize chain delay.

Intuition

- Given two inverters (first fixed) and a large load (C_L), how should the second be sized to minimize delay?
- $C_{G2} = C_{G1}$ (minimal)?
- $C_{G2} > C_L$?
- $C_{G2} = C_L$?
- Some other setting?
- Why?

Derivation I

$$\text{Let } W = W_n = W_p/2$$
$$R = R_p = R_n$$
$$T_{pHL} = T_{pLH} = 0.69RC_L$$
$$C_i = 3\frac{W_{i+1}}{W_{unit}}C_{unit}$$
$$t_p = kR(C_{int} + C_L) = kRC_{int} + kRC_L$$

Derivation II

Consider the impact of scaling factor S.

$$t_p = 0.69\left(\frac{R}{S}SC_{int}\left(1+\frac{C_L}{SC_{int}}\right)\right)$$

$$t_p = 0.69RC_{int}\left(1+\frac{C_L}{SC_{int}}\right)$$

$$t_p = t_{p0}\left(1+\frac{C_L}{SC_{int}}\right)$$

t_{p0}: Intrinsic delay.

- Scaling doesn't impact intrinsic delay.
- Scaling does impact total delay.
- $t_p \rightarrow t_{p0}$ as $S \rightarrow \infty$.
- Diminishing returns with increasing S.

Consider chain of inverters I

$$t_{p,chain} = t_{p1} + t_{p2} + \cdots + t_{pn}$$

$$t_{pi} \approx RC\left(1 + \frac{C_{g,i+1}}{\gamma C_{g,i}}\right)$$

$$t_{p,chain} = \sum_{i=1}^{N} t_{pi}$$

$$t_{p,chain} = t_{p0} \sum_{i=1}^{N}\left(1 + \frac{C_{g,i+1}}{\gamma C_{g,i}}\right)$$

Given that

$$C_{g,N+1} = C_L$$

Consider chain of inverters II

and

$$\gamma = \frac{C_{int}}{C_g} \approx 1 \text{ (technology-dependent constant).}$$

Sketch of derivation

- For each i, find $\sigma t_{p,chain} / \sigma C_{g,i}$.
- Solve for $\sigma t_{p,chain} / \sigma C_{g,i} = 0, \forall_{i=1} N$.
- Result is $\frac{C_{g,i+1}}{C_{g,i}} = \frac{C_{g,i}}{C_{g,i-1}}$.
- Each stage size geometric mean of previous and next: $C_{g,i} = \sqrt{C_{g,i-1} C_{g,i+1}}$.
- Constant factor relates sizing of all adjacent gate pairs.
- Each stage has same delay.

Sizing for optimal inverter chain delay

- Optimal stage-wise sizing factor: $\sqrt[N]{\frac{C_L}{C_{g,1}}}$.
- Minimum path delay: $t_{p,chain} = N t_{p0} \left(1 + \sqrt[N]{\frac{C_L}{C_{g,1}}}/\gamma\right)$

Example of inverter sizing

Given

- $C_L = 16C_1$.
- $N = 4$.

Per-stage scaling factor: $\sqrt[4]{16C_1/C_1} = 2$

Optimizing N I

Let

$$\Phi = \frac{C_L}{C_{g,1}}$$

$$t_{p,chain} = N t_{p0} \left(1 + \frac{\sqrt[N]{\Phi}}{\gamma} \right)$$

$$t_{p,chain} \frac{d}{dN} = \gamma + \sqrt[N]{\Phi} - \frac{\sqrt[N]{\Phi} \ln(\Phi)}{N}$$

Optimizing N II

Set this to zero.

$$\text{Let } \phi = \sqrt[N]{\Phi}$$

$$0 = \gamma + \phi - \frac{\phi \ln\left(\phi^N\right)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \frac{\ln\left(\phi^N\right)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \frac{N \ln\left(\phi\right)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \ln\left(\phi\right)$$

$$\ln\left(\phi\right) = \frac{\gamma}{\phi} + 1$$

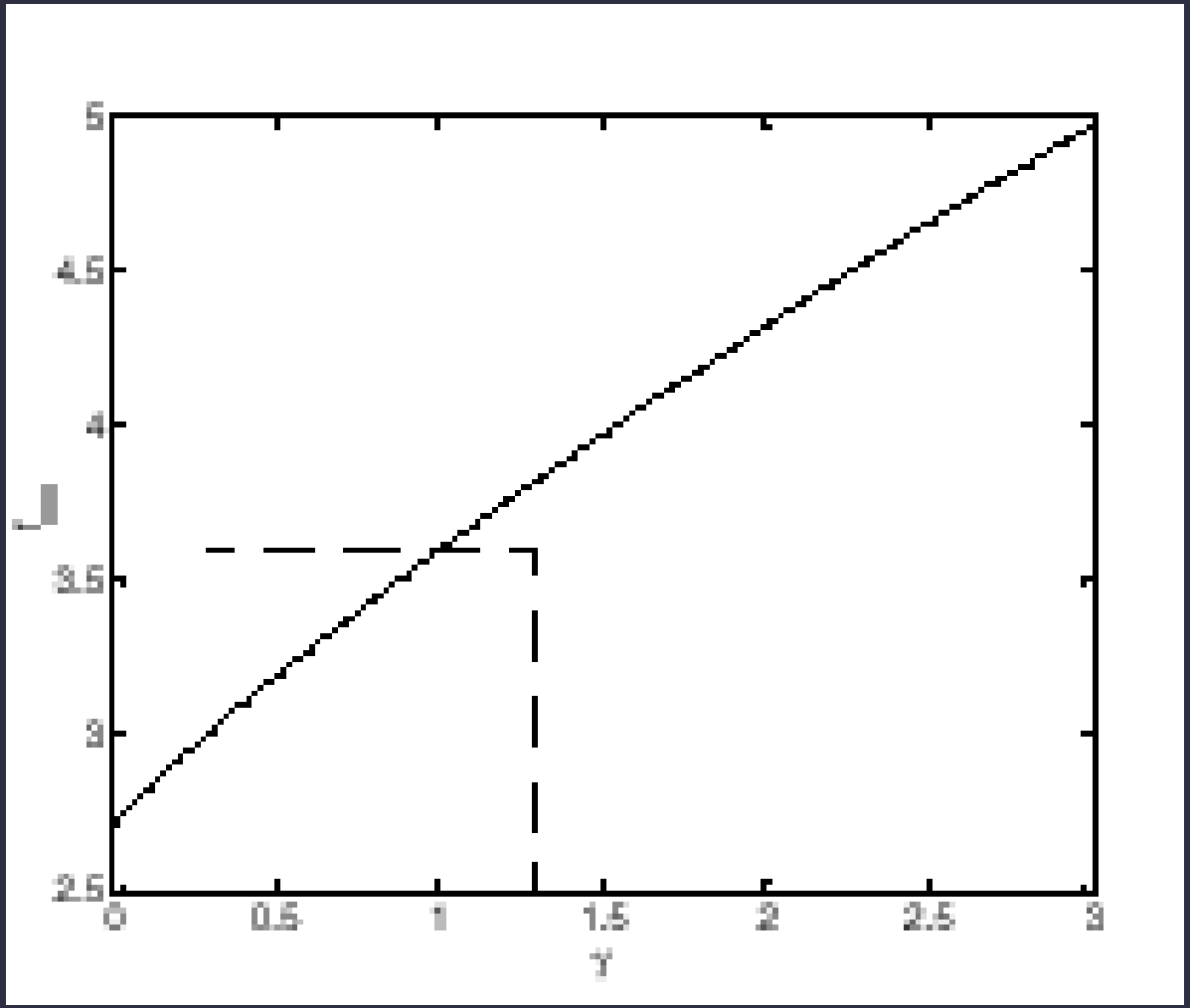
$$\phi = e^{\gamma/\phi + 1}$$

Optimizing N III

Hard to deal with this for $\gamma \neq 0$. Consider implications for $\gamma = 0$.

$$\phi = e$$

Optimal stage sizing factor

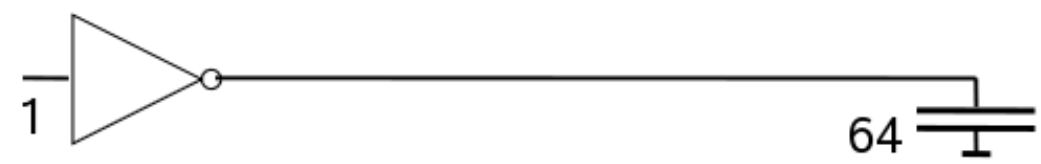


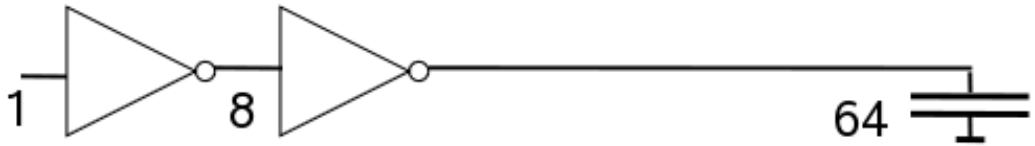
- Optimal tapering factor for $\gamma = 0$: $e \approx 2.7$.
- 3.6 for $\gamma = 1$.

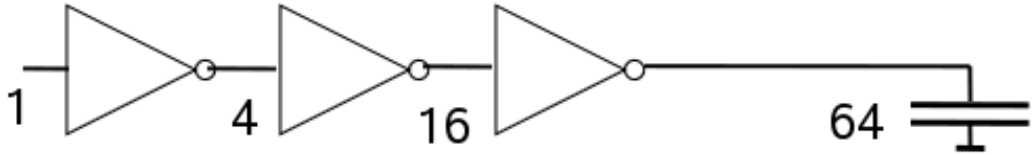
$t_{p,chain}(\Phi)$

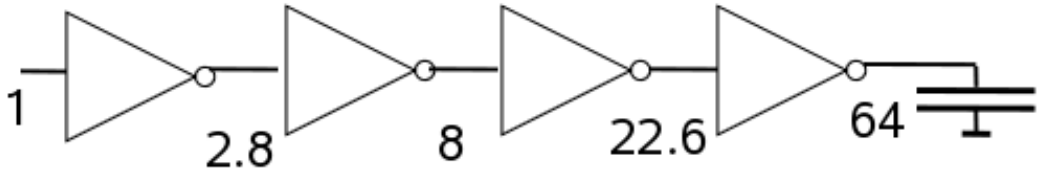
Φ	Unbuffered	$N = 2$	Optimal N
10	11	8.3	8.3
100	101	22	16.5
1,000	1,001	65	24.8
10,000	10,001	202	33.1

Buffering example









N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

Upcoming topics

- Interconnect.
- Alternative logic design styles.

Lecture plan

1. Inverter sizing
2. Homework

Homework assignment

- 2 November, Tuesday: Rest of Lab 3.
- 2 November, Tuesday: Read Sections 4.4.1–4.4.4 and 5.4.3 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003. Don't put off the reading or you might be overloaded when more homework problems are assigned.
- 4 November, Thursday: First short talk.