Digital Integrated Circuits – EECS 312

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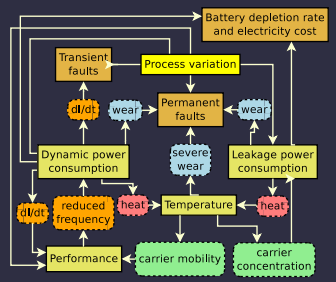
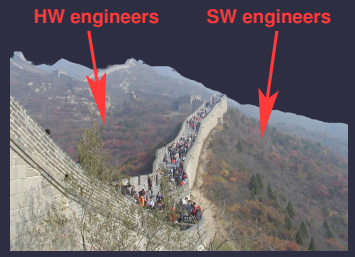
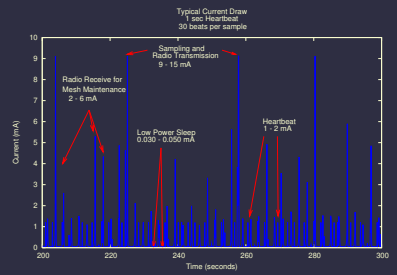
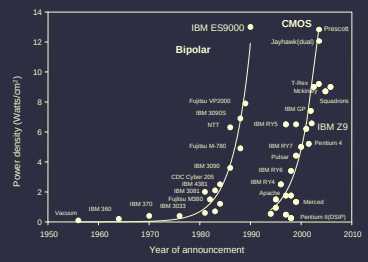
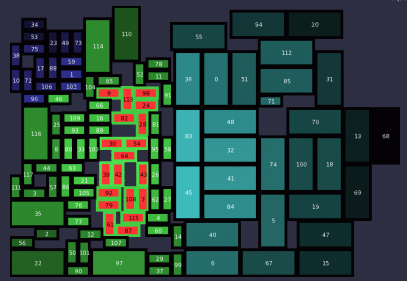










Review

- What are the historical motivations that have driven changes in digital device implementation technologies?
- What is the difference between a combinational and sequential network?
- What substrates (device types) have been used for computation?
- What are the primary advantages of integrated circuits over these competing technologies?

Lecture plan

1. Recent history of digital integrated circuits
2. Digital device requirements
3. Introduction to Cadence tools
4. Homework

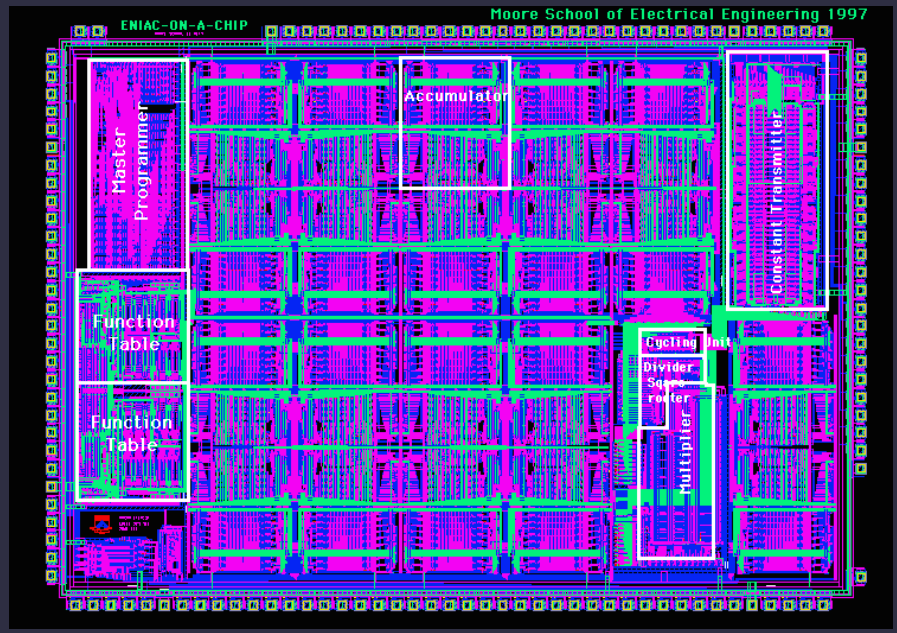
Remember the ENIAC?

- 1946.
- 18,000 vacuum tubes.
- 30 tons.
- 100 kHz.
- Unreliable.

What impact would ICs have on it?

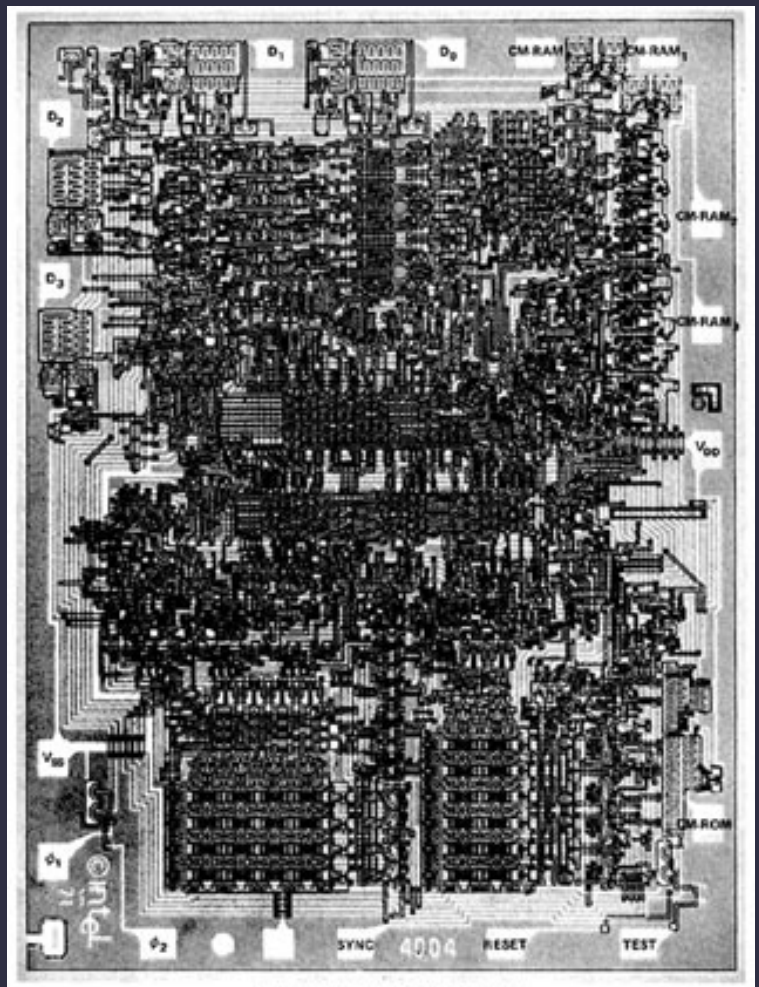
IC ENIAC

- 30 tons $\rightarrow$ 40 mm^2.
- 100 kHz $\rightarrow$ 20 MHz.
- ~~Un~~reliable.



First microprocessor

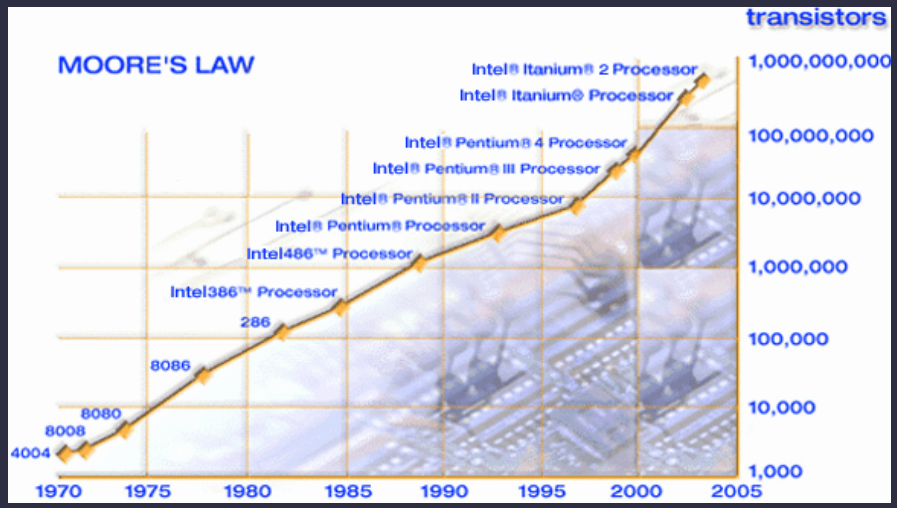
- Intel 4004.
- 1971.
- 2,300 transistors.
- 12 mm^2.
- 740 kHz.
- 12-bit addresses, 8-bit instructions, 4-bit data words.



4004 Photomicrograph With Pin Designations

Trend for one company

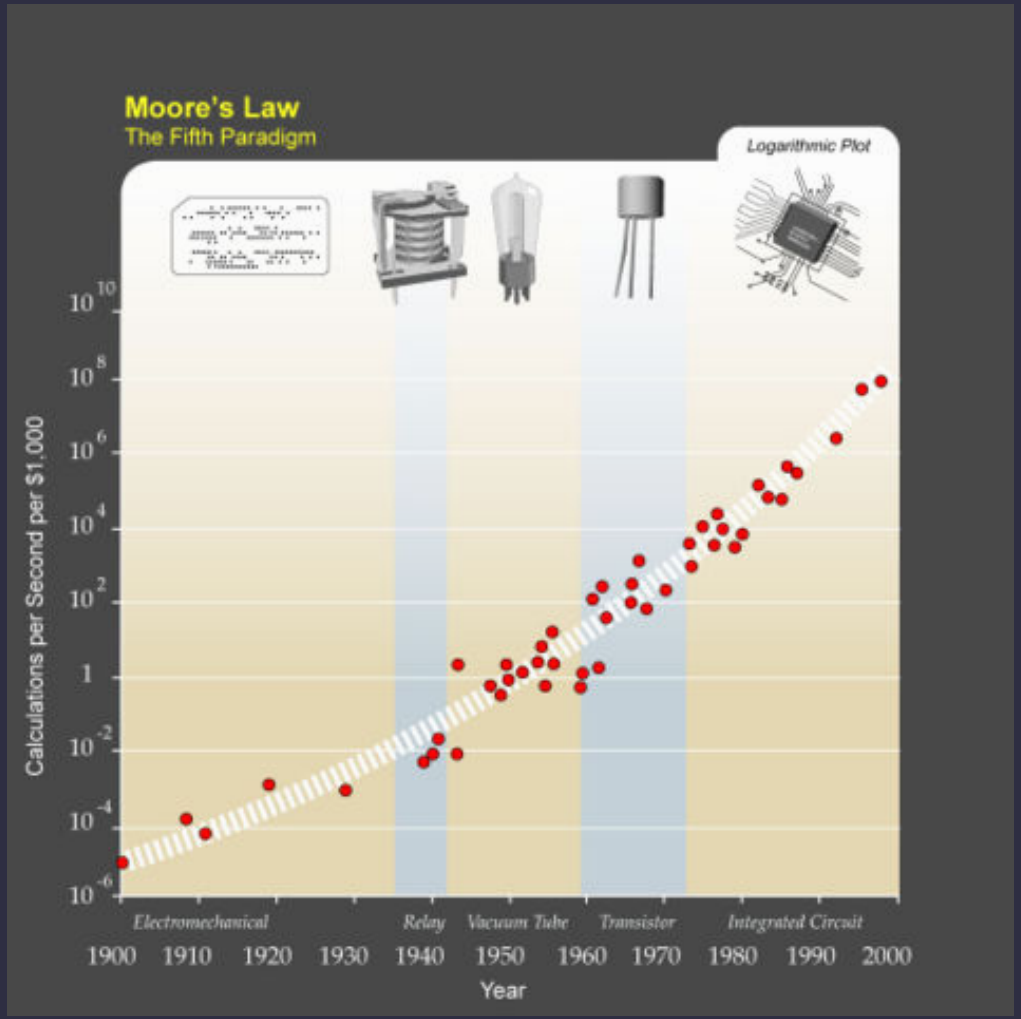
- More than ten generations.
- Datapath: 4 bits $\rightarrow$ 64 bits.
- Frequency: 740 KHz $\rightarrow$ 3 GHz.
- In-order, cache-less $\rightarrow$ Architectural features for common-case performance.
- Uni-processor $\rightarrow$ Chip-multiprocessor (CMP).
- A few thousand transistors $\rightarrow$ Billions of transistors.



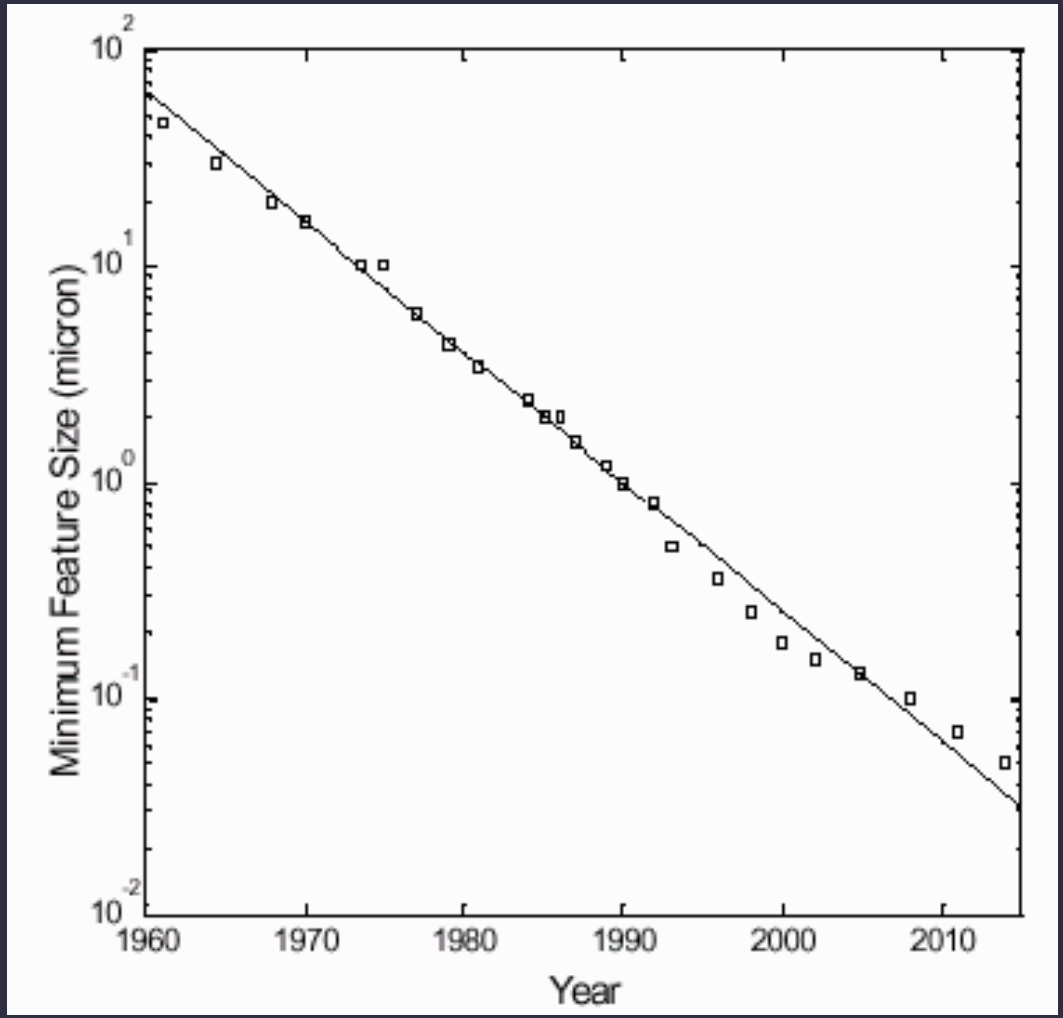
Moore's law

- 1965.
- The number of transistors in an IC doubles every 18–24 months.

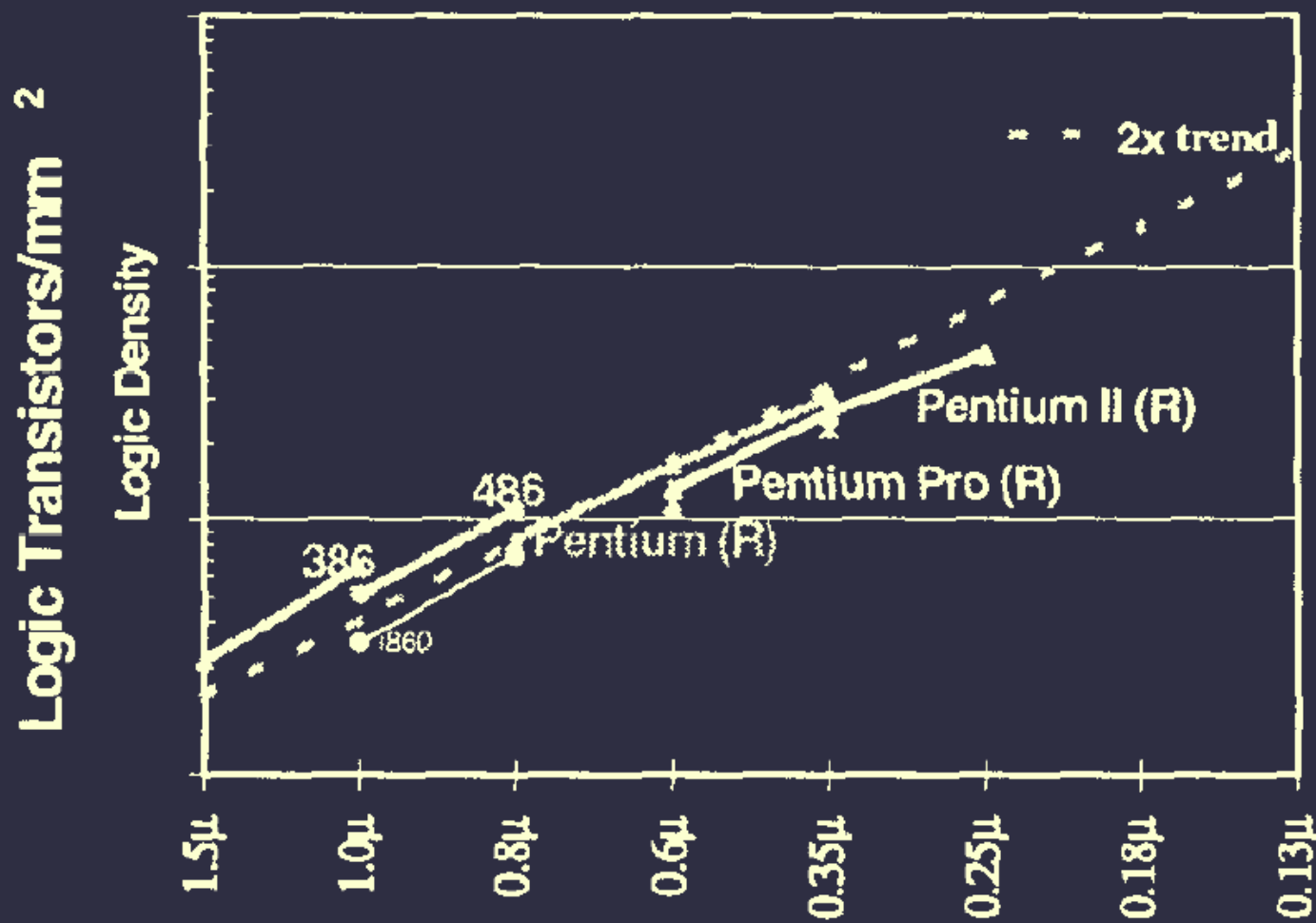
Actual trend



Feature size trends

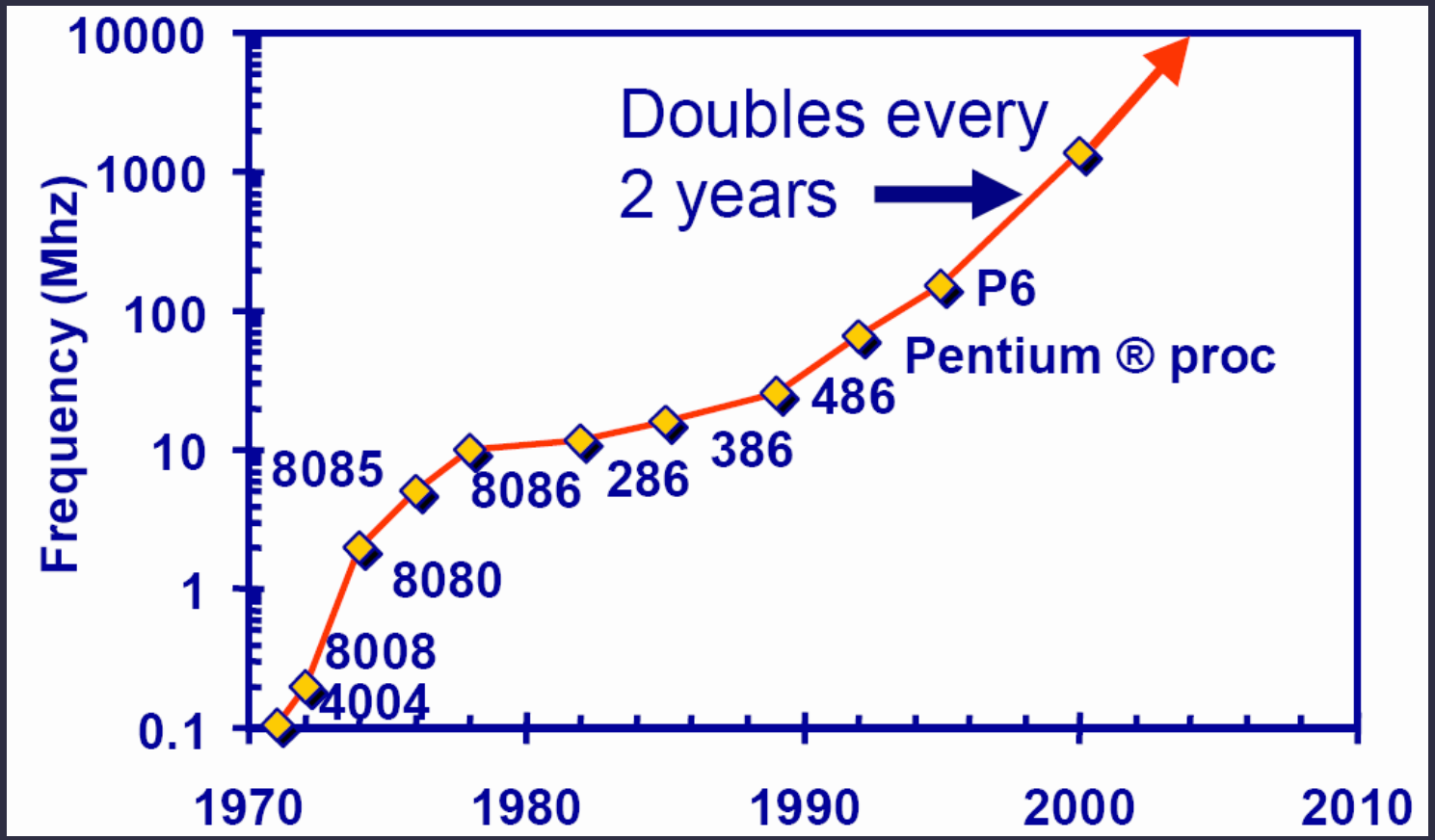


Logic density trends

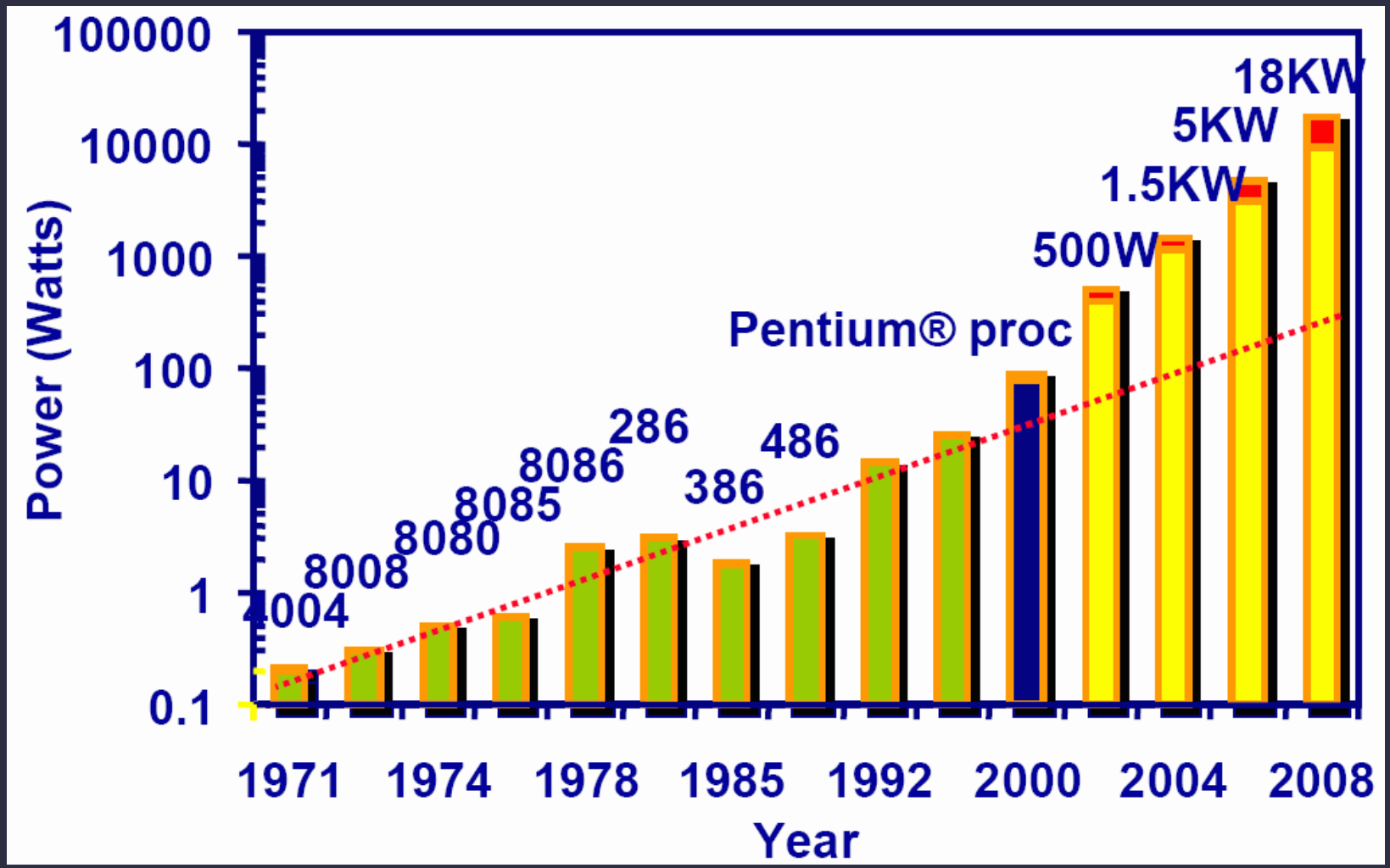


Frequency trends

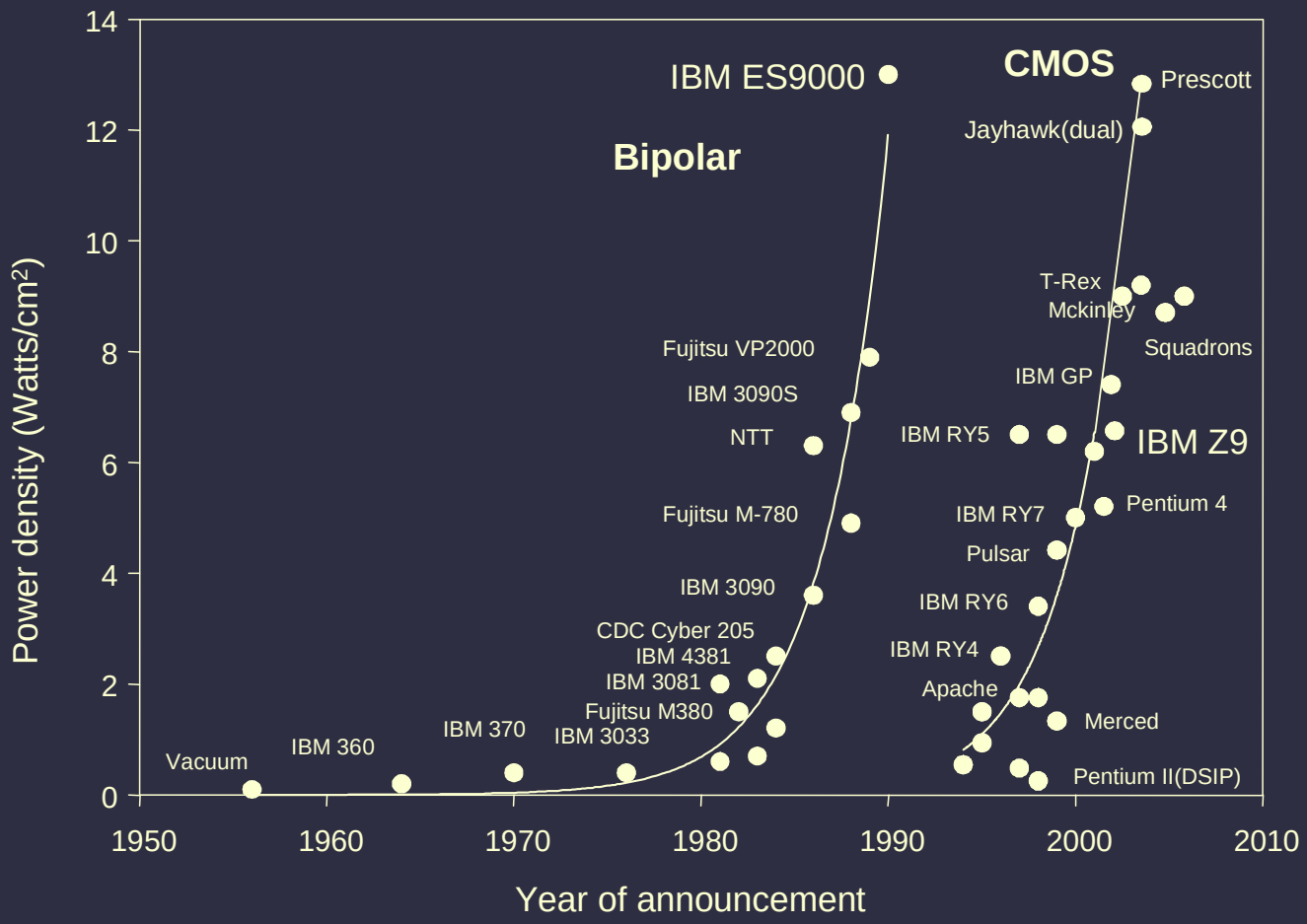
- Technology scaling ↓ delay by 30% and ↑ frequency by 43%.
- Frequency $\propto$ 1/Delay.



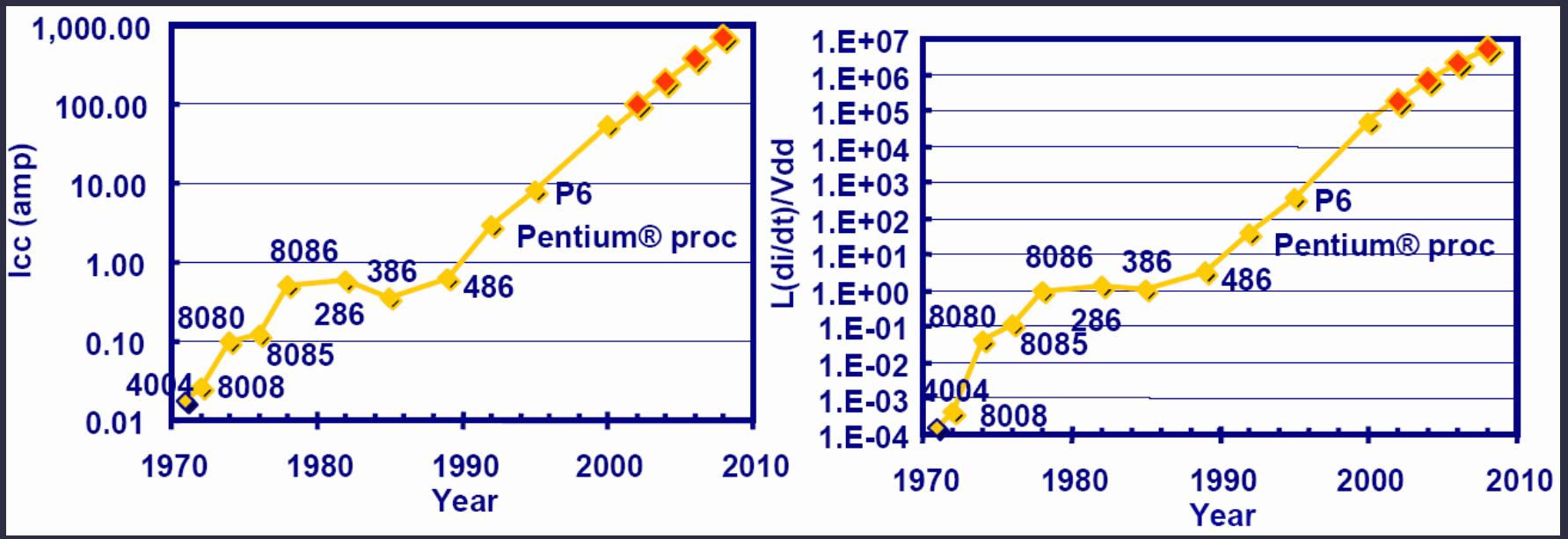
Power trends



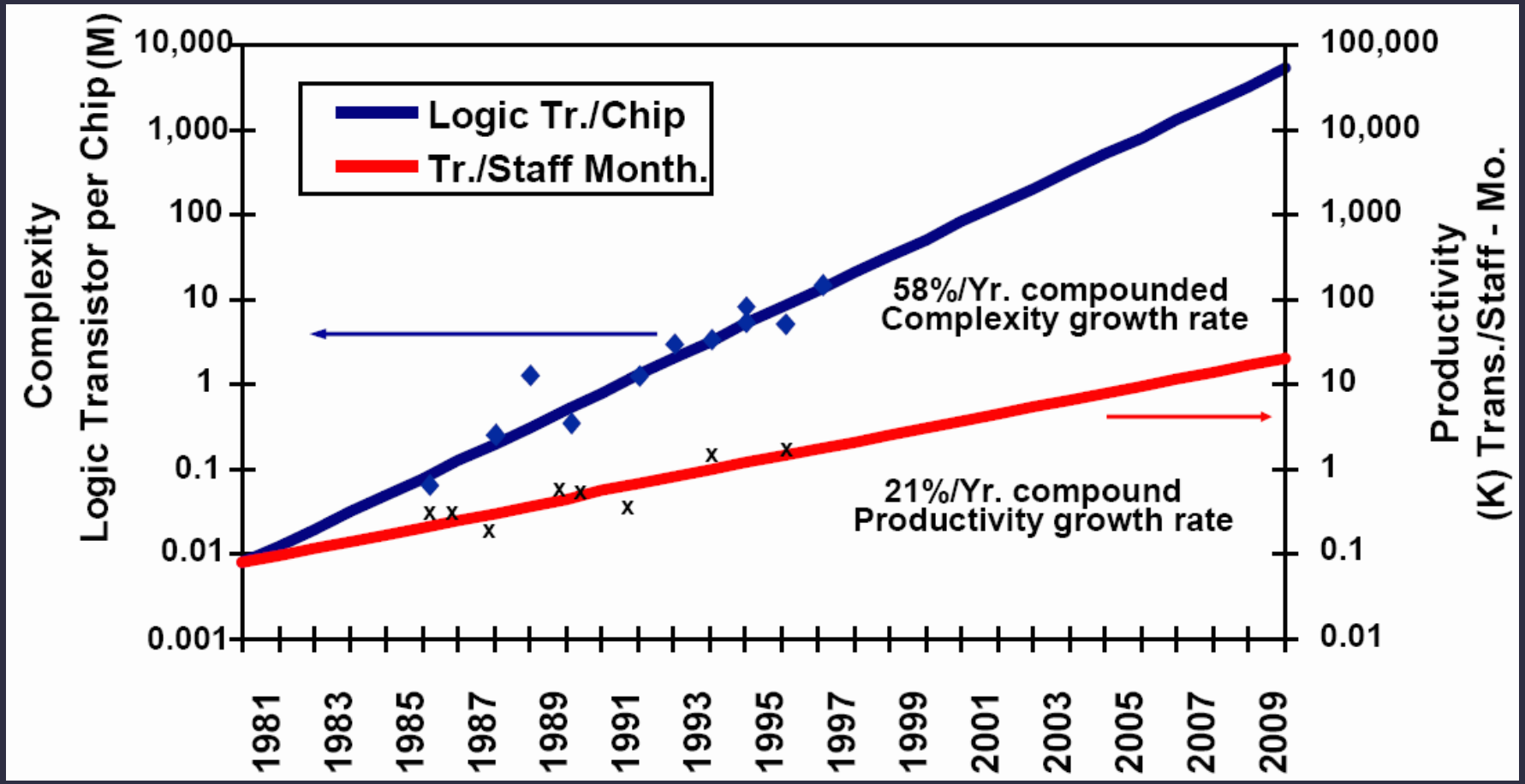
Power density trends



Power supply trends



Productivity trends



Impact of power consumption and temperature

- Early ICs used bipolar transistors (BJT).
- Easier to manufacture reliably, faster.
- In the 1970s, integration densities rose.
- Each bipolar device consumes a lot of power.
- Eventually power became the limiting factor in moving from BJT to MOS devices.
- Currently CMOS dominates.
- Complementary MOS logic.
- Likely to dominate for the next decade.

Power consumption trends

- Initial optimization at transistor level.
- Further research-driven gains at this level difficult.
- Research moved to higher levels, e.g., RTL.
- Trade area for performance and performance for power.
- Clock frequency gains linear.
- Voltage scaling $V_{DD}{}^2$ – important.

Power consumption in synchronous CMOS

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot {V_{DD}}^2 \cdot f \cdot A$$

$$\dagger\ P_{SHORT} = \frac{b}{12}(V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance

V_{DD} : high voltage

f : switching frequency

A : switching activity

b : MOS transistor gain

V_T : threshold voltage

t : rise/fall time of inputs

$\dagger\ P_{SHORT}$ usually $\leq 10\%$ of P_{SWITCH}

Smaller as $V_{DD} \to V_T$

$A < 0.5$ for combinational nodes, 1 for clocked nodes.

Wiring power consumption

- In the past, transistor power $\gg$ wiring power.
- Process scaling $\Rightarrow$ ratio changing.

Other (related) design trends

- Smaller transistors.
- Bigger chips (die).
- Lower power consumption.
- Higher clock frequencies.
- More complex designs.
- Lower voltage.

Other (related) design trends

- Smaller transistors.
- Bigger chips (die).
- Lower power consumption.
- Higher clock frequencies.
- More complex designs.
- Lower voltage.
- More cores.

Some of these trends are slowing.

Current status

- Feature size: 22 nm.
- Integration: 700,000,000 transistors.
- Frequency: 2-4 GHz.
- Power: 100 W.

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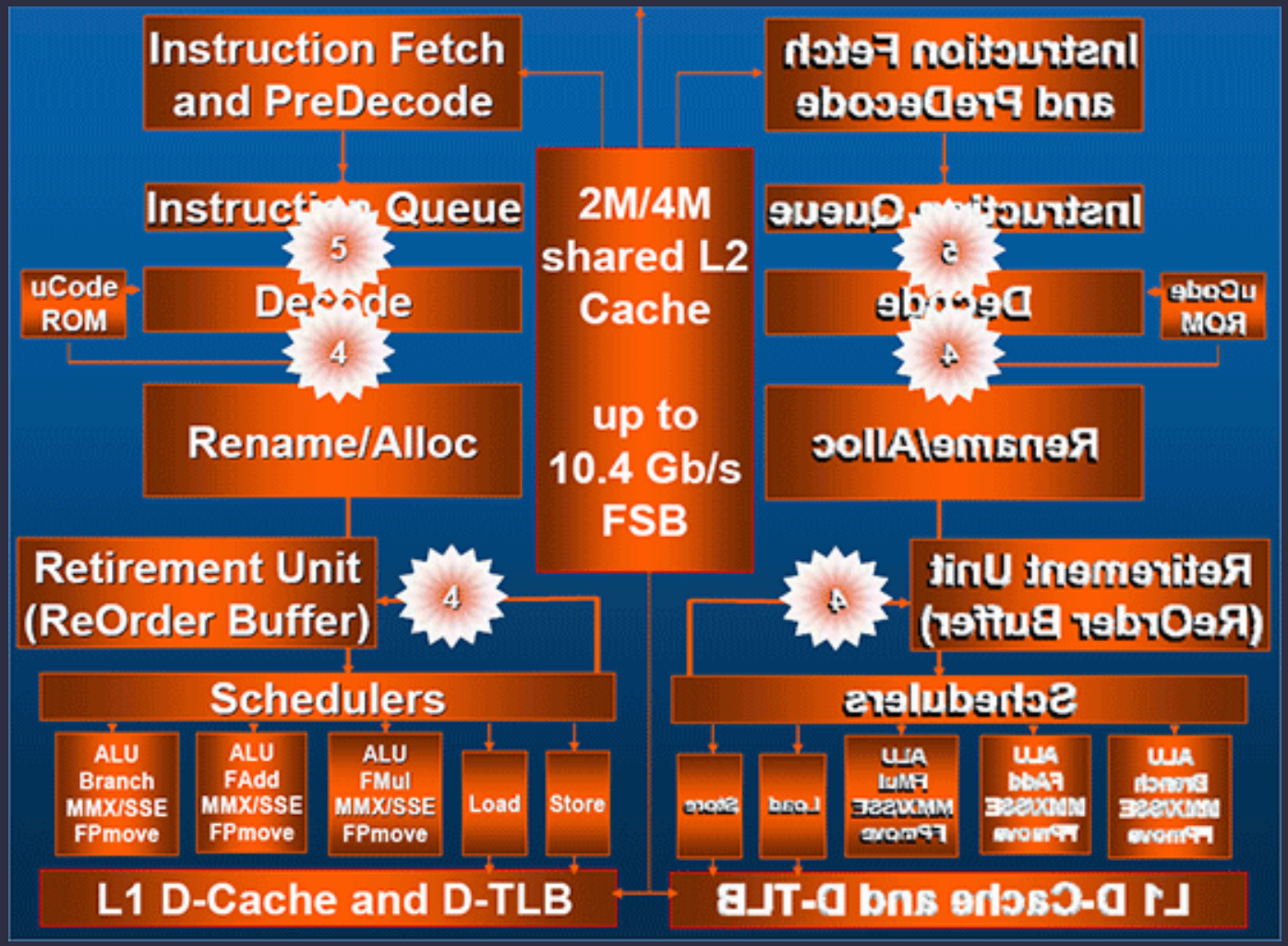
Only two of these characteristics have changes in the past few years.

Multi-core processors



Intel Core 2 Duo

Summary of recent IC history

- Process scaling improves device count, speed.
- Power density increases, eventually limiting further improvements.
- Current move to multi-core.
- Also considering new device technologies, but no clear winners now.

Lecture plan

1. Recent history of digital integrated circuits
2. Digital device requirements
3. Introduction to Cadence tools
4. Homework

Levels of abstraction

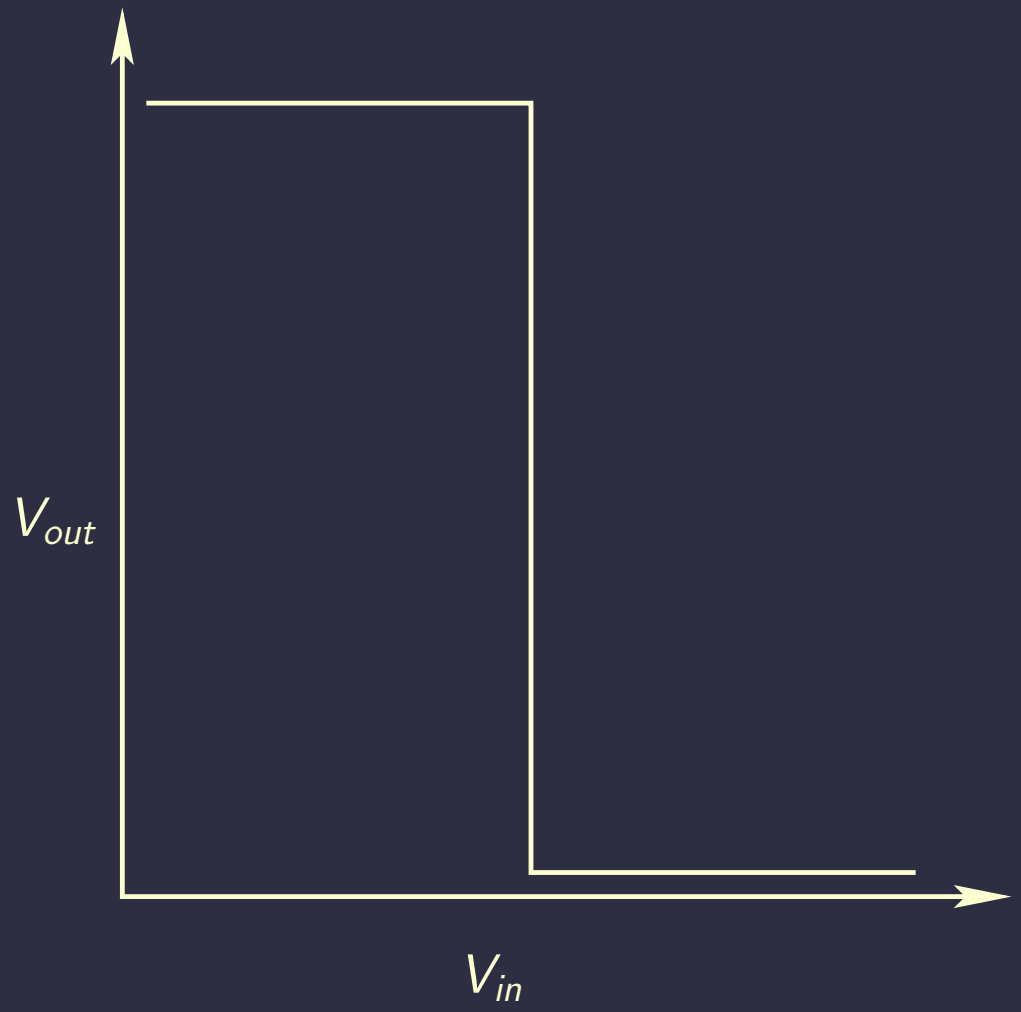
- Hardware–software system.
- Processor.
- Functional unit.
- Logic stage: flip-flop or combinational logic network.
- Gate.
- Transistor or wire.
- Physical material or doping regions.

Derive and explain.

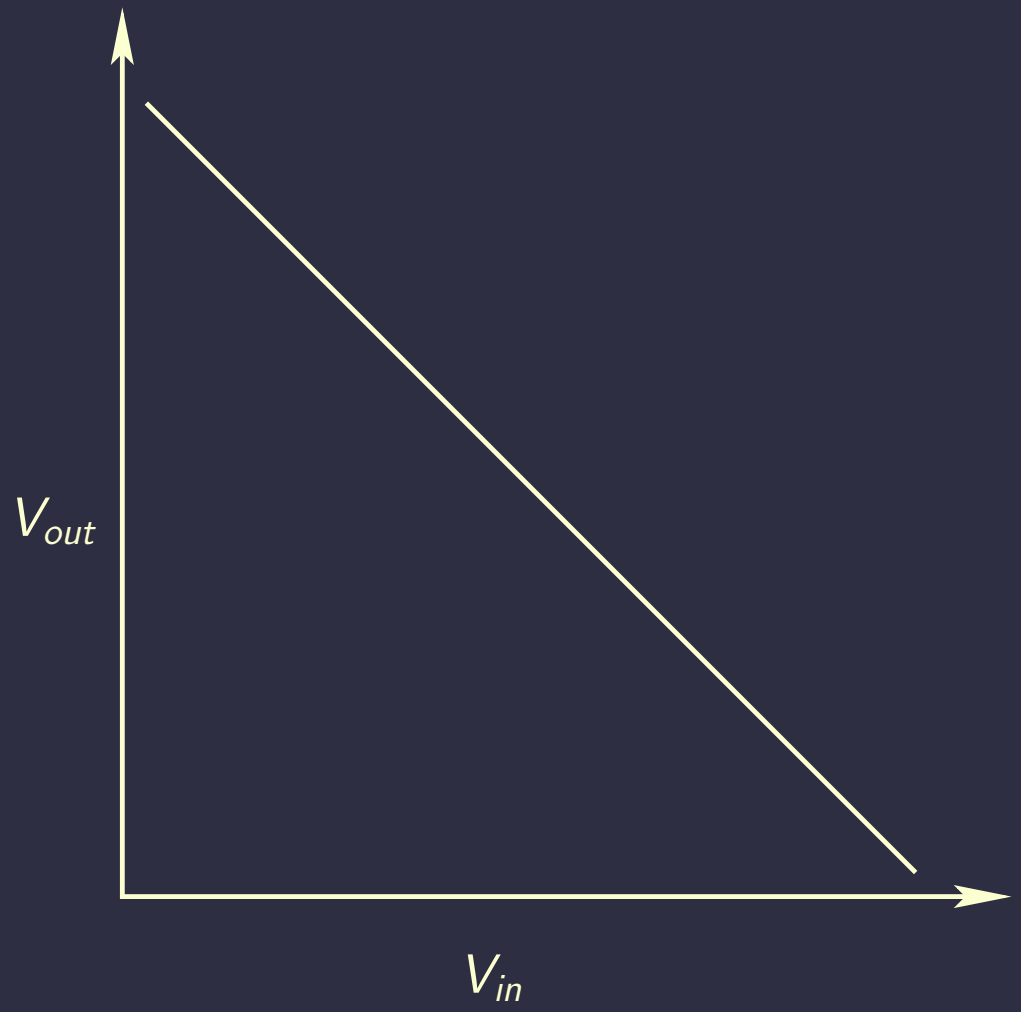
What properties must a "digital" device have?

- What allows us to treat a device as digital, and still have the system work?
- Does this imply certain properties for the transfer function?

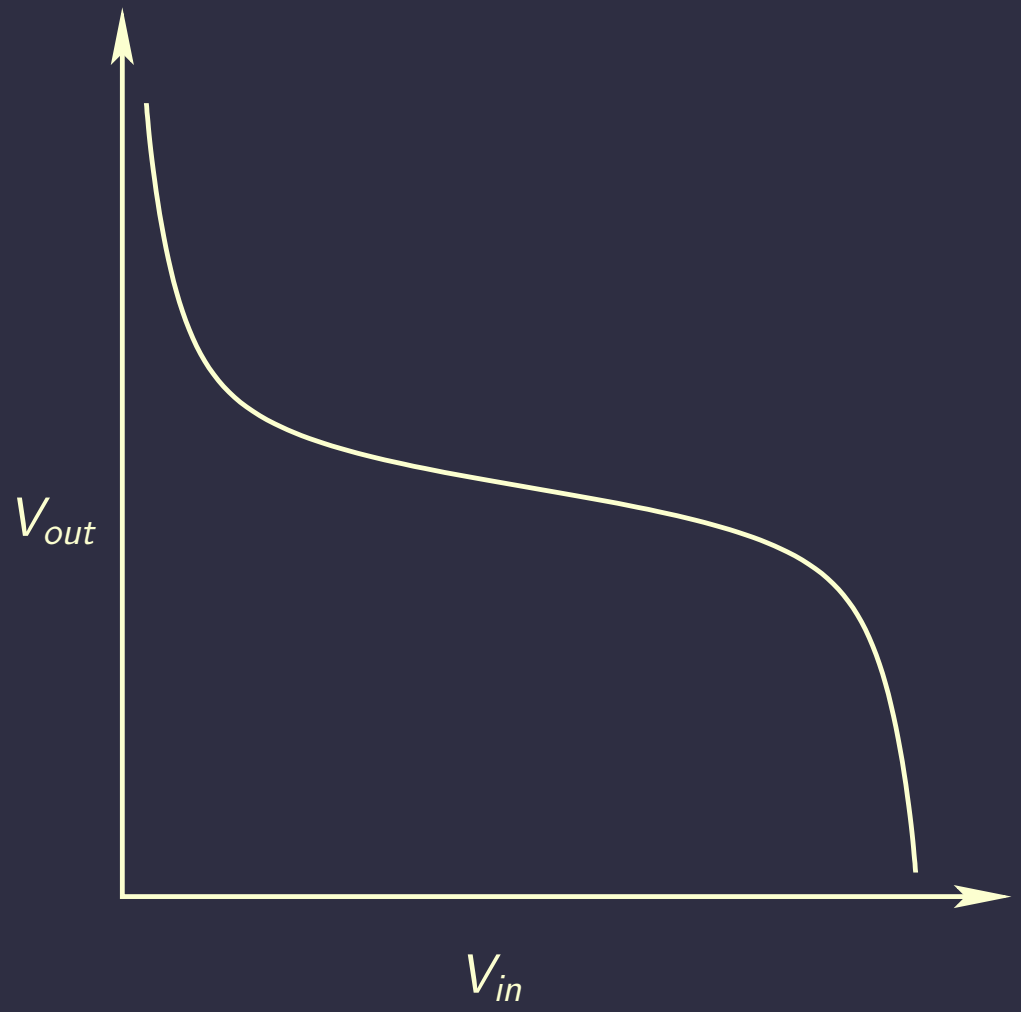
Transfer function



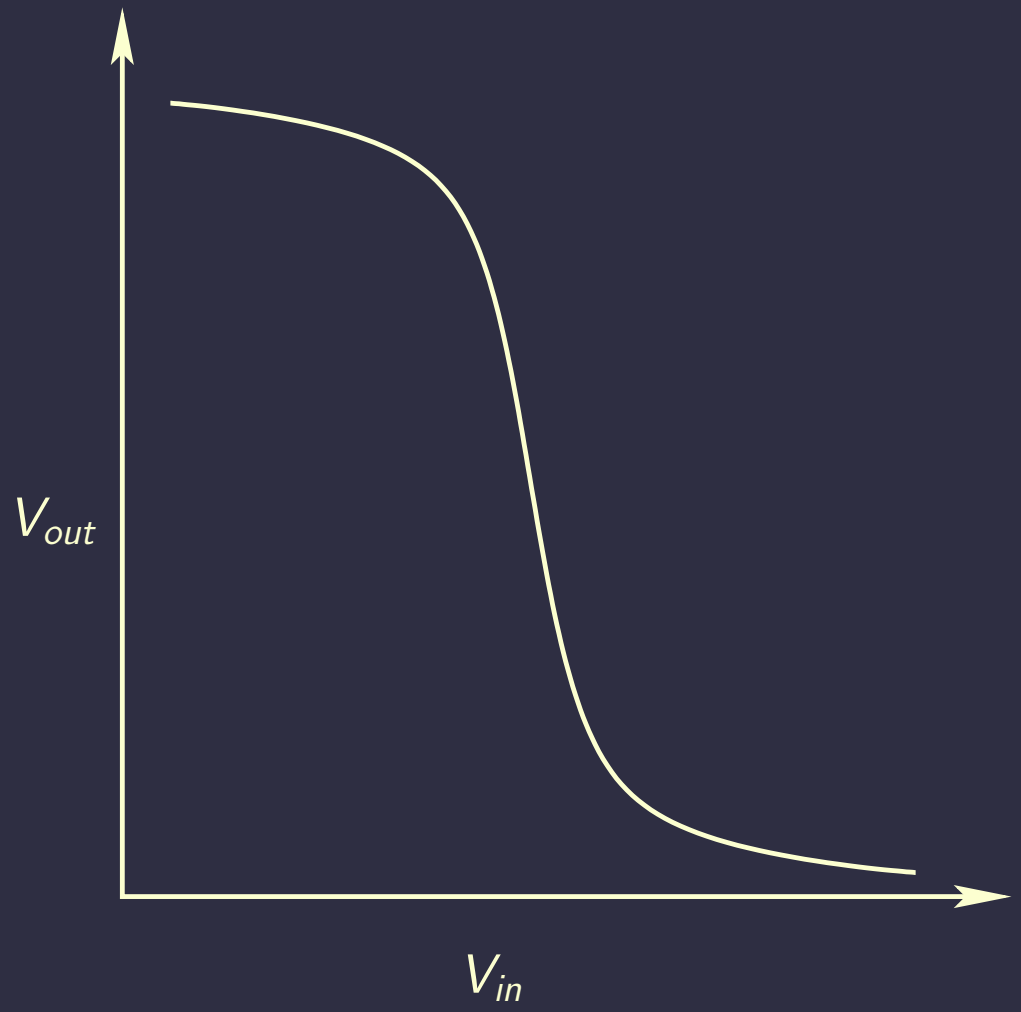
Transfer function



Transfer function



Transfer function



Completeness

- Technology should support implementation of arbitrary Boolean functions.
- Consider {AND2, OR2} and {NAND2}.

Derive and explain.

CMOS

- Metal Oxide Semiconductor
- Positive and negative carriers
- Complimentary MOS
- PMOS gates are like normally closed switches that are good at transmitting only true (high) signals
- NMOS gates are like normally open switches that are good at transmitting only false (low) signals

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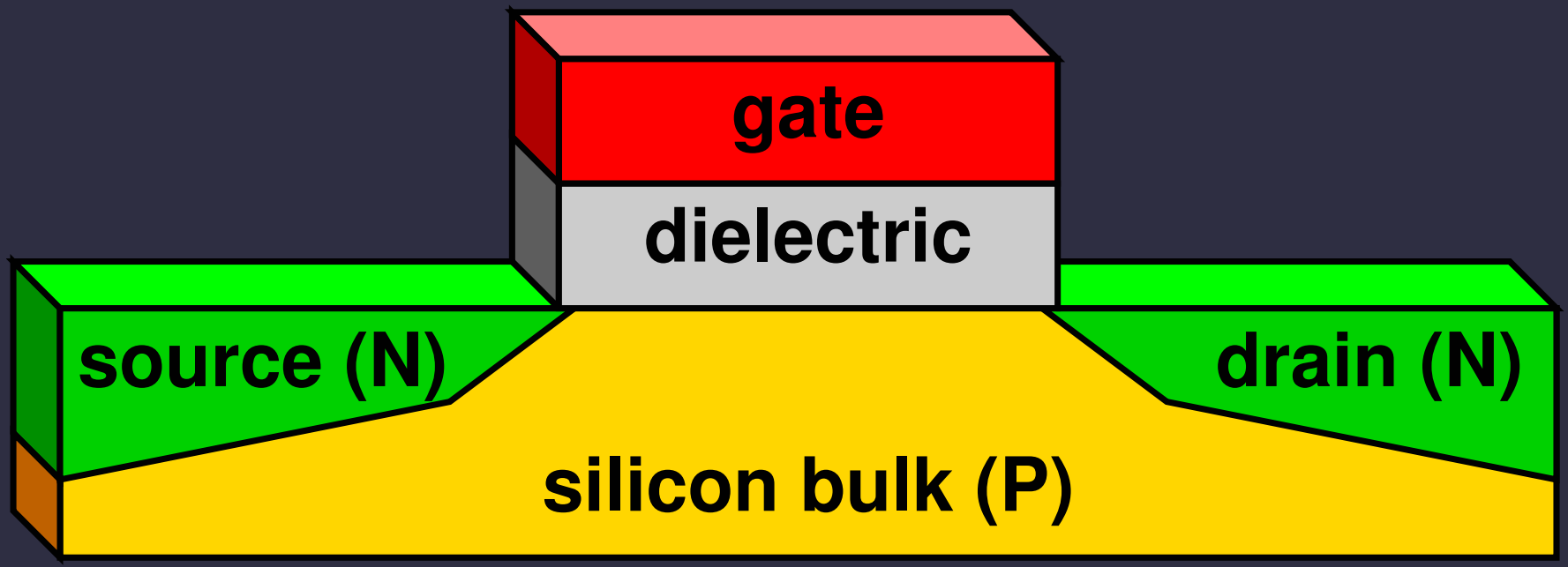
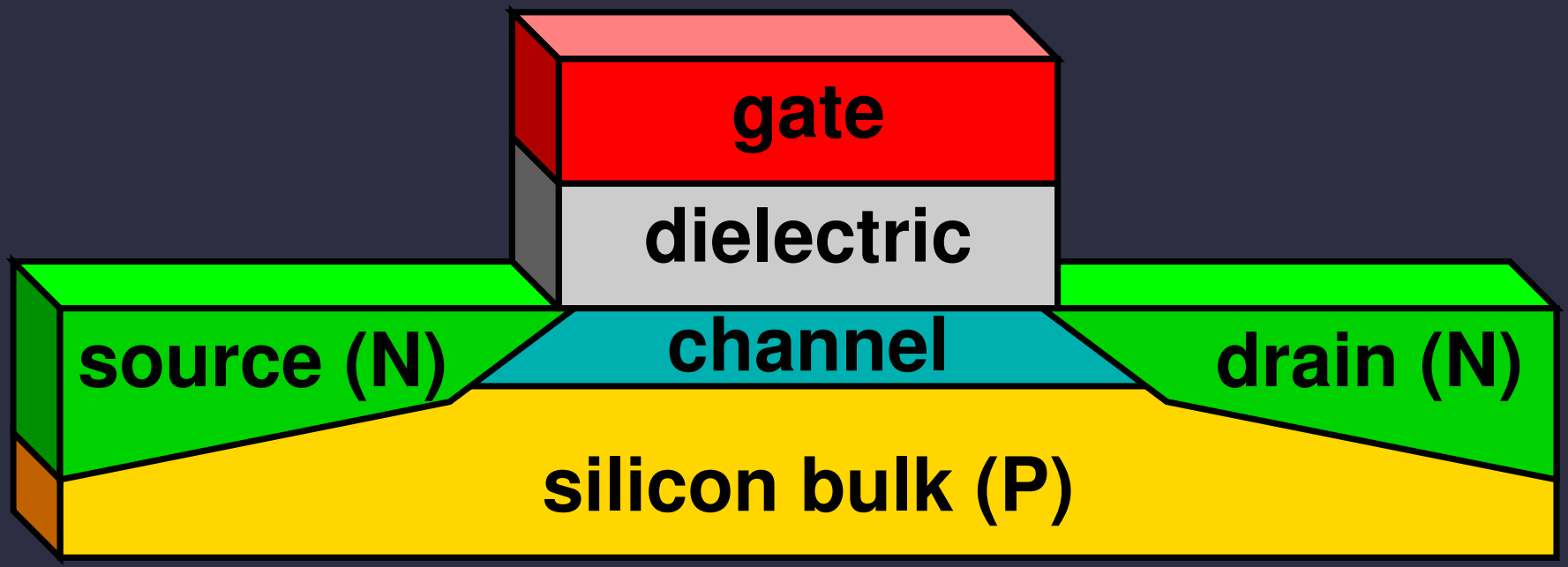
NMOSFET



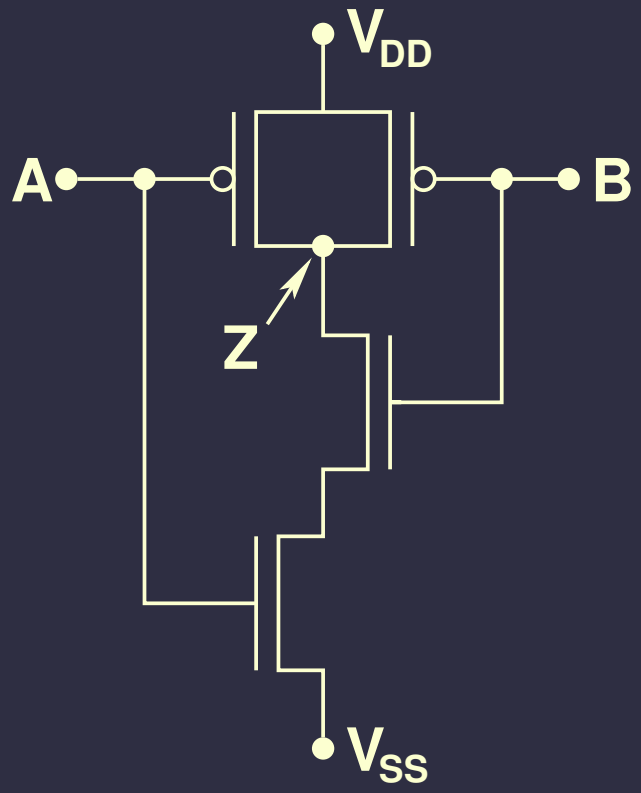
NMOSFET



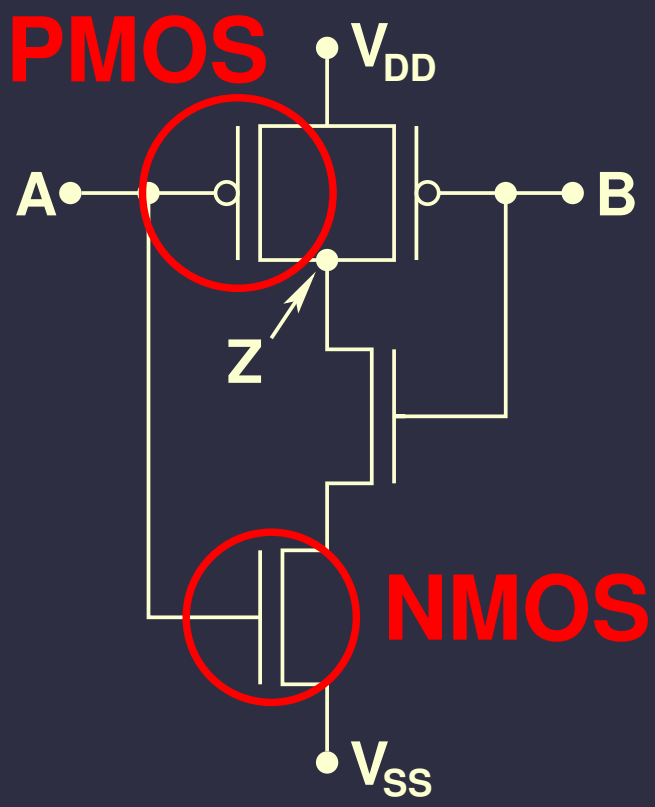
CMOS

- NMOS turns on when the gate is high
- PMOS just like NMOS, with N and P regions swapped
- PMOS turns on when the gate is low
- NMOS good at conducting low (0s)
- PMOS good at conducting high (1s)
- Use NMOS and PMOS transistors together to build circuits
  - Complementary metal oxide semiconductor (CMOS)

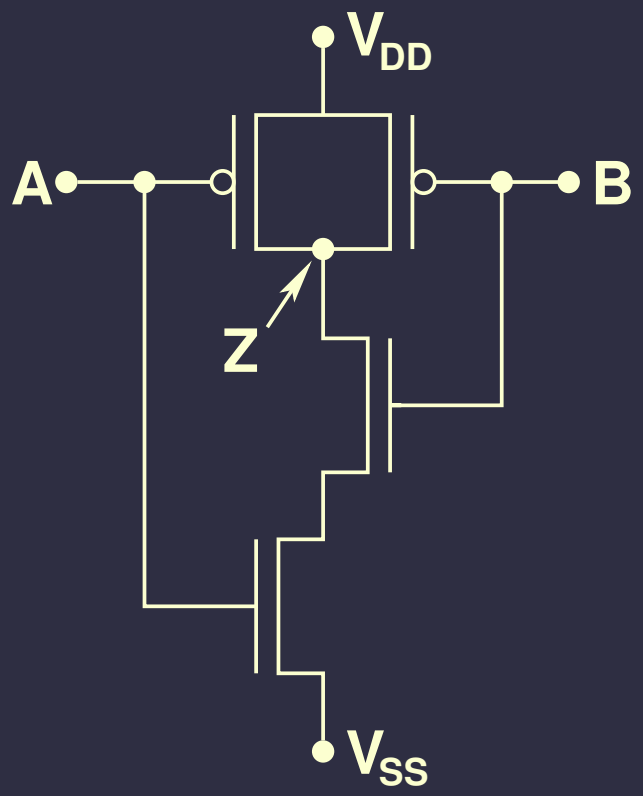
CMOS NAND gate



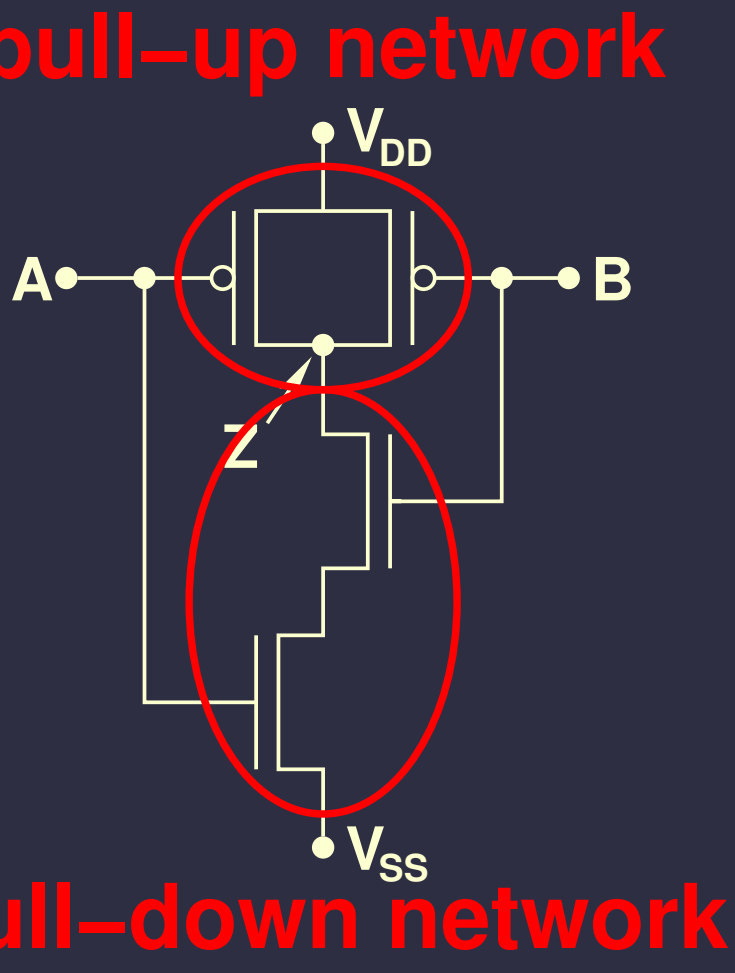
CMOS NAND gate



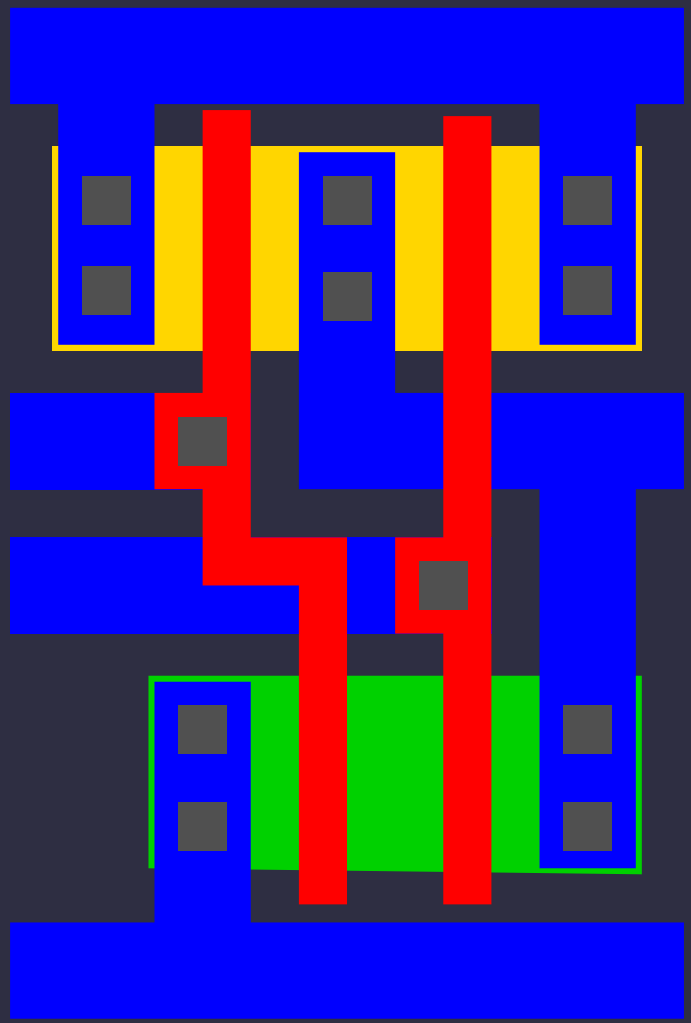
CMOS NAND gate



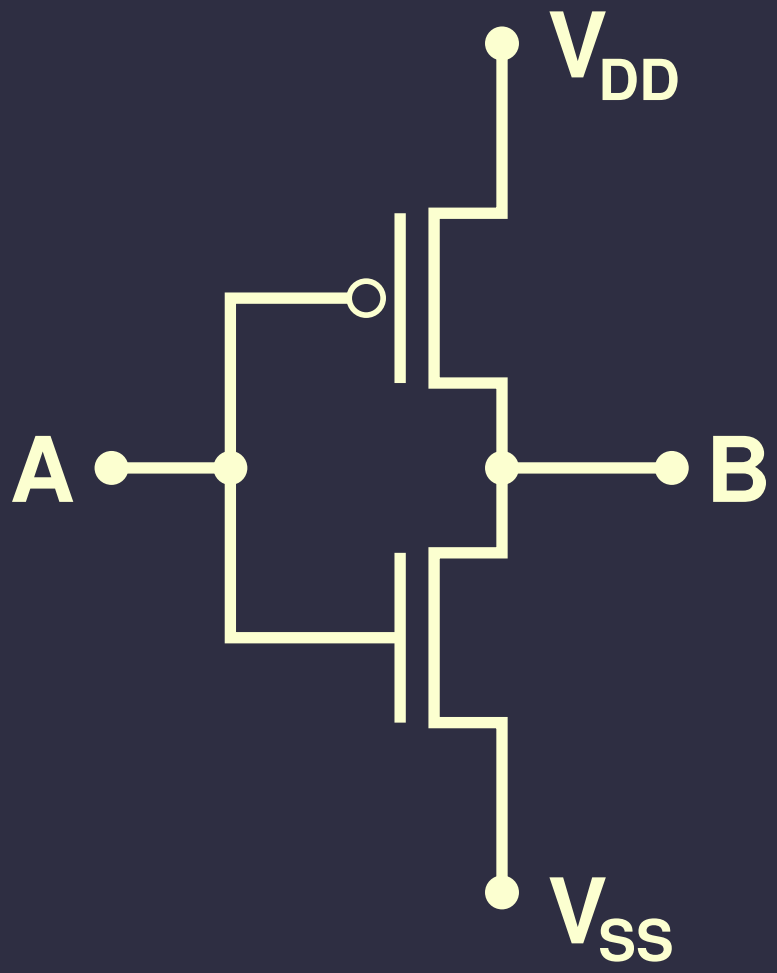
CMOS NAND gate



What is this?



What is this? How would we lay it out?



Non-Credit quiz on material covered so far

1. History of integrated circuits.
   1. What happens as a result of process scaling?
   2. What have the motivations for major changes in device technology been?
   3. What is a digital system?
   4. What is a general-purpose computer?
   5. What is an embedded system?
   6. What is an integrated circuit?
   7. What is an ASIC?
   8. What is an instruction processor?
   9. What is an FPGA?
2. What gate properties support use in digital systems?
   1. What properties should V_{out}–V_{in} curve have?
   2. Describe completeness.

Upcoming topics

Enough overview: time to start building!

- Diodes
- Transistor static behavior
- Transistor dynamic behavior

Lecture plan

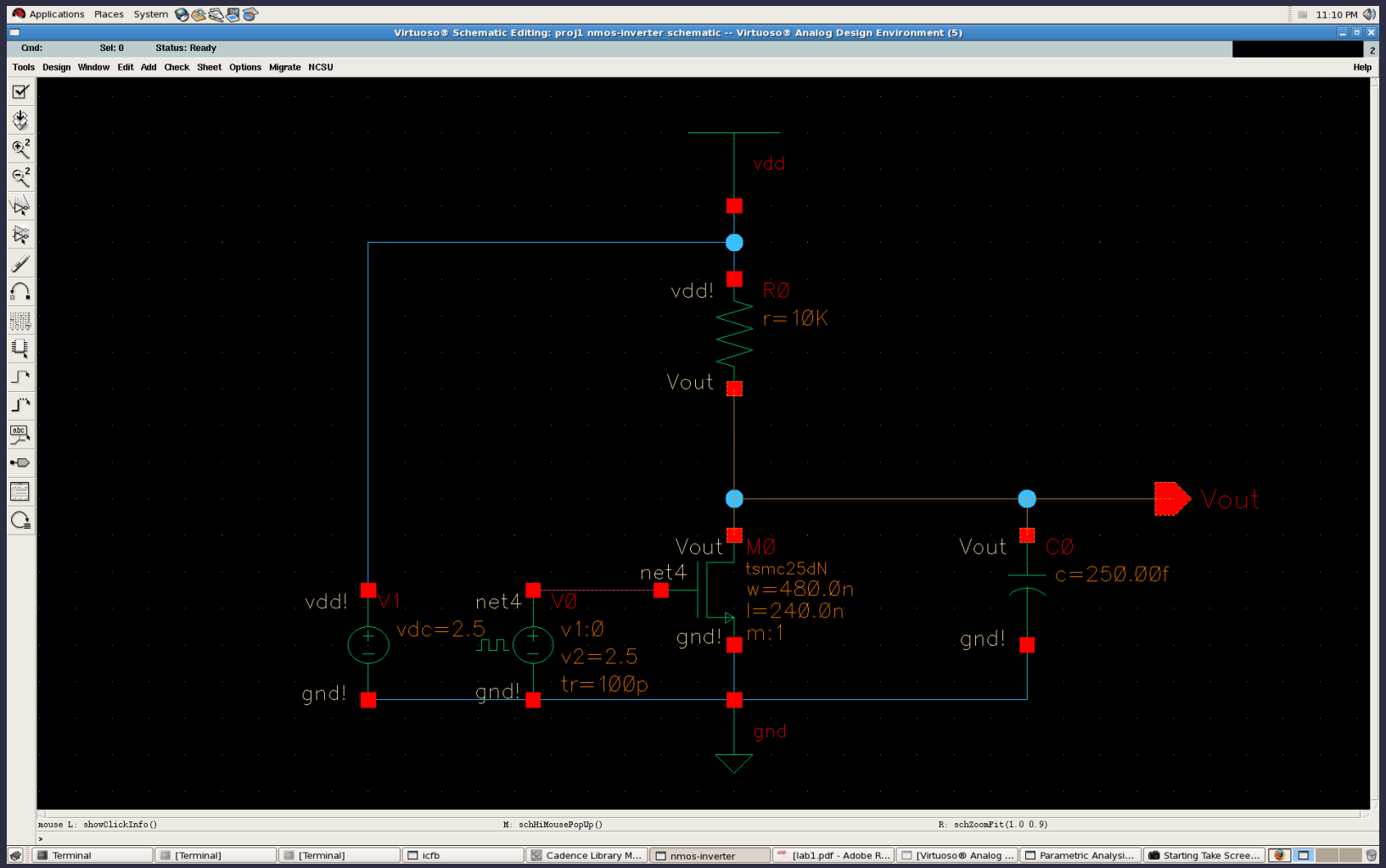
1. Recent history of digital integrated circuits
2. Digital device requirements
3. Introduction to Cadence tools
4. Homework

Lab one challenges

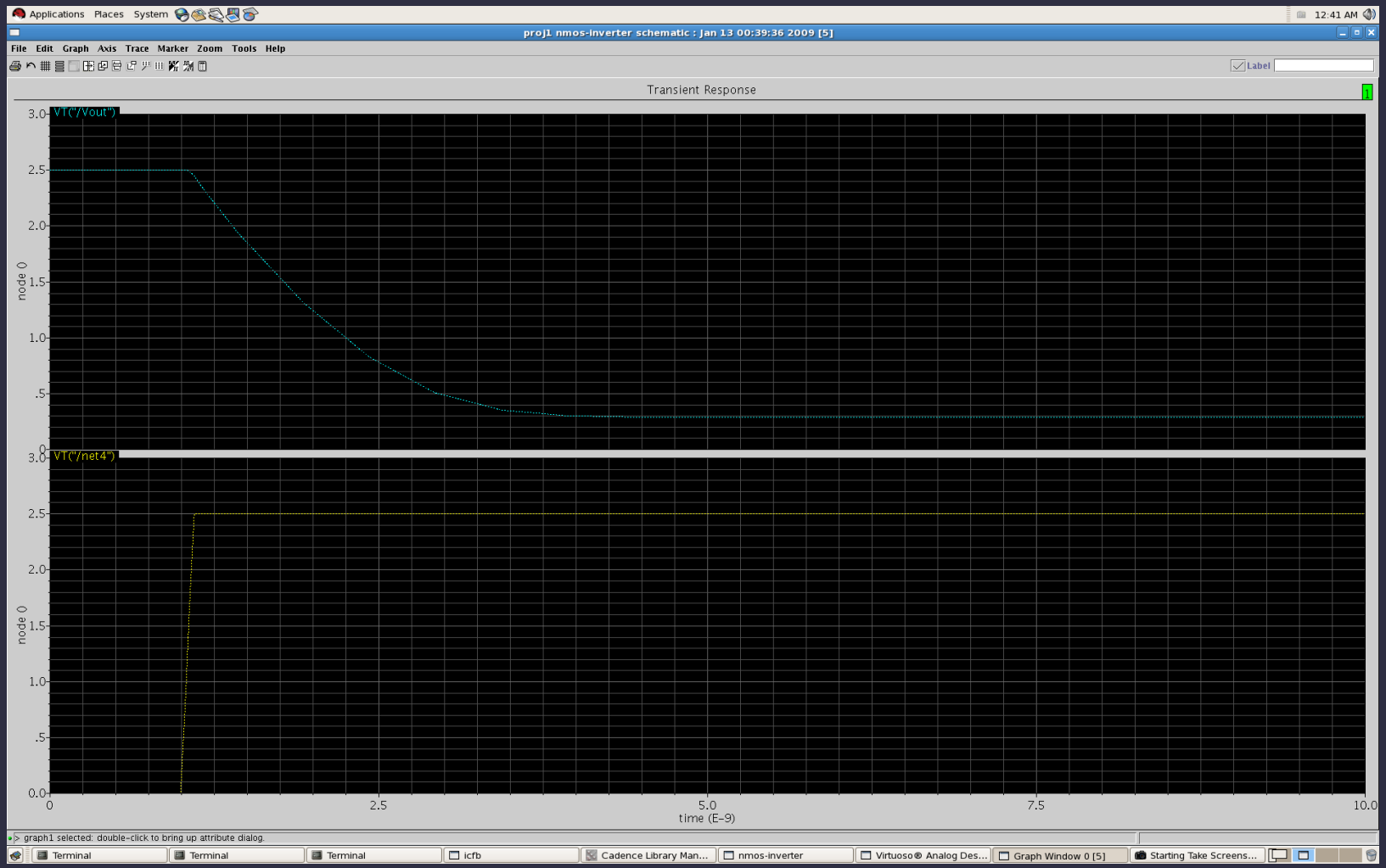
- Learning to use the tools (Friday).
- Understanding the circuits used in the lab (Tuesday).
- A note on the CAD tools market.

Derive and explain.

NMOS inverter schematic



NMOS inverter simulation results



Upcoming topics

- 6 September: Discussion in room 1620 BBB will focus on Lab 1.
- 10 September: MOSFETs.

Lecture plan

1. Recent history of digital integrated circuits
2. Digital device requirements
3. Introduction to Cadence tools
4. Homework

Homework assignment and announcement

- 5 September: Email topics of interest.
- 10 September: Read Sections 3.1, 3.2, and 3.3.1 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 17 September: Laboratory assignment one.