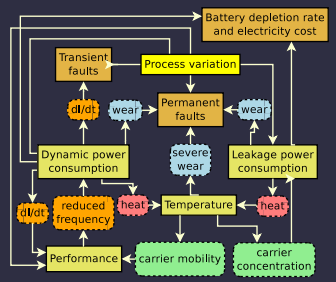
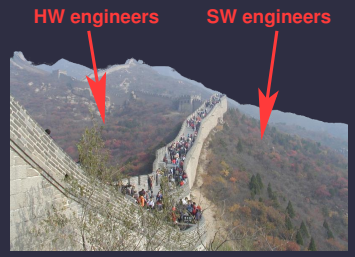
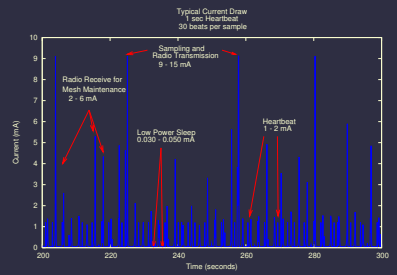
Digital Integrated Circuits – EECS 312

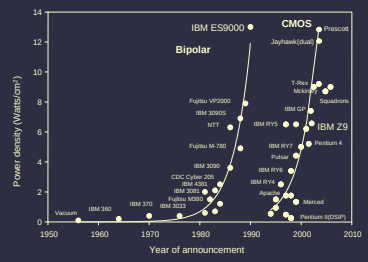
http://robertdick.org/eecs312/

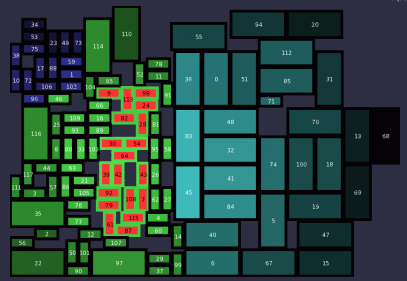
Teacher:	Robert Dick	GSI:	Shengshou Lu
Office:	2417-E EECS	Office:	2725 BBB
Email:	dickrp@umich.edu	Email:	luss@umich.edu
Phone:	734–763–3329		
Cellphone:	847–530–1824		











Review

1. Explain each transistor operating region.
2. What is pinch-off?
3. How does body bias work?
4. What is velocity saturation?
5. What is sub-threshold operation?

Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework

Process variation

Given our current knowledge of transistor operation, what impact will variation in

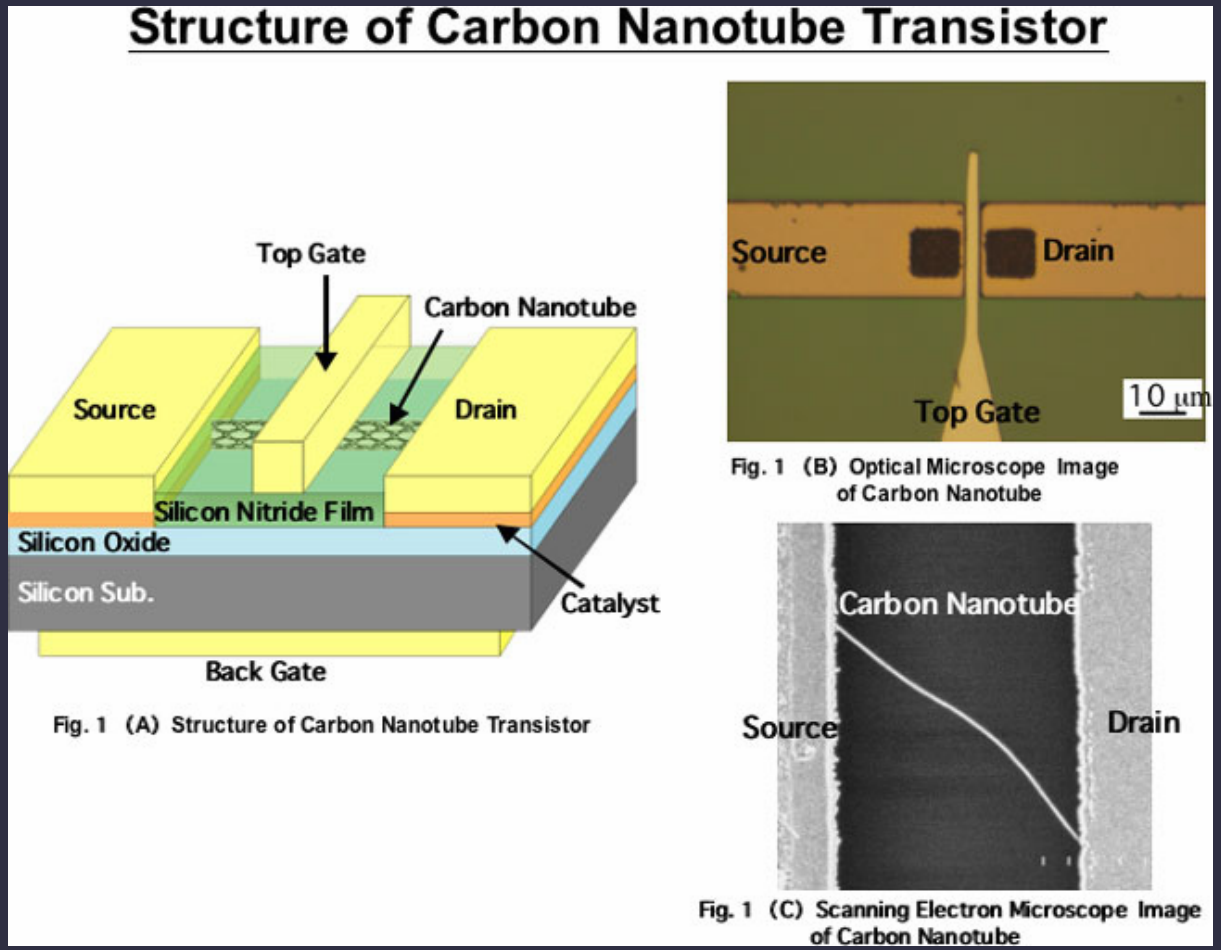
- dopant concentrations,
- oxide thickness,
- transistor width, and
- interconnect width

have?

FinFETs

From Freescale.

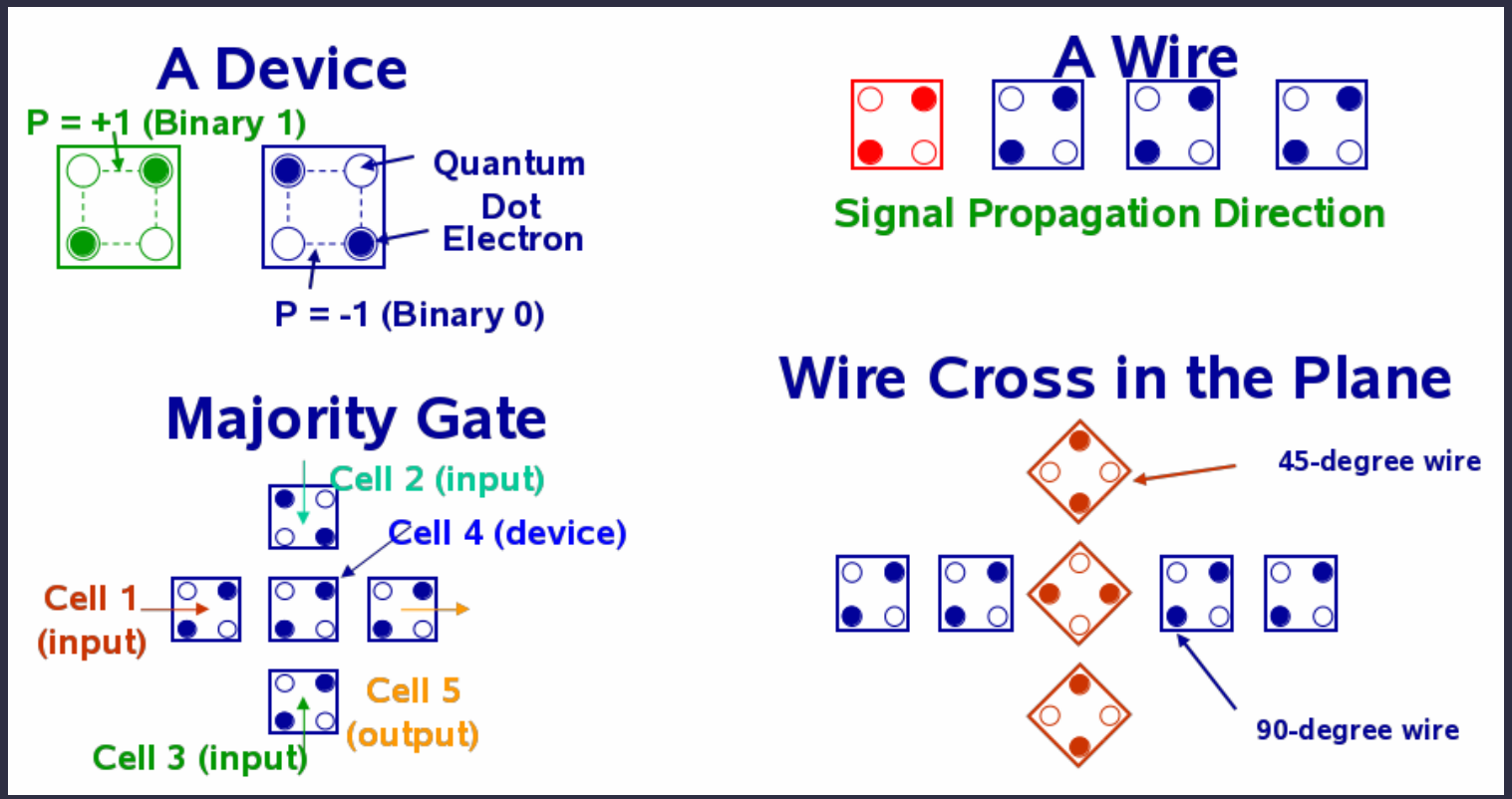
Carbon nanotubes and nanowires



From AIST.

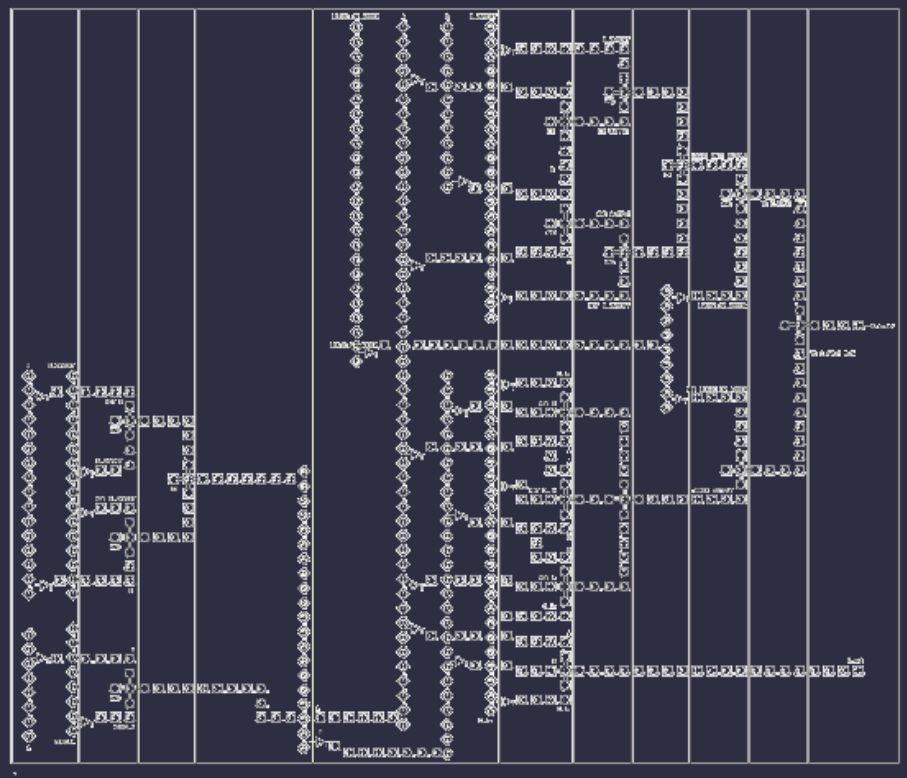
Quantum cellular automata

- Binary information encoded in device configuration.
- Signals are propagated through nearest neighbor interaction.



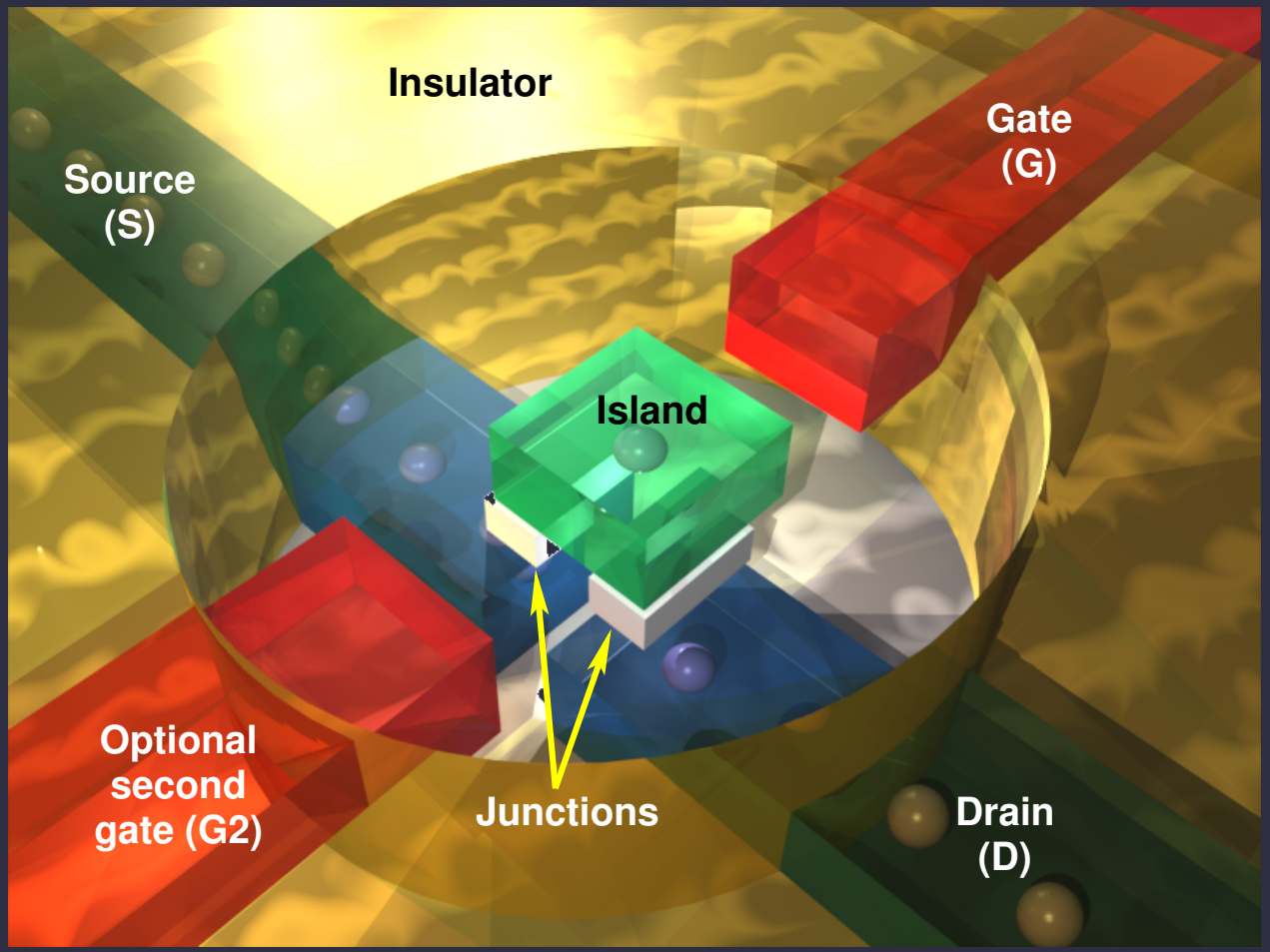
From Professor Xiaobo Sharon Hu.

Quantum cellular automata arithmetic-logic unit



From Professor Xiaobo Sharon Hu.

Single-electron tunneling transistors



Common problems

- Difficult to get high-quality devices where they are needed.
- High susceptibility to thermal noise.
- High susceptibility to charge trap offsets.
- Low gain.

What does the future hold

- CMOS for another decade or so, until devices consist of a small integer number of atoms.
- Nobody knows what comes next.
- Nothing? New device technology?
- Implications for information technology?

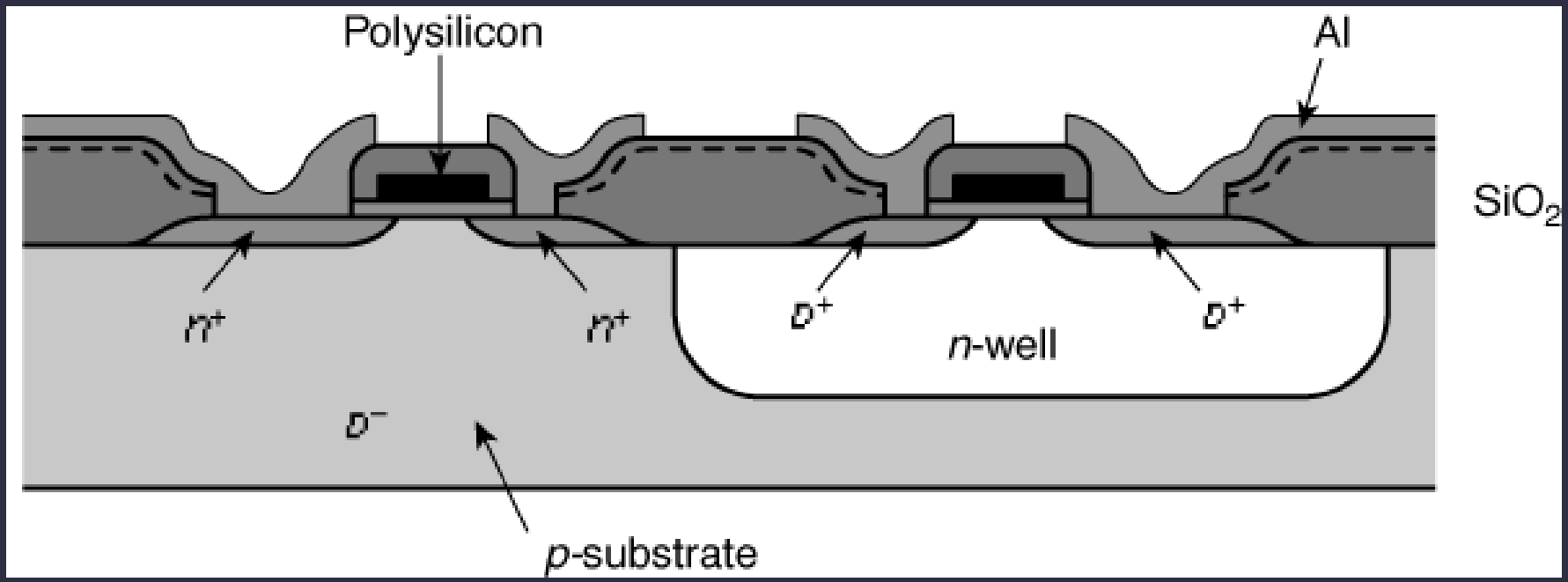
Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework

Review

1. List a few different alternatives to CMOS for use in digital systems.
2. Indicate their advantages and disadvantages relative to CMOS.

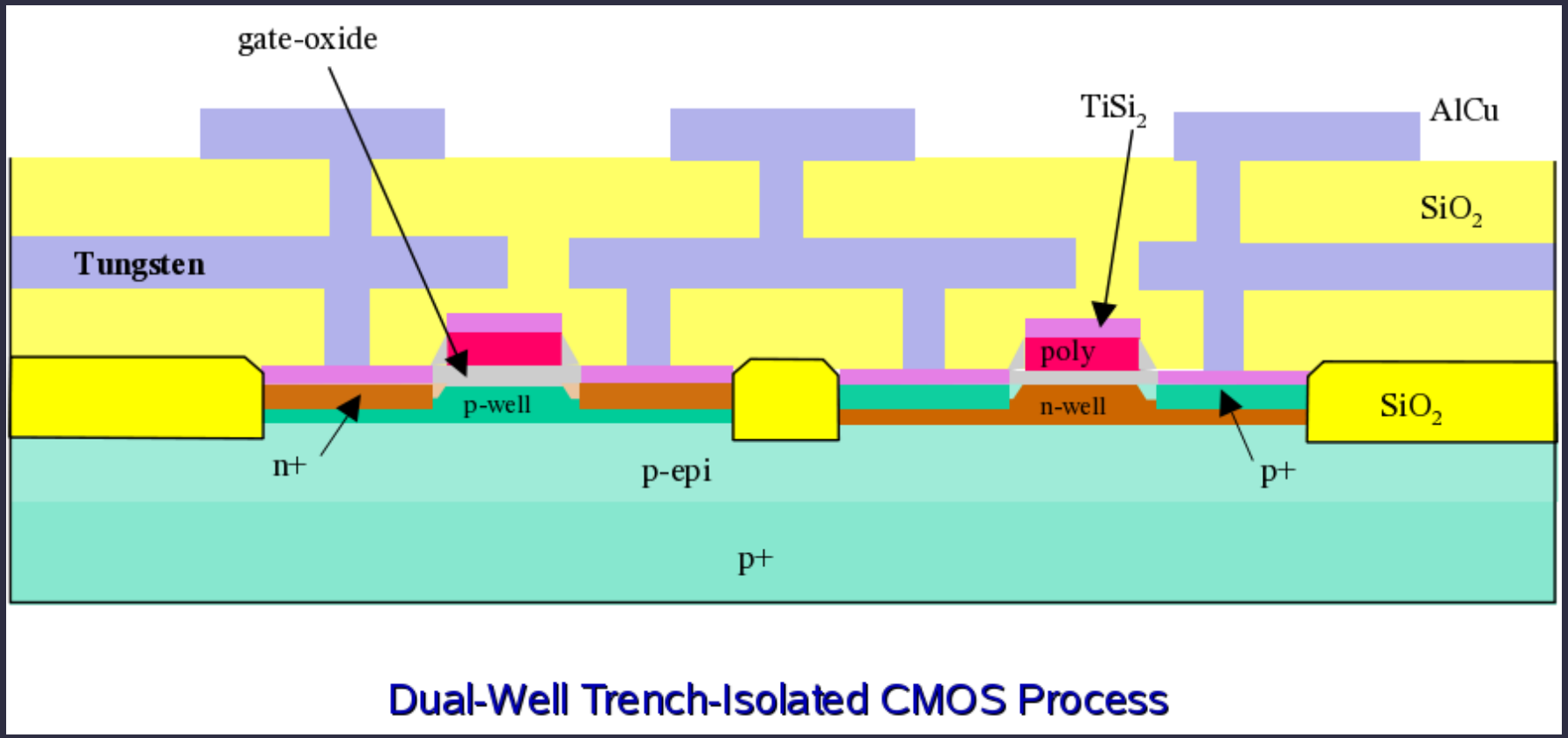
NMOSFET



Insulator properties

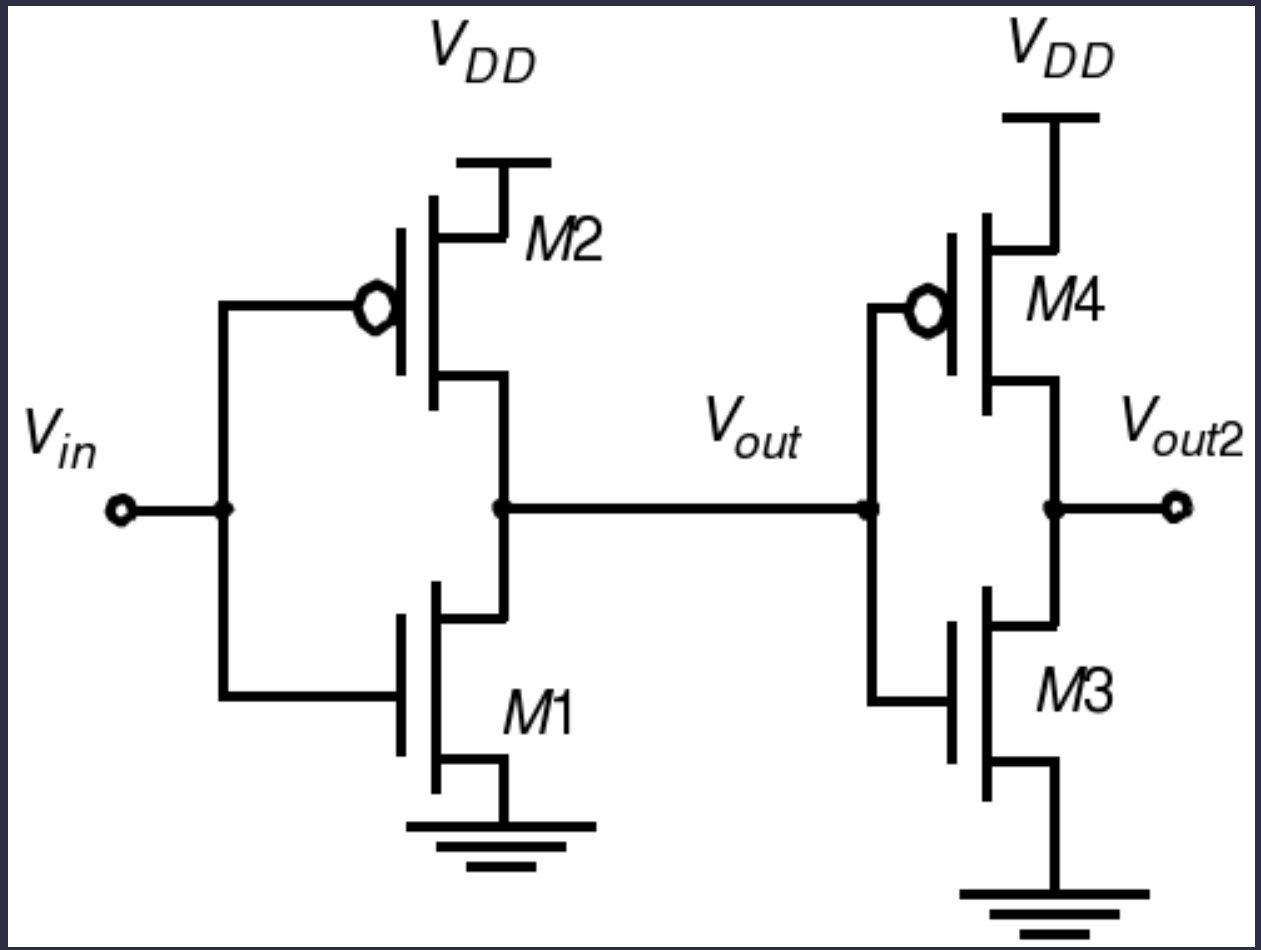
- Low-κ: reduced capacitance, useful for isolating wires.
- High-κ: increased capacitance, useful for maintaining k despite increased gate thickness.

High-level fabrication process overview

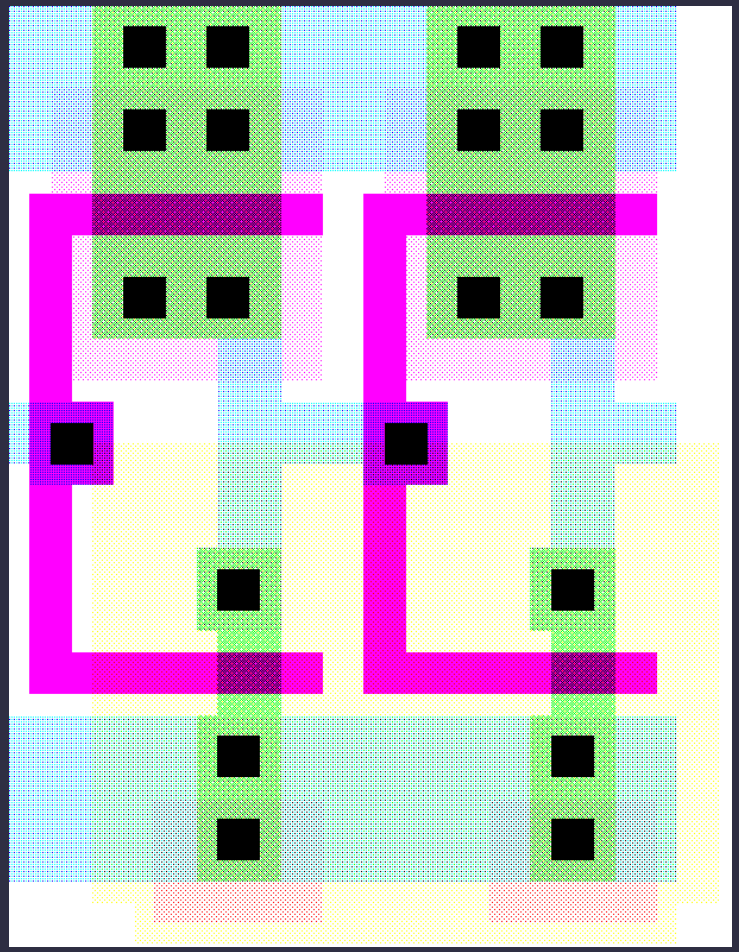


Dual-Well Trench-Isolated CMOS Process

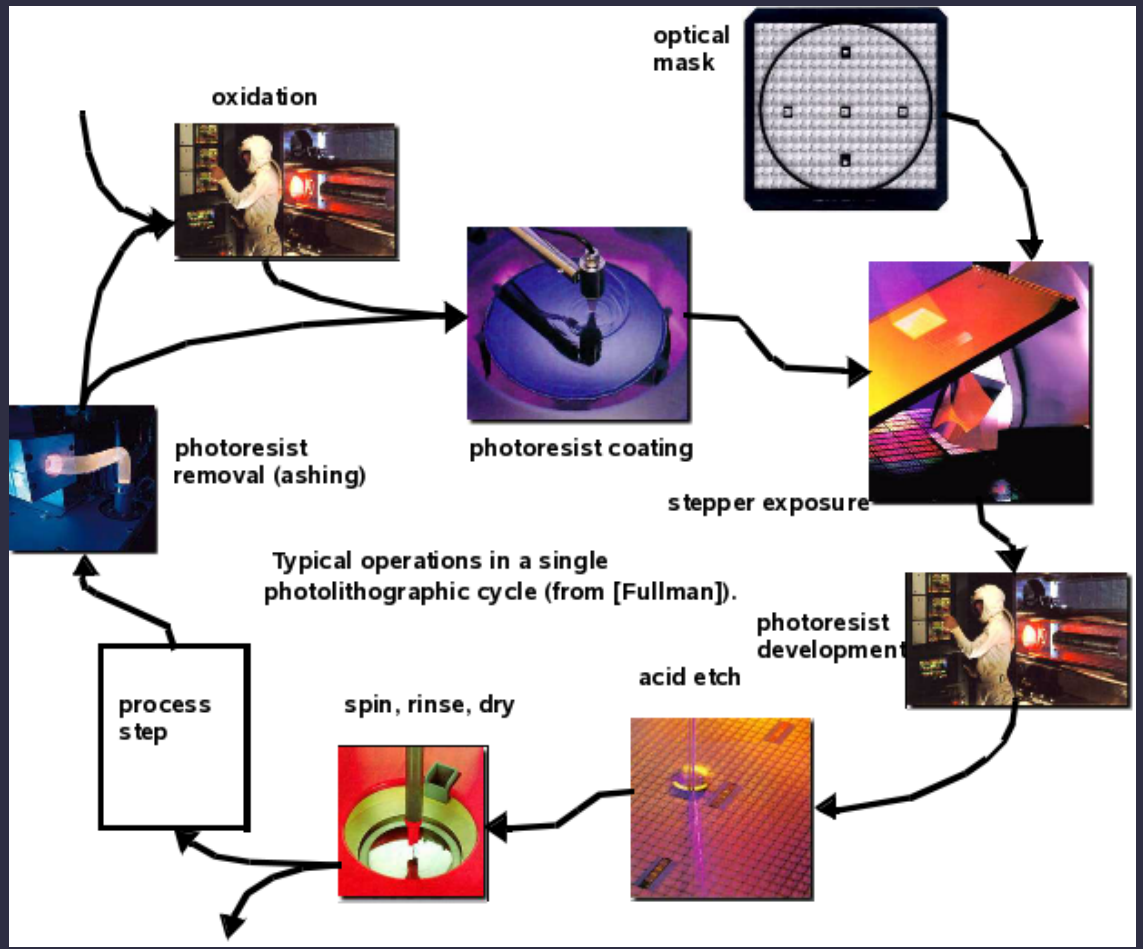
Schematic of circuit to fabricate



Layout of circuit to fabricate



Overview of fabrication process



Fabrication process details

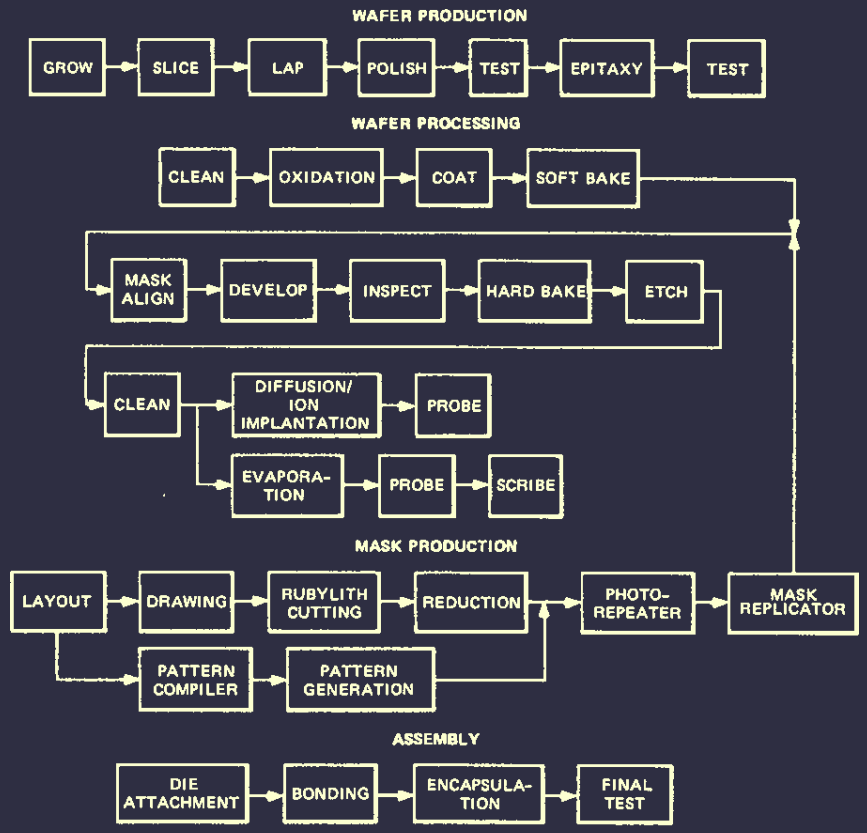
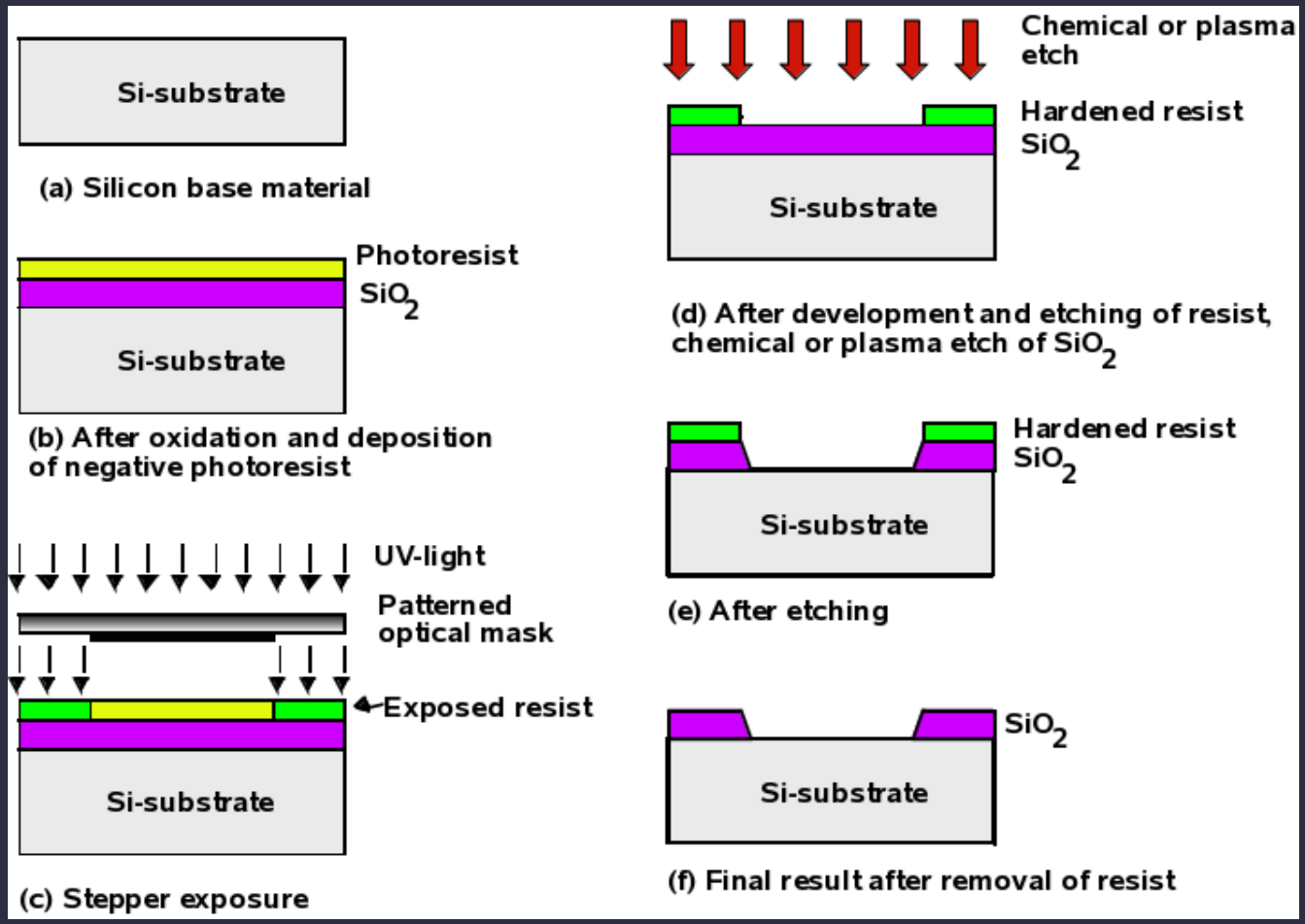


FIGURE 1.37. General semiconductor production process.

From Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Addison-Wesley, 1993.

SiO_2 patterning



Etching

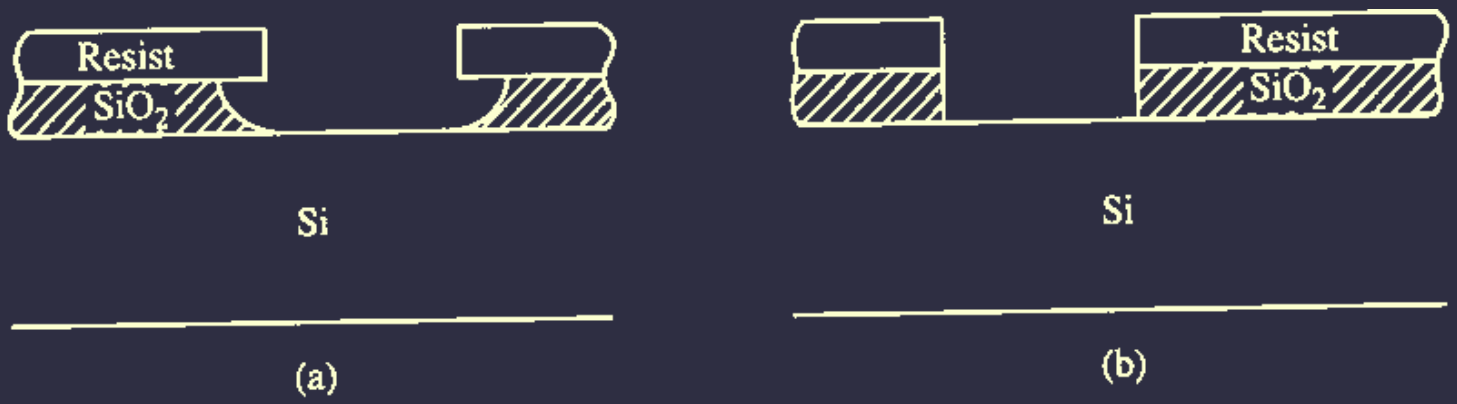


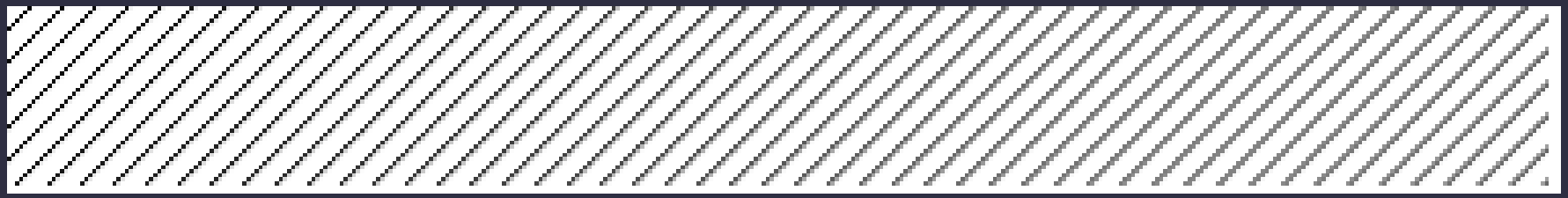
Fig. 2.5 Etching profiles obtained with (a) isotropic wet chemical etching and (b) dry anisotropic etching in a plasma or reactive-ion etching system.

From Richard C. Jaeger. *Introduction to Microelectronic Fabrication*. Addison-Wesley, 1993.

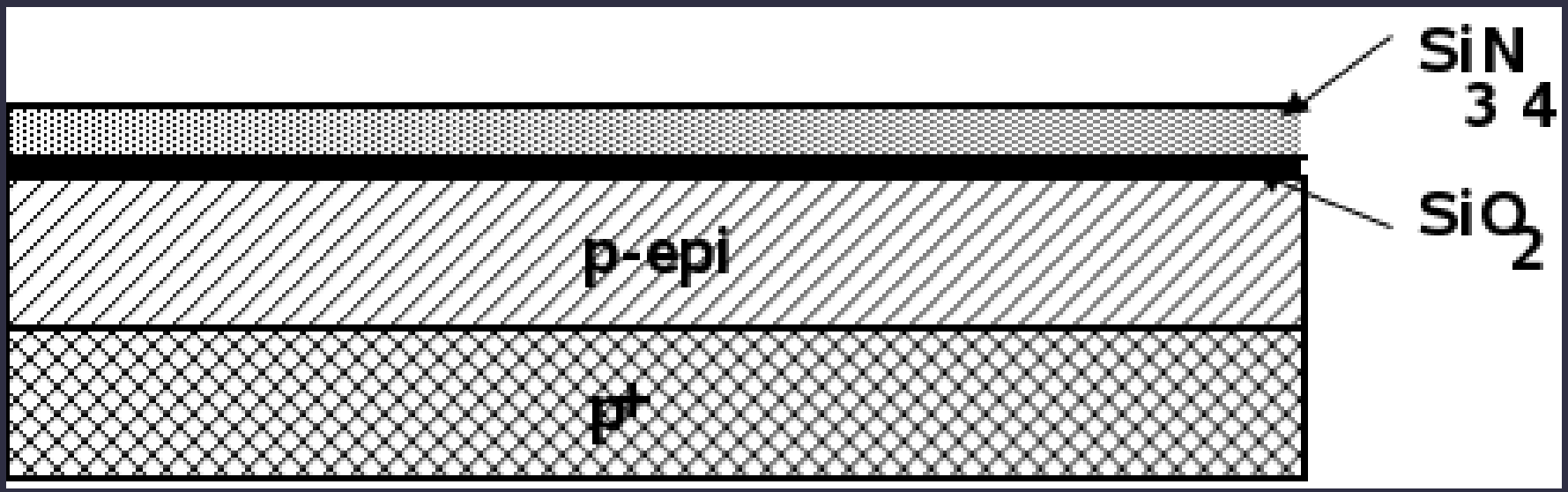
Summary of processing steps

1. Define active areas.
2. Etch and fill trenches.
3. Implant well regions.
4. Deposit and pattern polysilicon/metal gate layer.
5. Implant source and drain regions, and substrate contacts.
6. Create contacts and via windows.
7. Deposit and pattern metal layers.

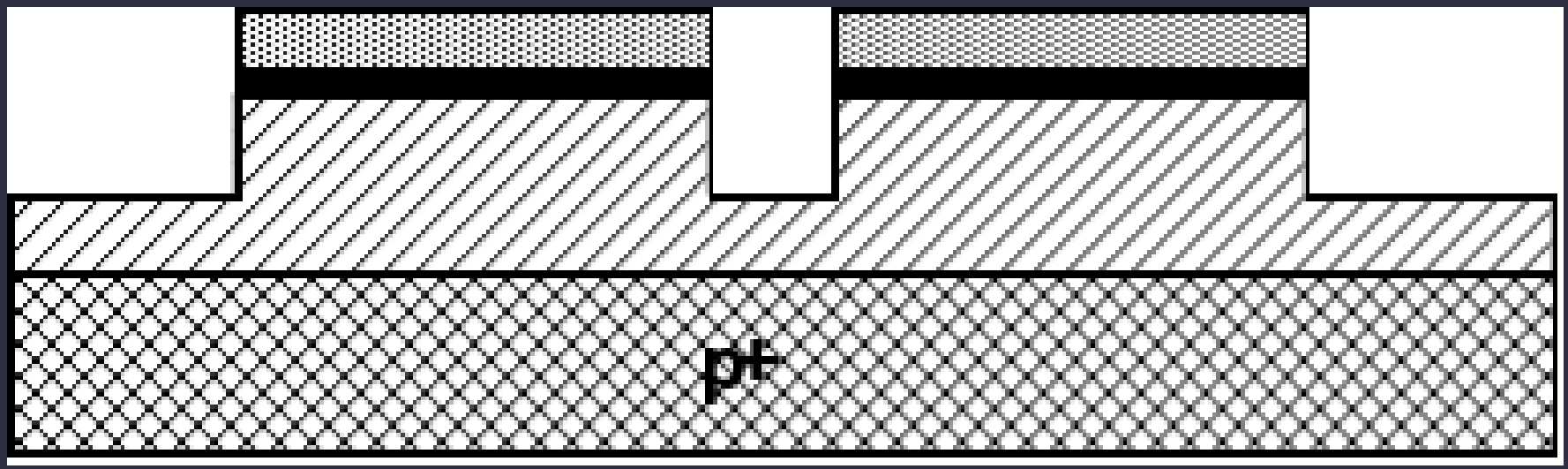
Step 1: epitaxial layer



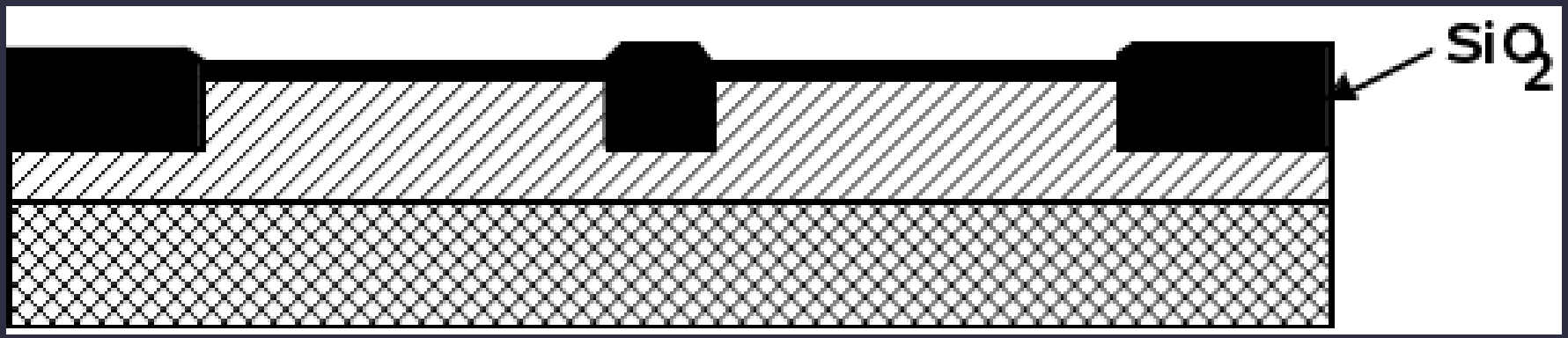
Step 2: gate oxide and sacrificial nitride layer deposition



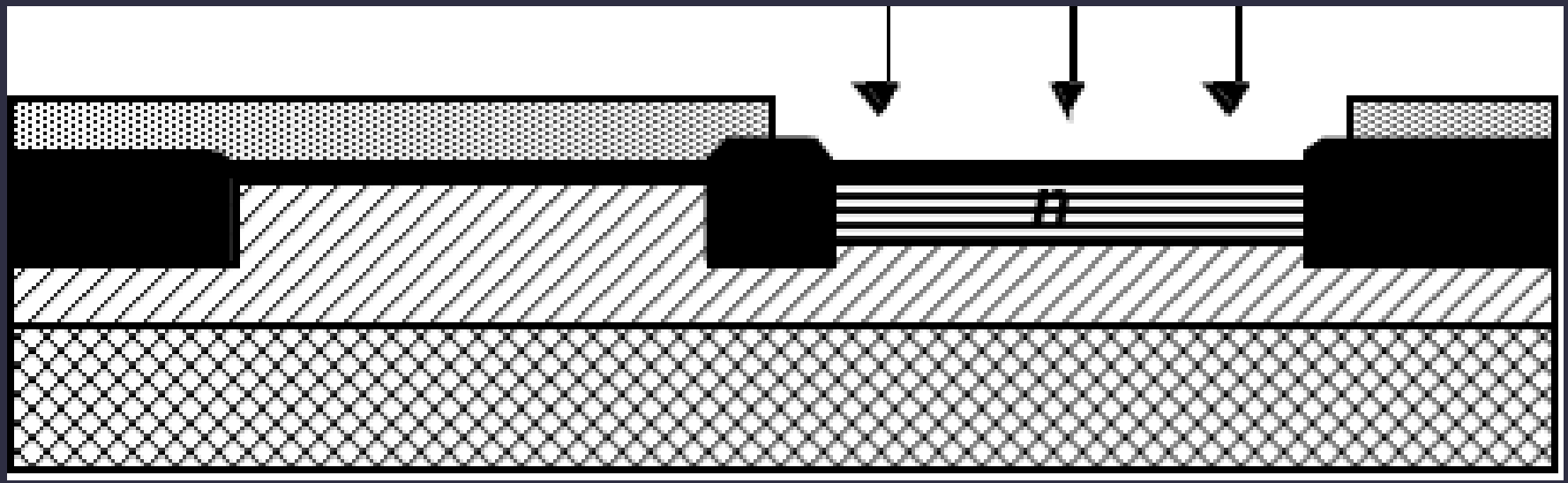
Step 3: plasma etching



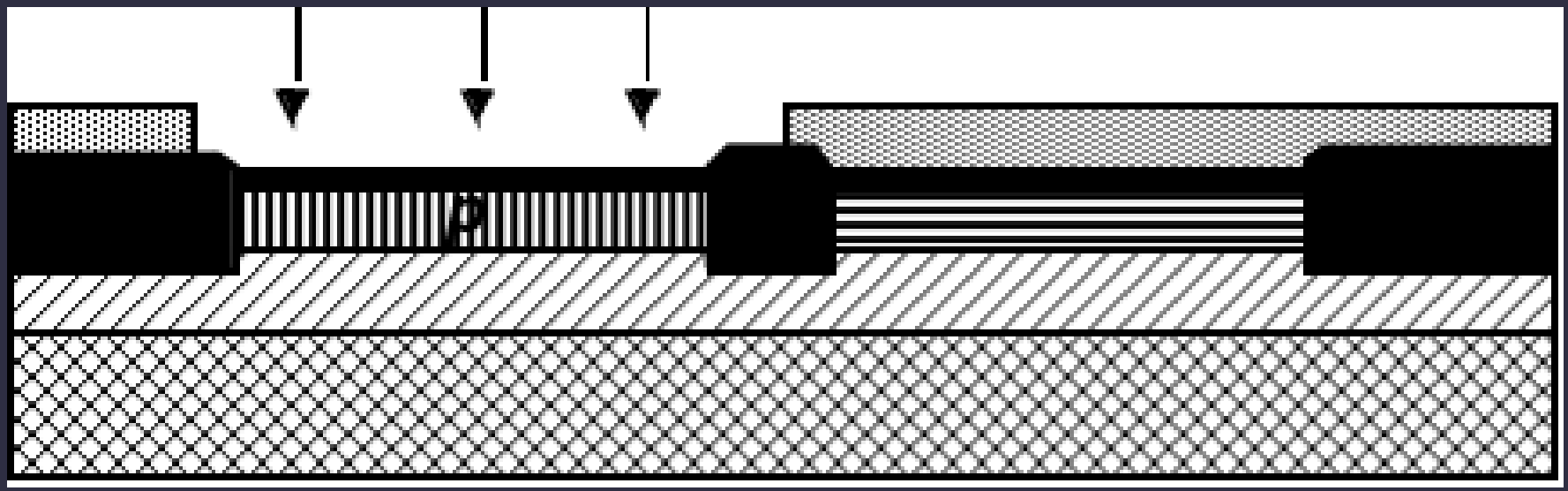
Step 4: trench filling, CMP, etching, SiO_2 deposition



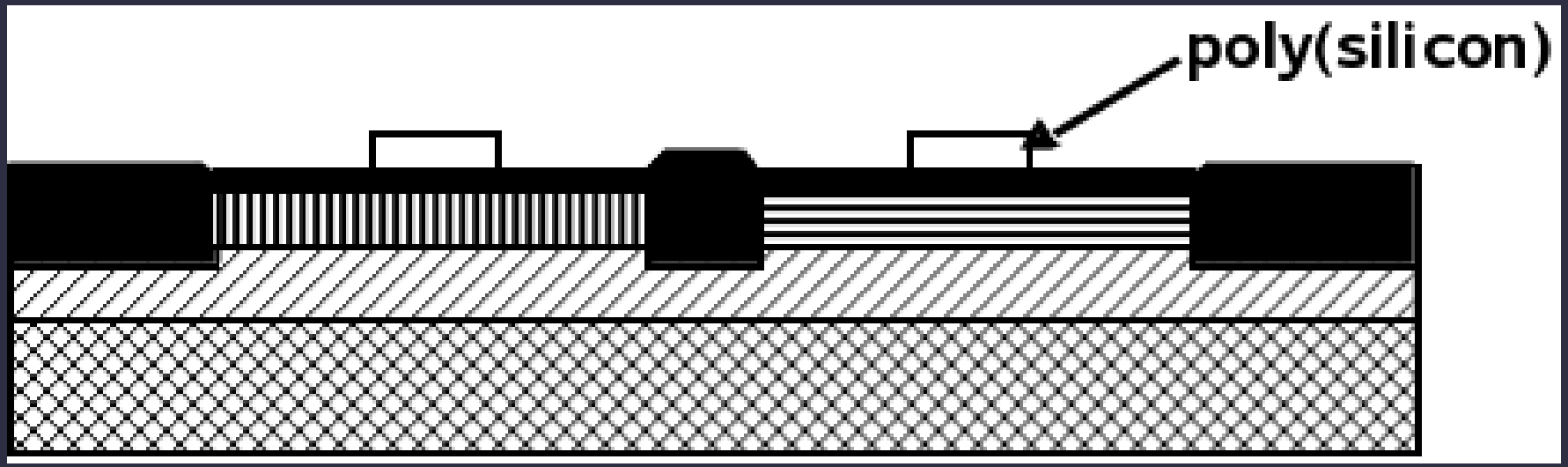
Step 5: n-well and V_{Tn} adjustment implants



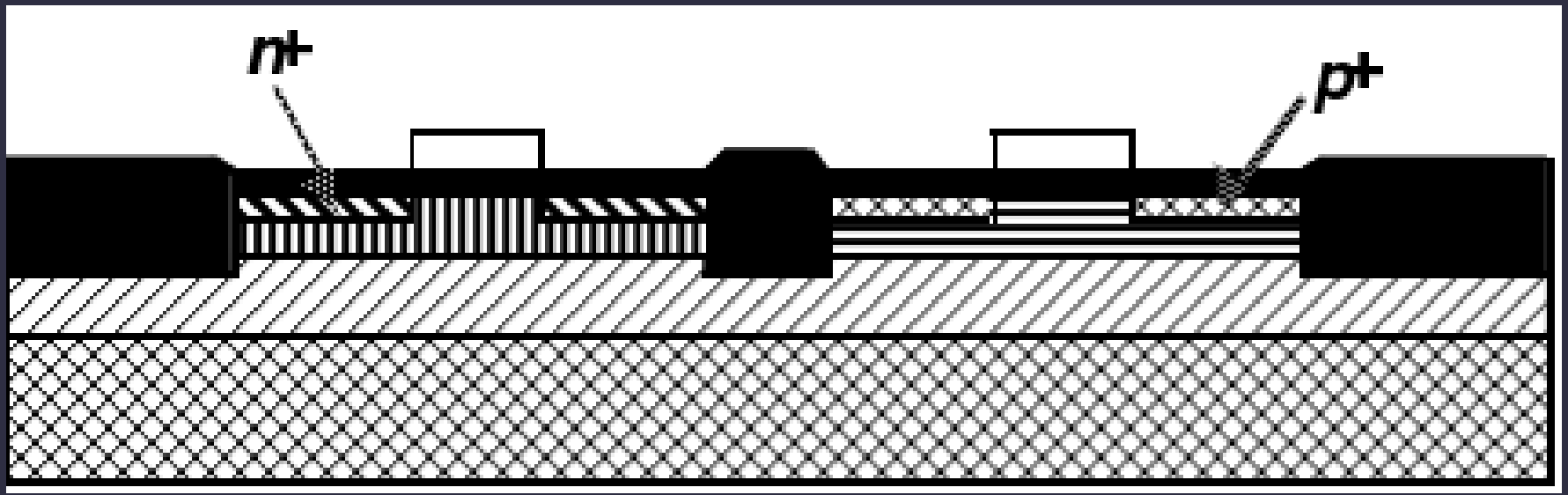
Step 6: p-well and V_{Tp} adjustment implants



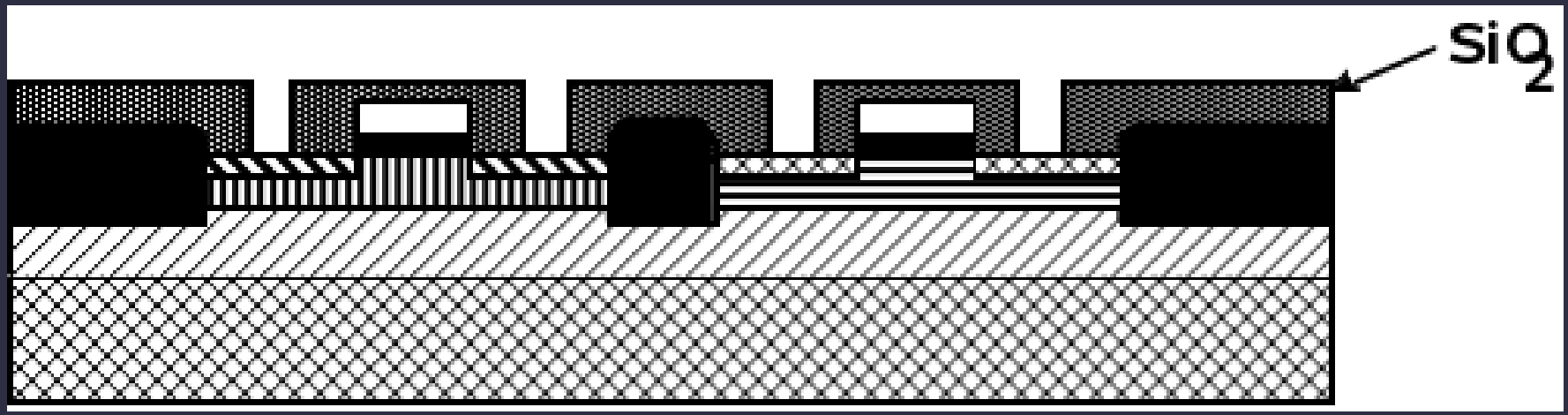
Step 7: polysilicon/metal deposition and etch



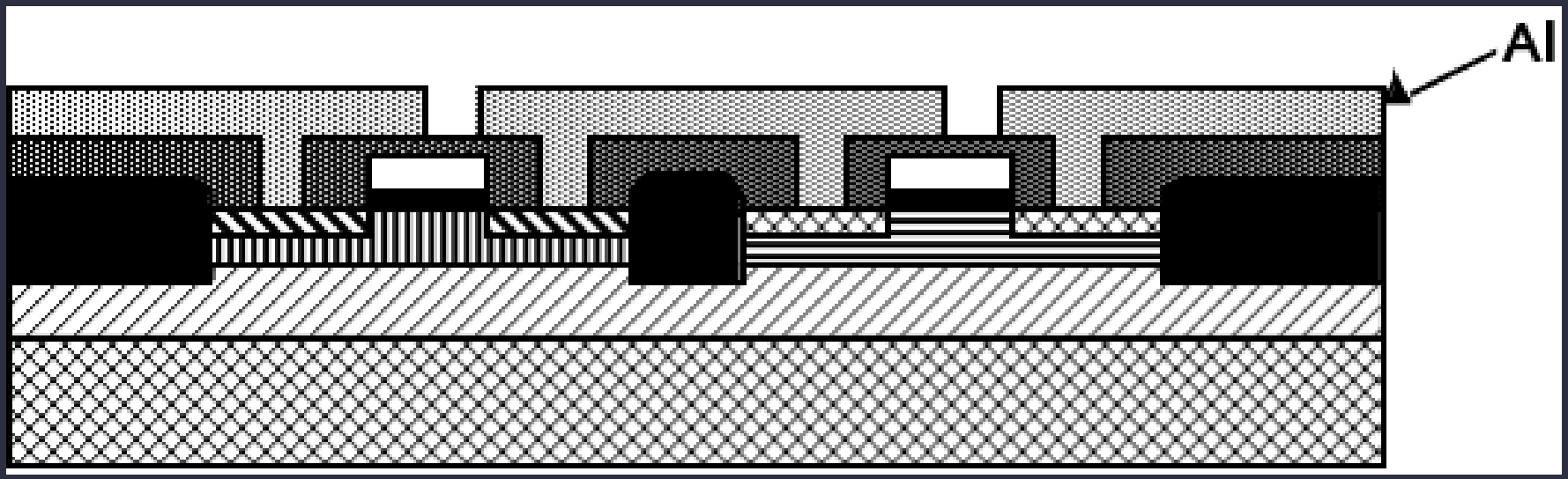
Step 8: n^+ and p^+ source, drain, and poly implantation



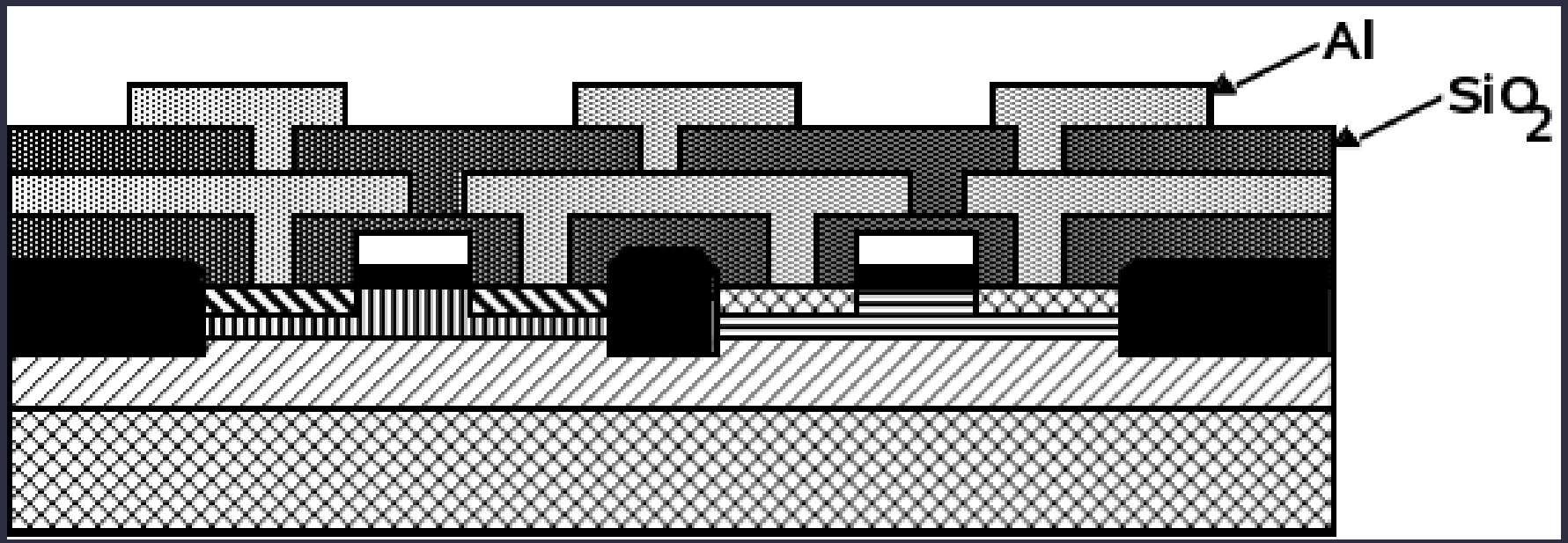
Step 9: SiO_2 deposition and contact etch



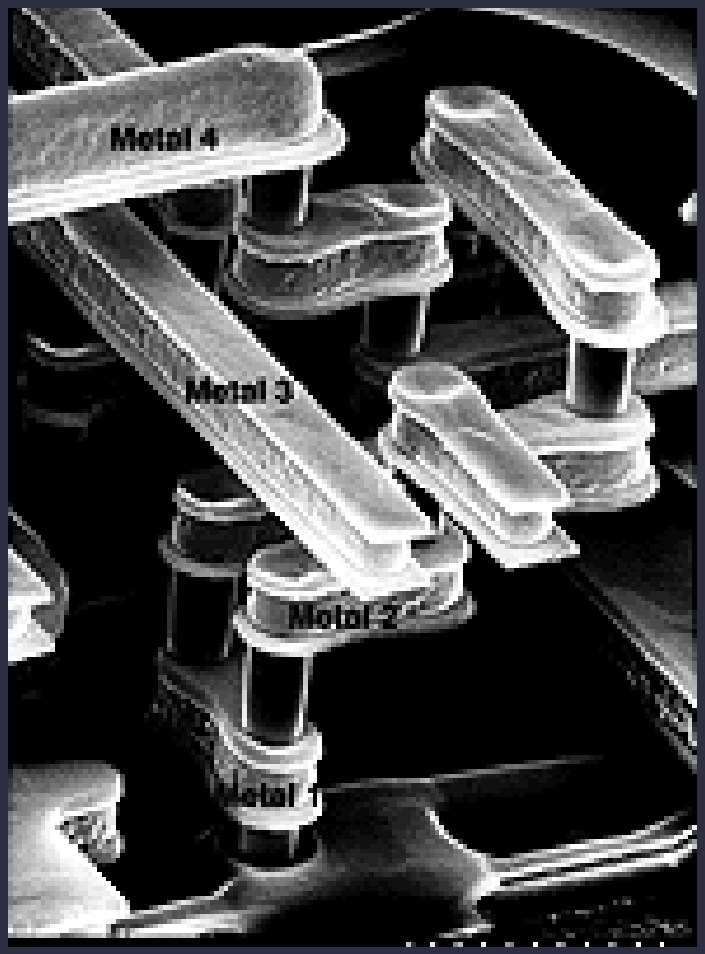
Step 10: deposit and pattern first interconnect layer



Step 11: deposit SiO_2, etch contacts, deposit and pattern second interconnect layer



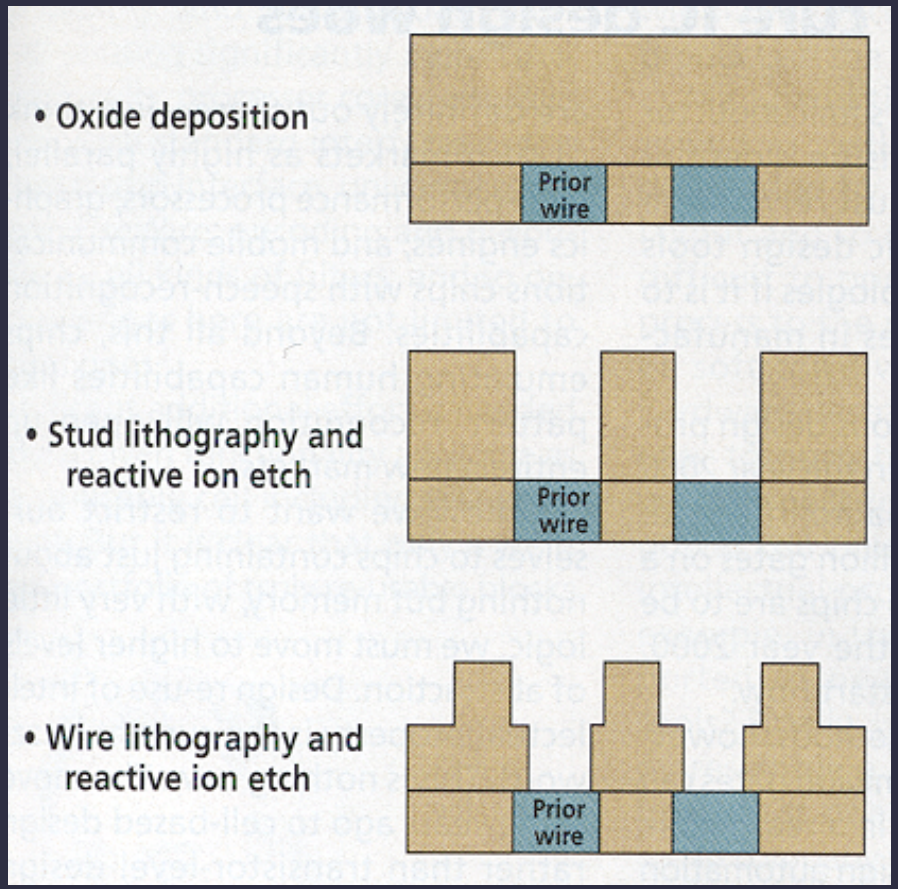
Interconnect layers

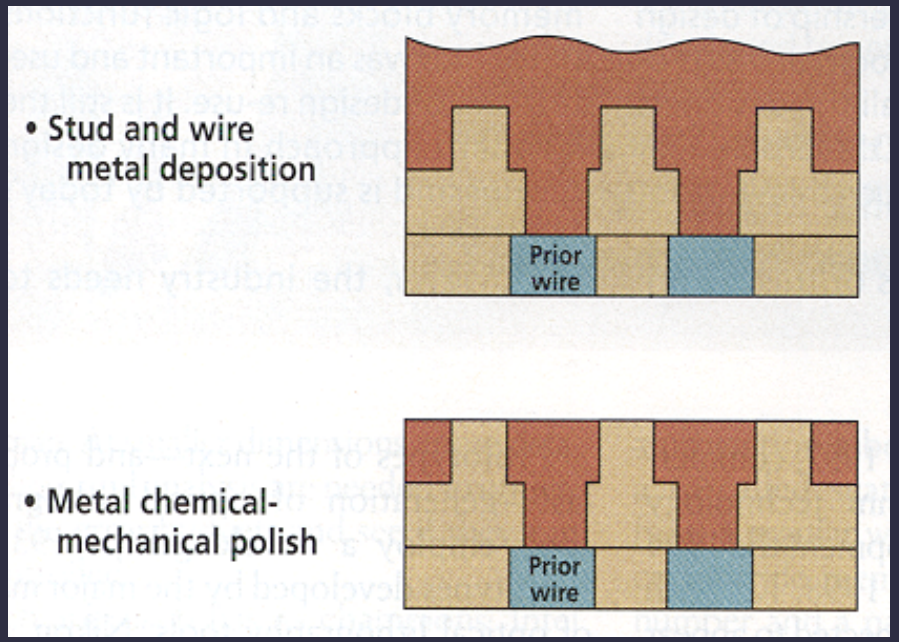


Al vs. Cu

- For Al, can deposit and etch metal layers.
- Cu alloys with Si.
- Cannot safely deposit Cu directly on Si.
- Cu difficult to controllably etch.
- Instead, build SiO_2 shield and etch contact regions.

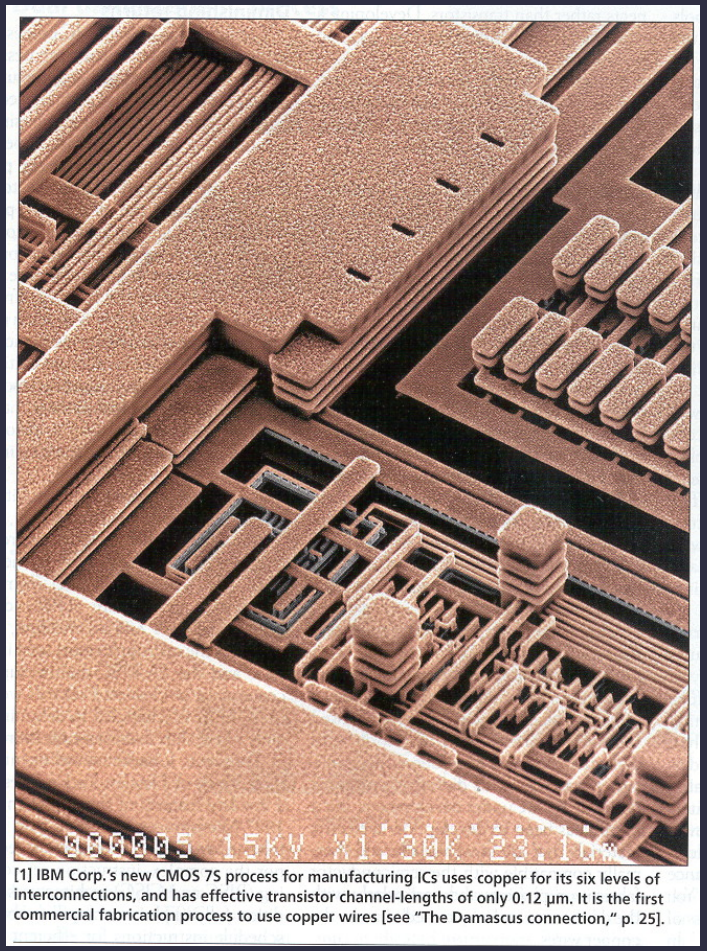
Damascene process





From IBM.

Interconnect layers



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12 µm. It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].

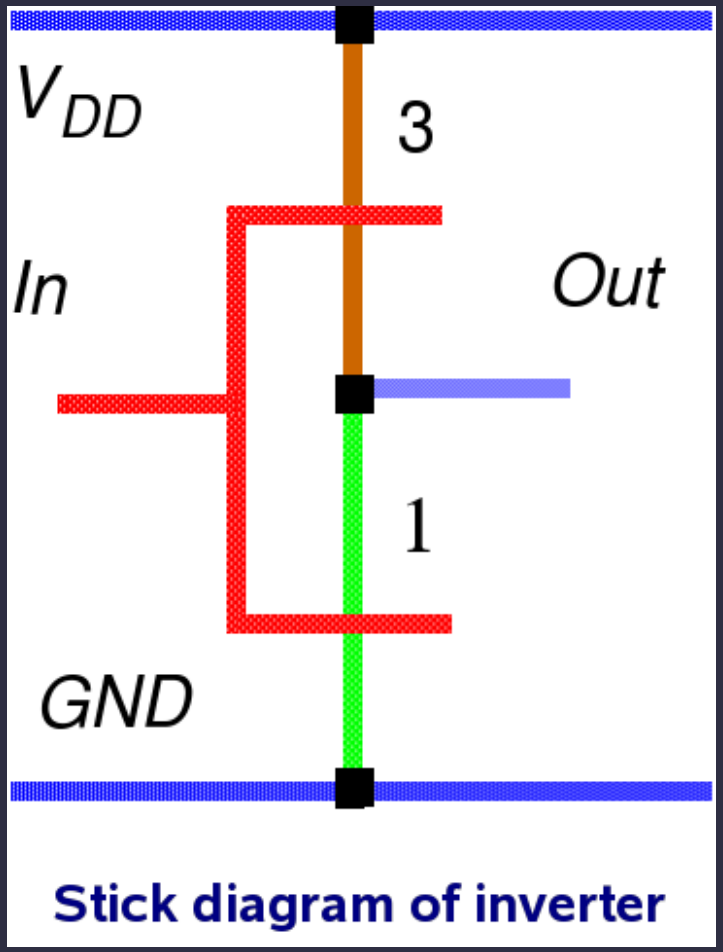
Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework

Layout production

- Must define 2-D structure for each mask/layer.
- Initial topology planning often done.
- Can be partially or fully automated.
- Must adhere to design rules.

Stick diagrams

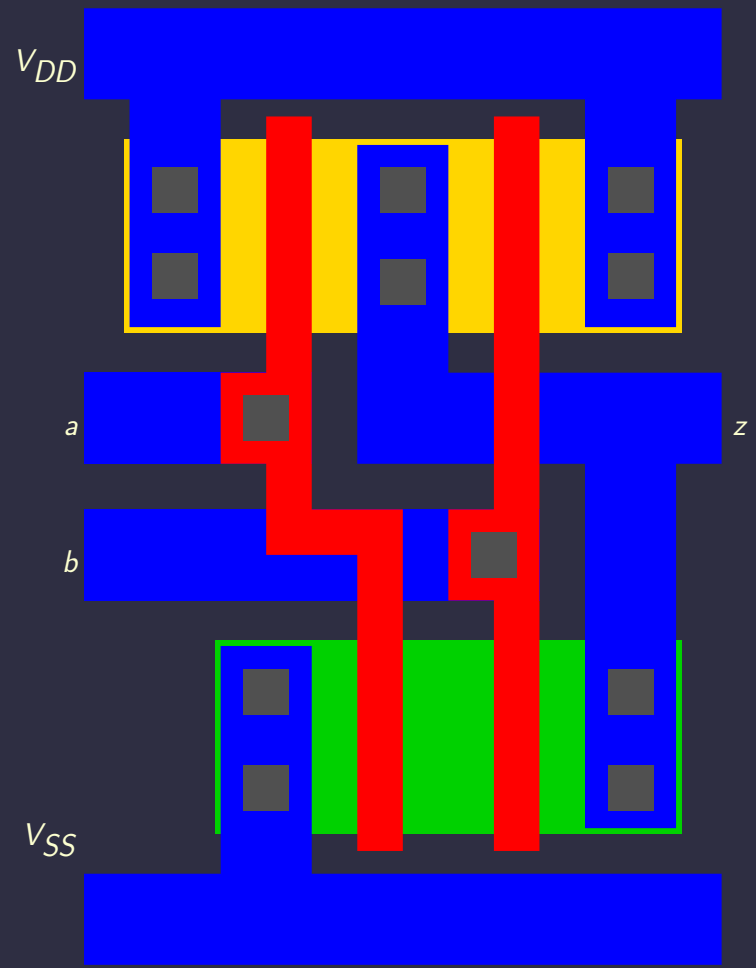


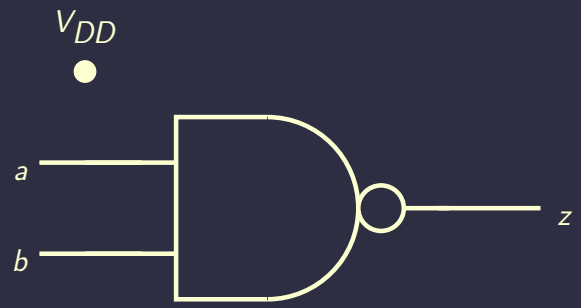
Stick diagram of inverter

Faults and variation

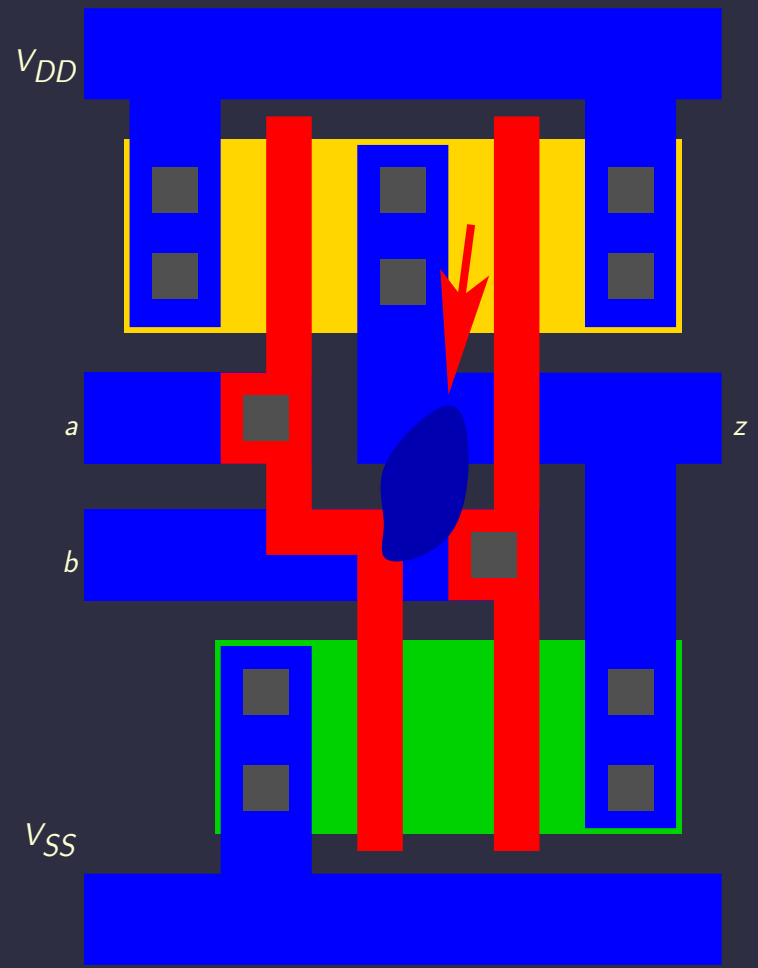
- Clearly cannot have two wires crossing each other.
- Variation imposes further constraints.

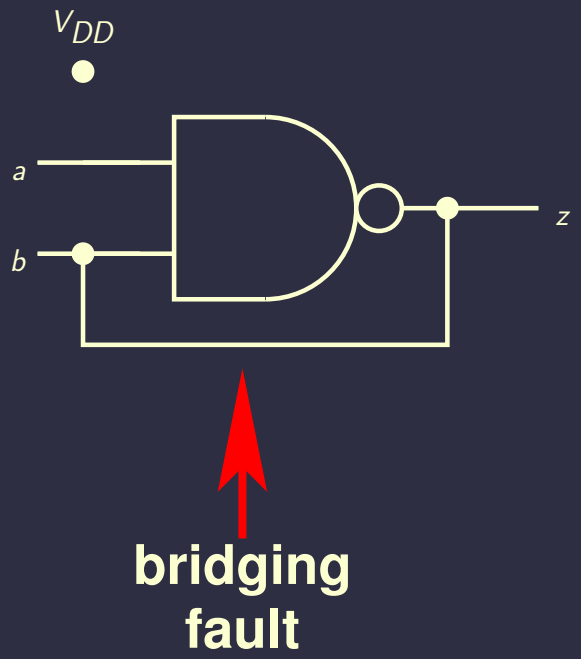
Possible faults



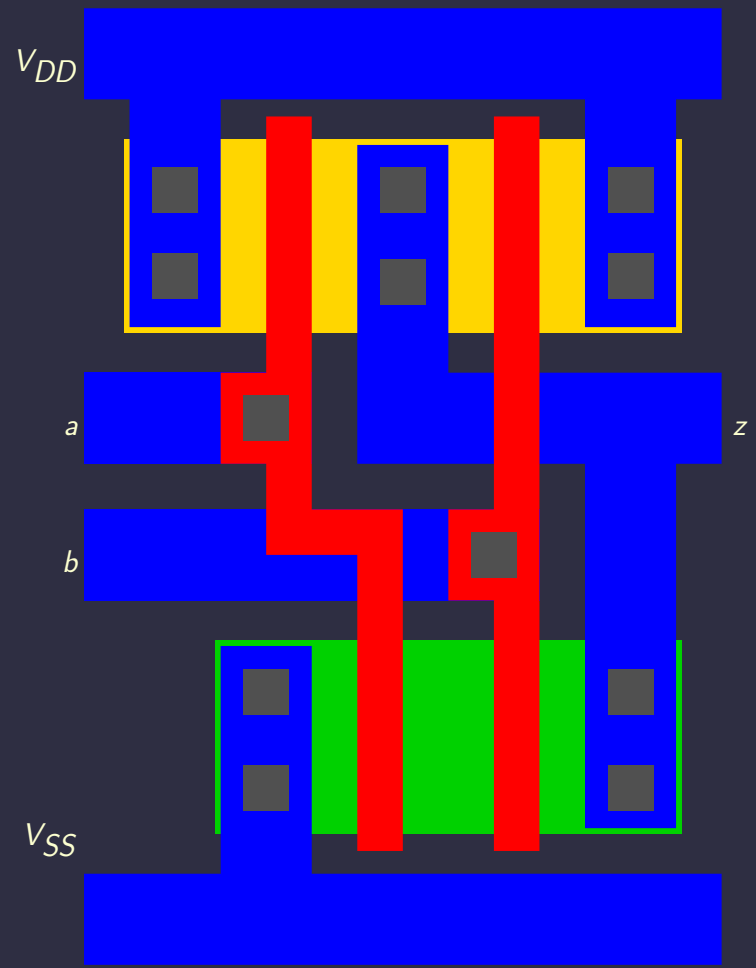


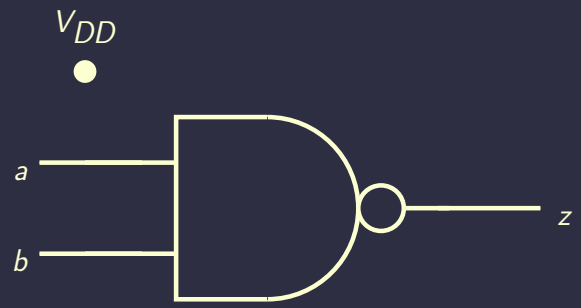
Possible faults



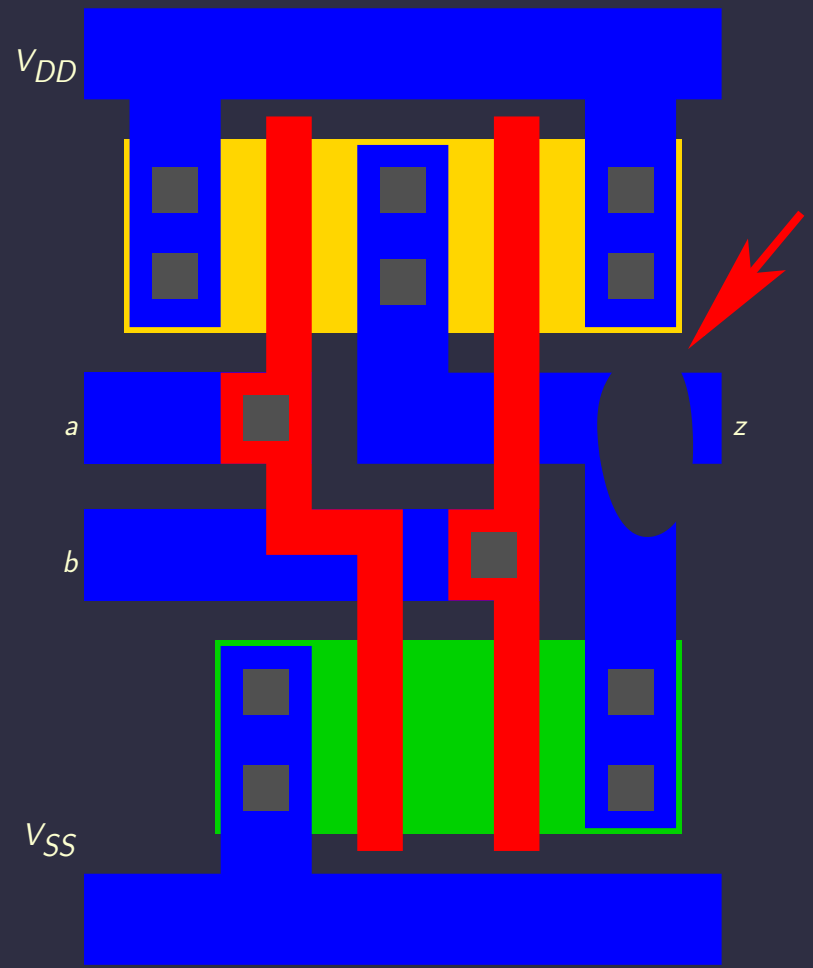


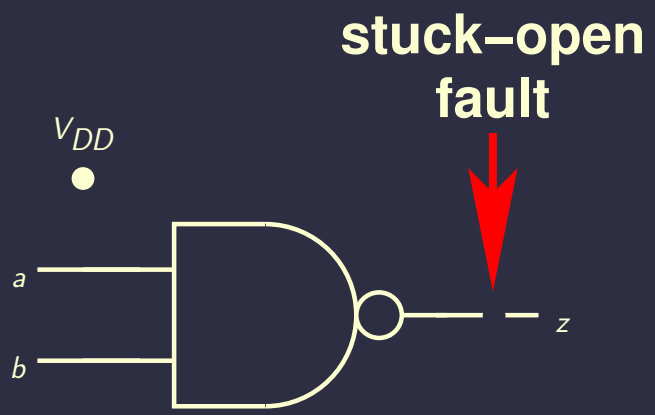
Possible faults



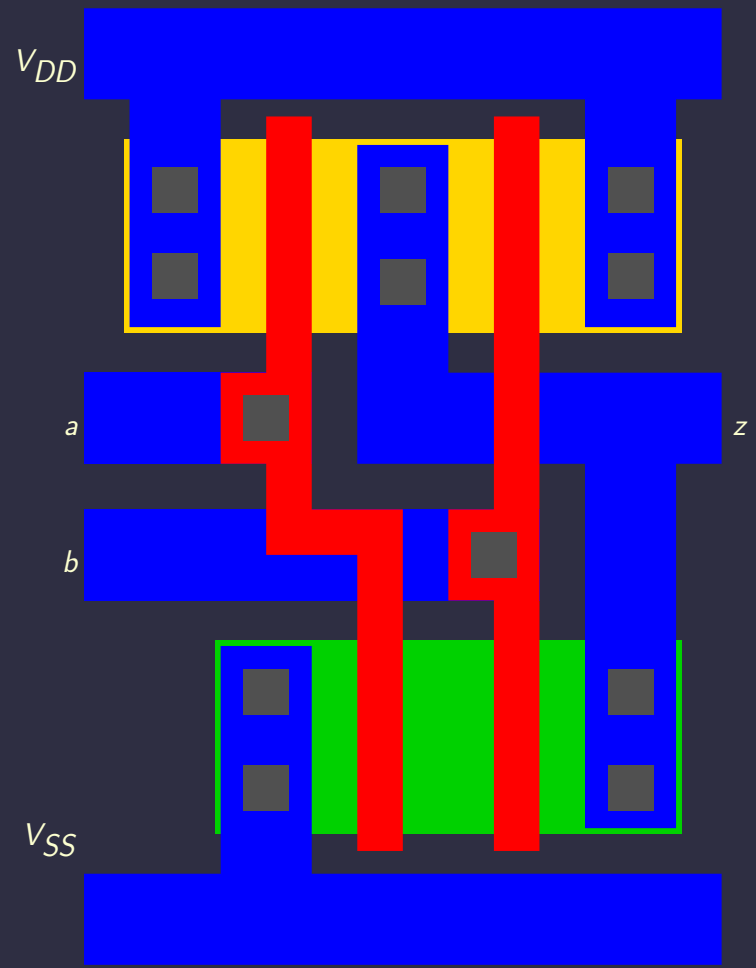


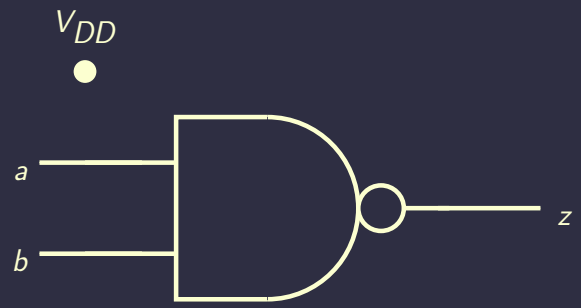
Possible faults



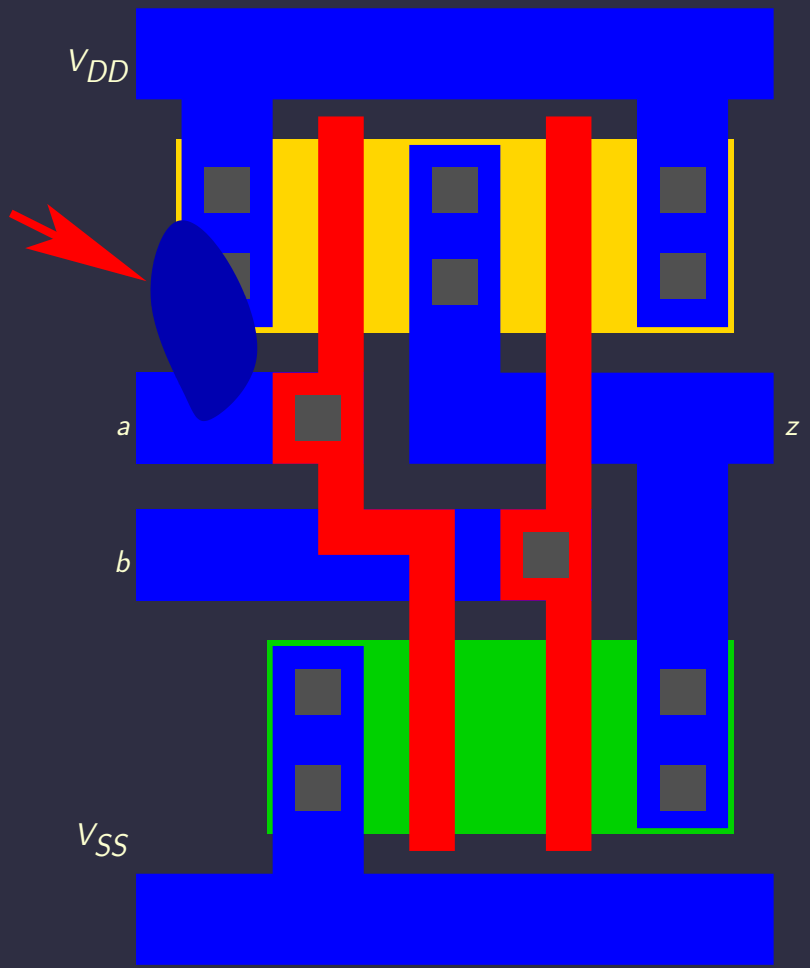


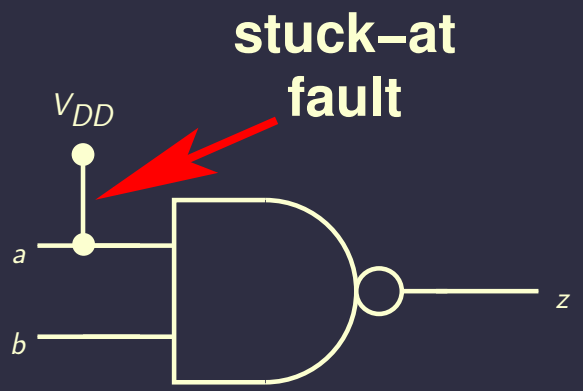
Possible faults



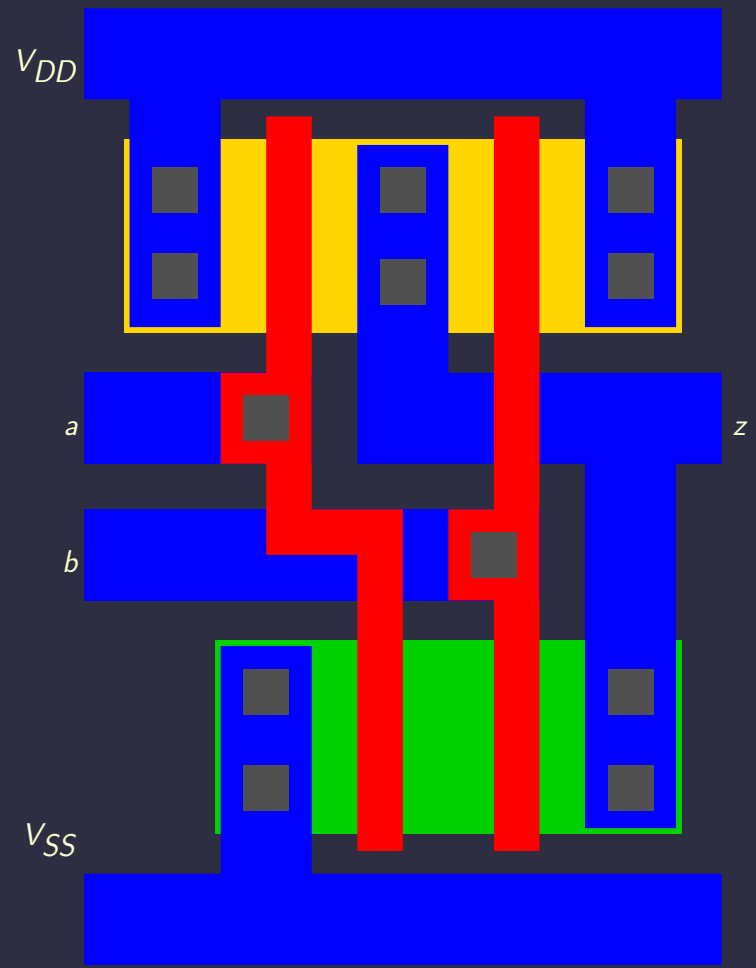


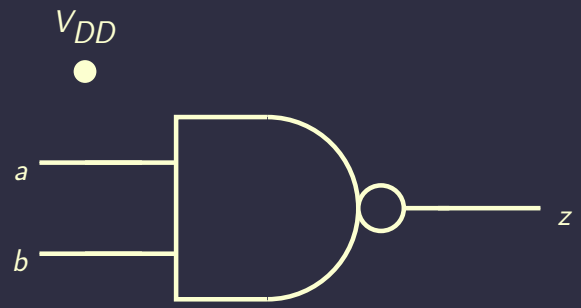
Possible faults





Possible faults





Design rules

Summary

- Automatically-checked layout rules.
- Reduce fault probabilities.
- Generally regarded as necessary.

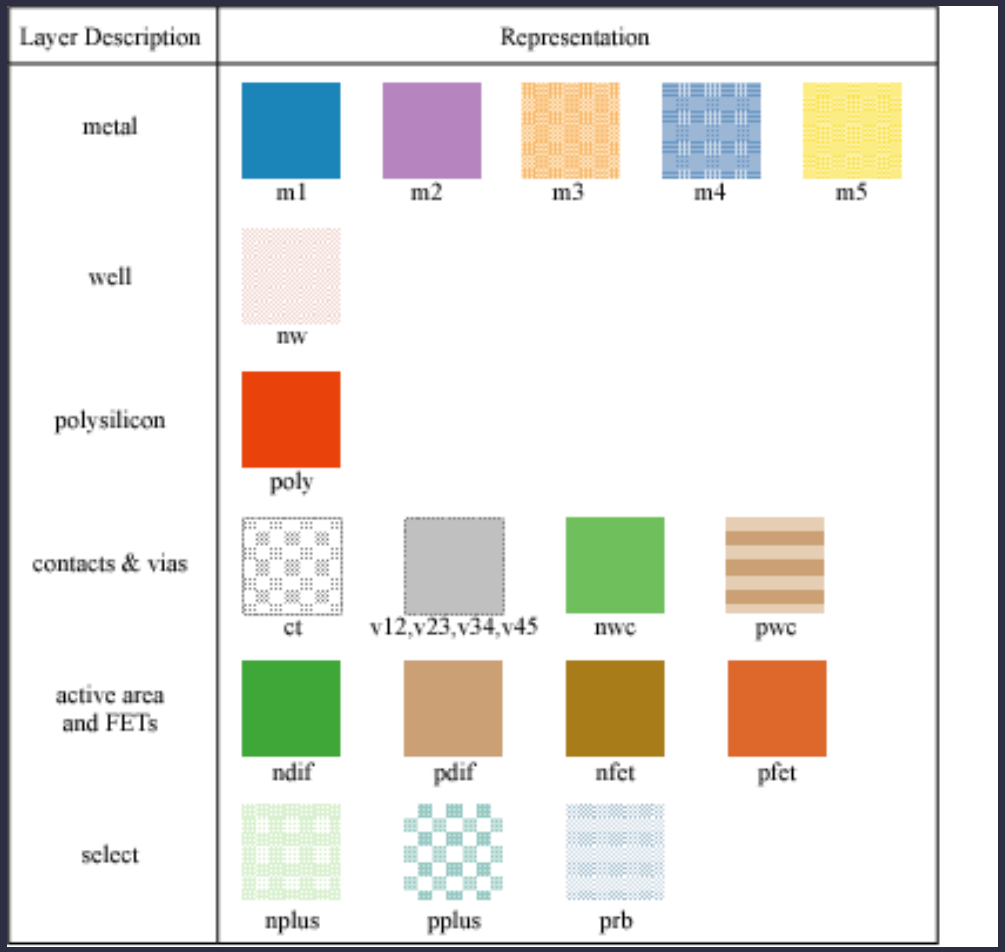
Caveats

- Recent studies show many rules are not beneficial.
- Interaction range is increasing relative to λ.
  - Complicates design rules, making manual comprehension difficult.
- Design rule checking can be slow.

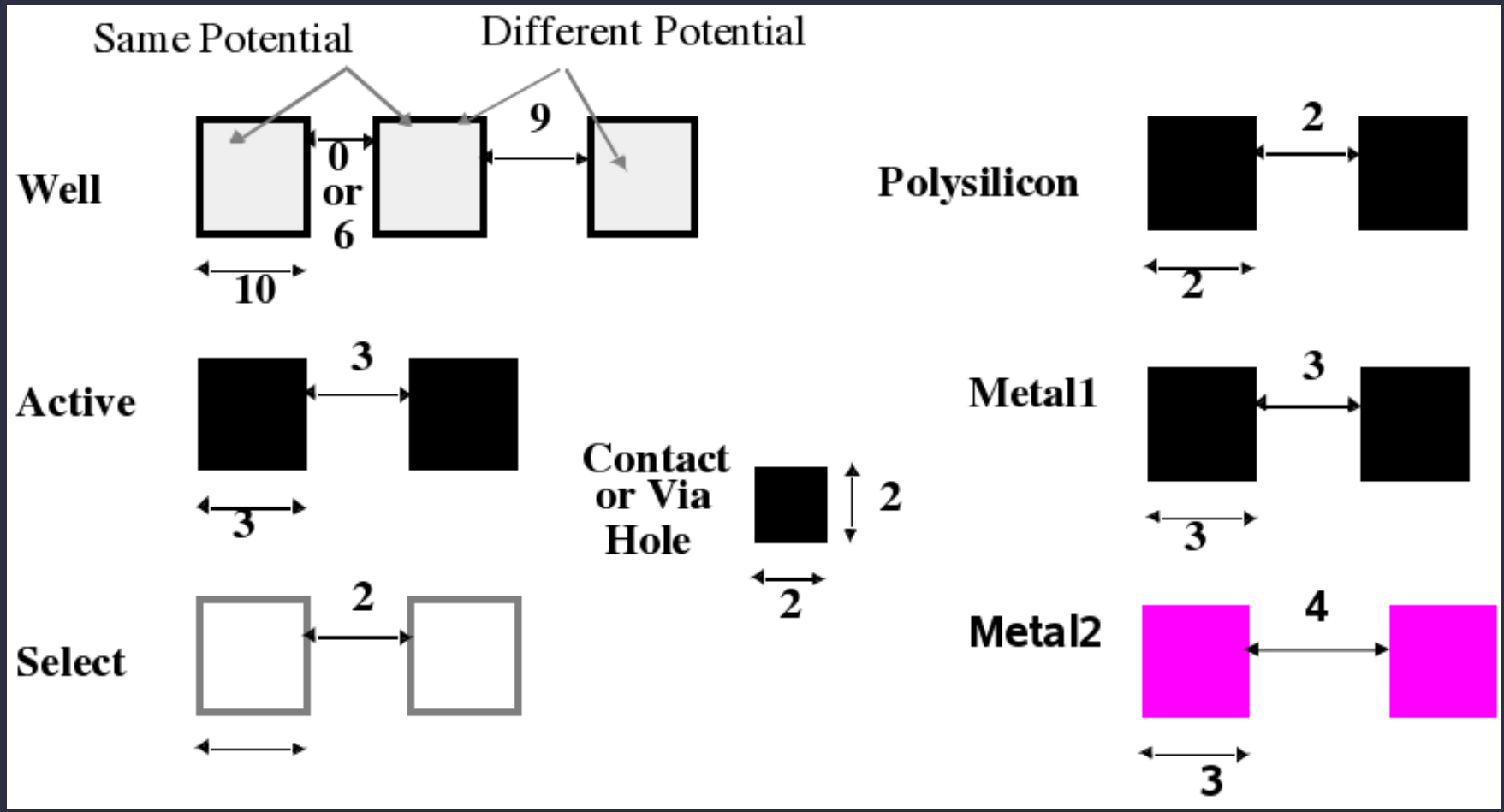
Meanings of colors in layouts

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

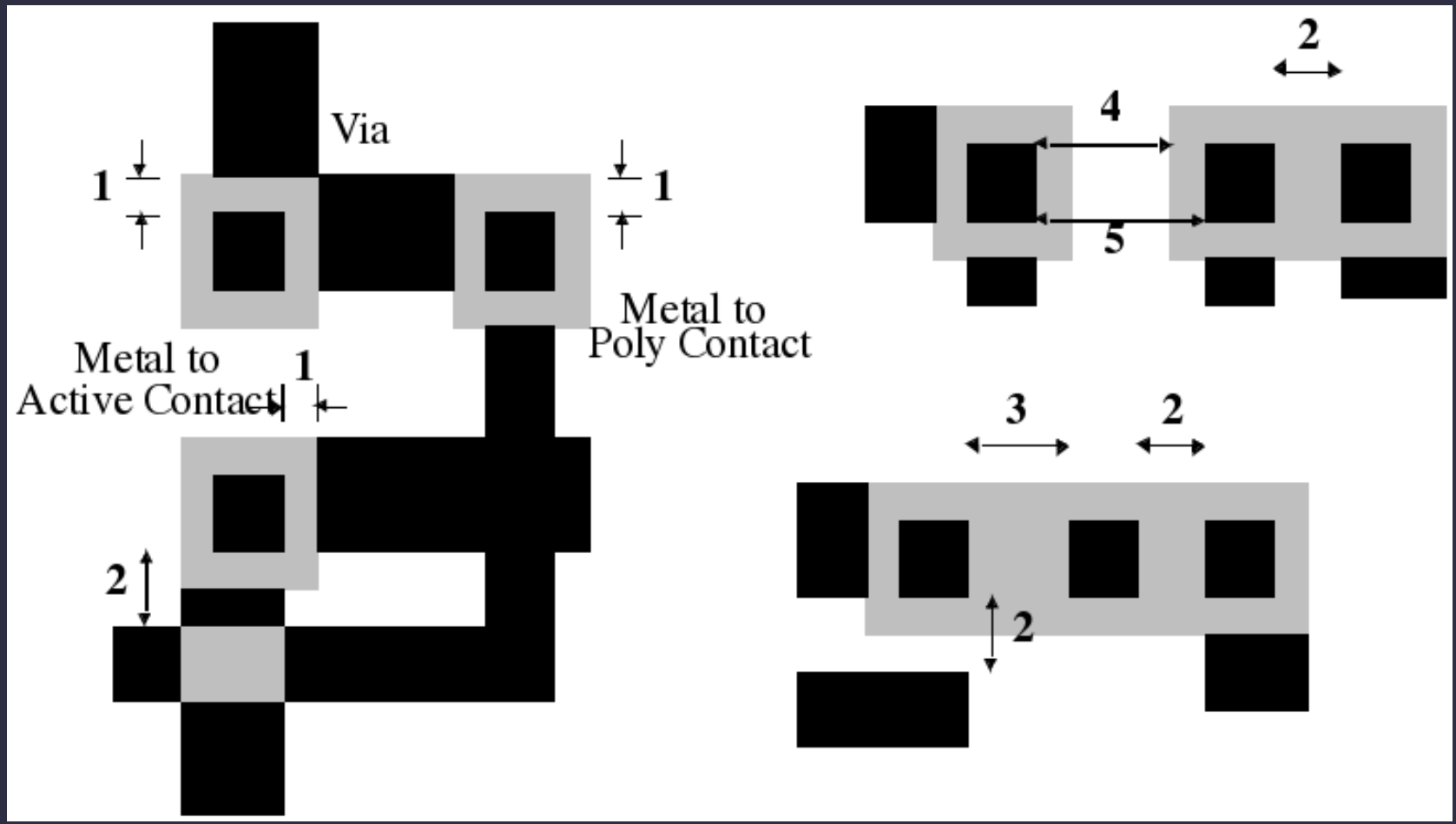
Layout layers



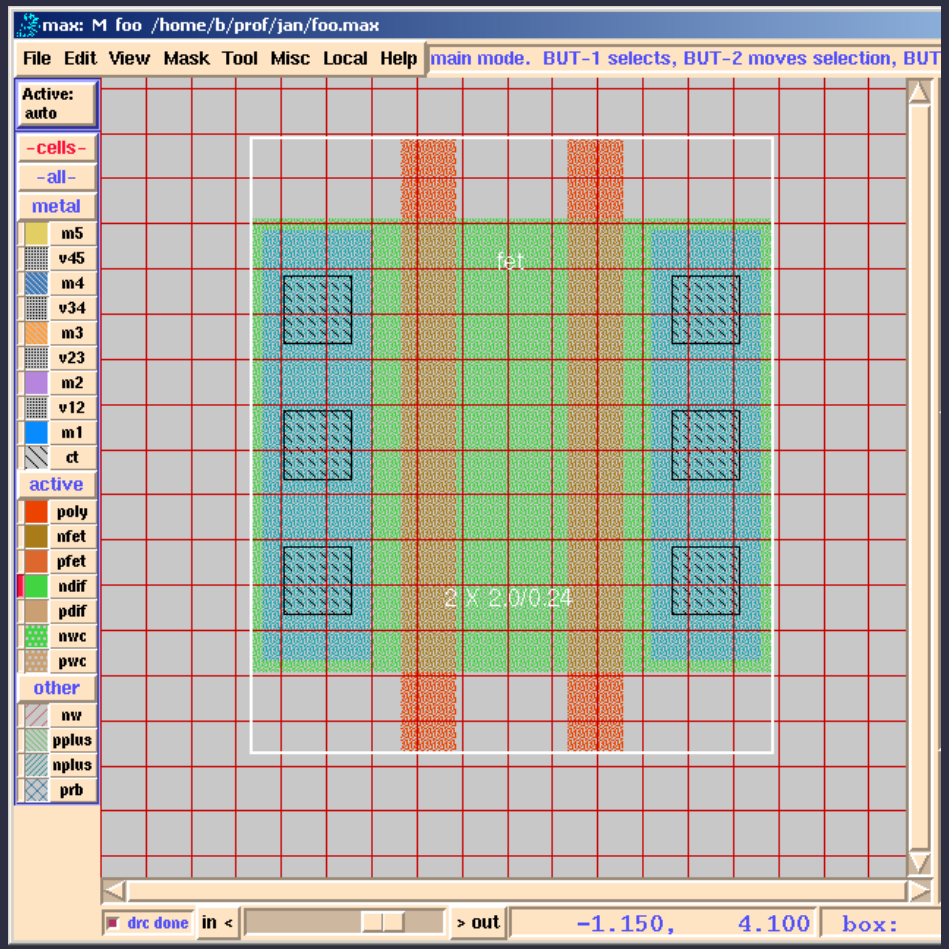
Intra-layer design rules



Via design rules



Layout editor



Design rule checker

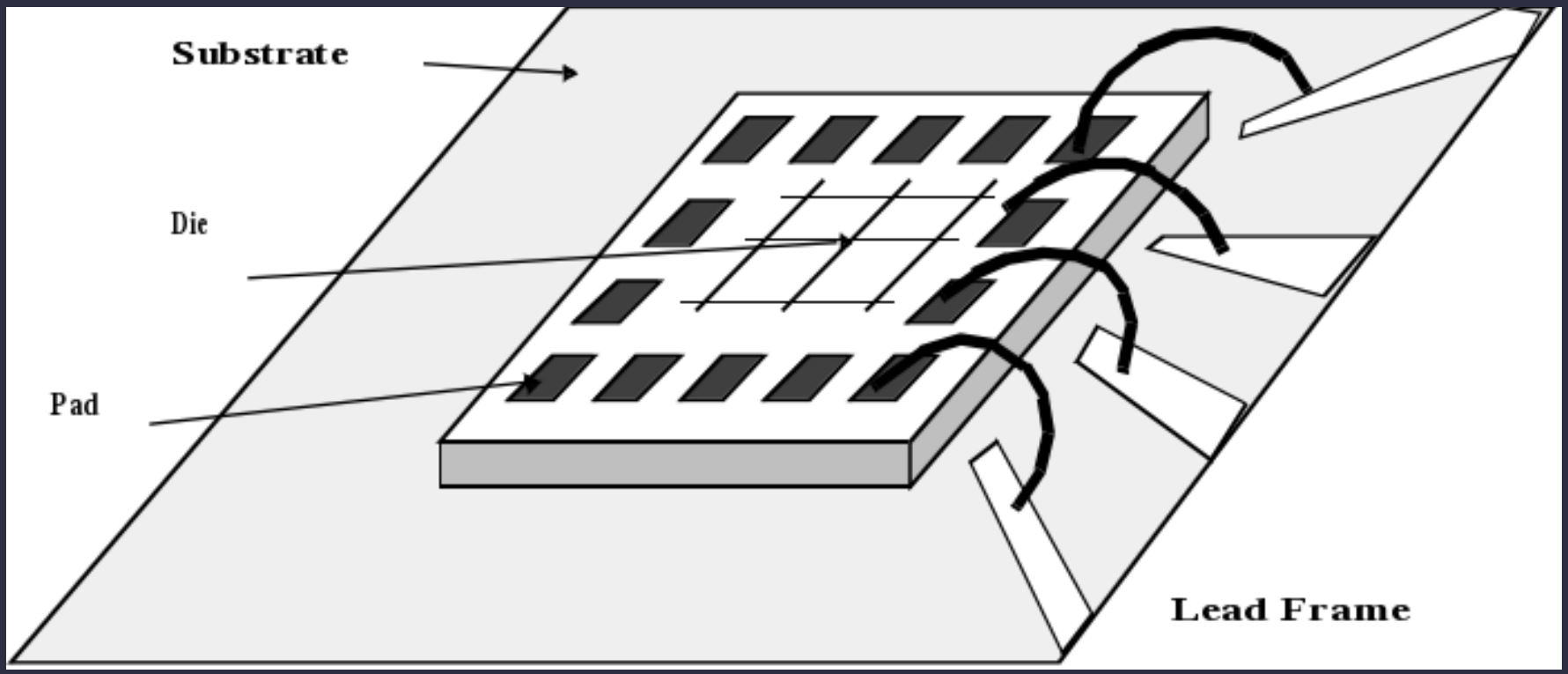
Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework

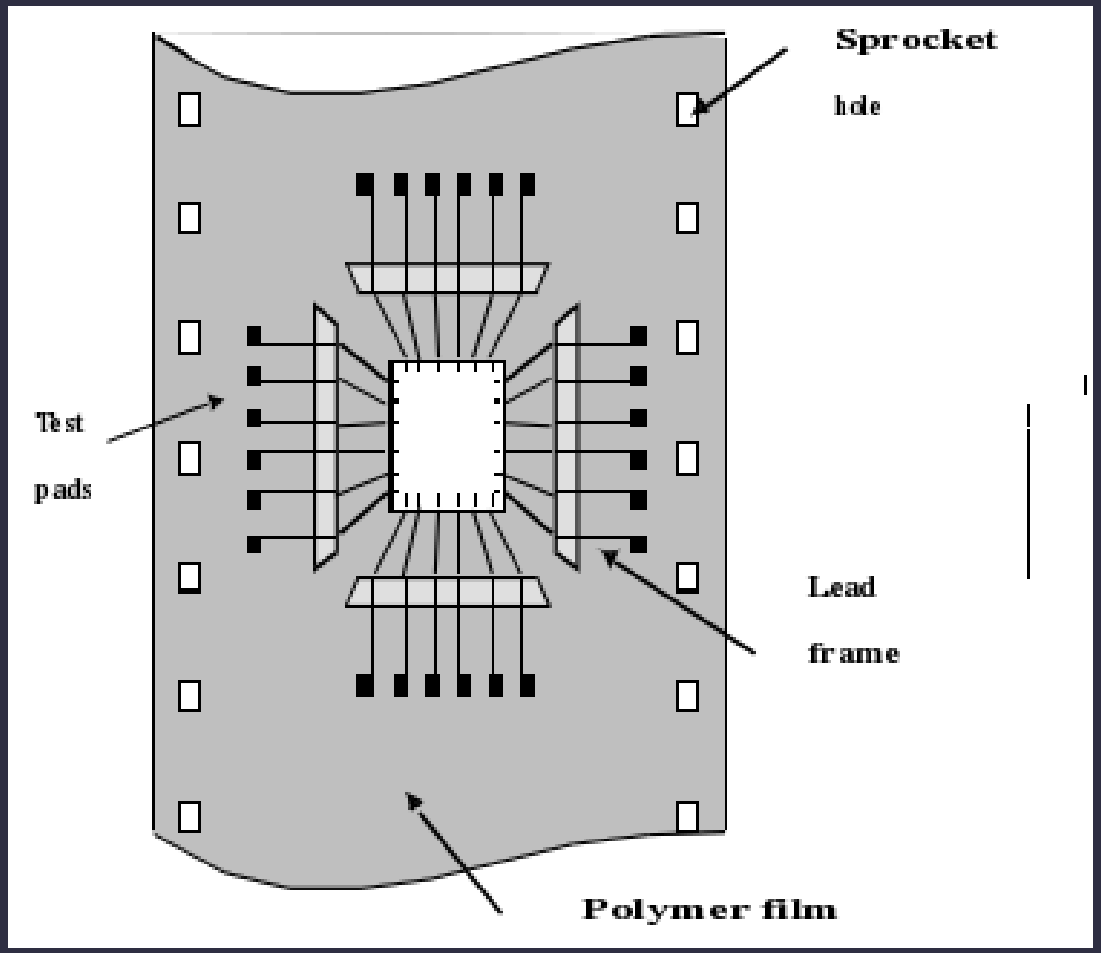
Packaging requirements

- Electrical: Good insulators and conductors.
- Mechanical: Reliable, doesn't stress IC.
- Thermal: Low thermal resistance to ambient. In some cases, consistency more important.
- Cost.

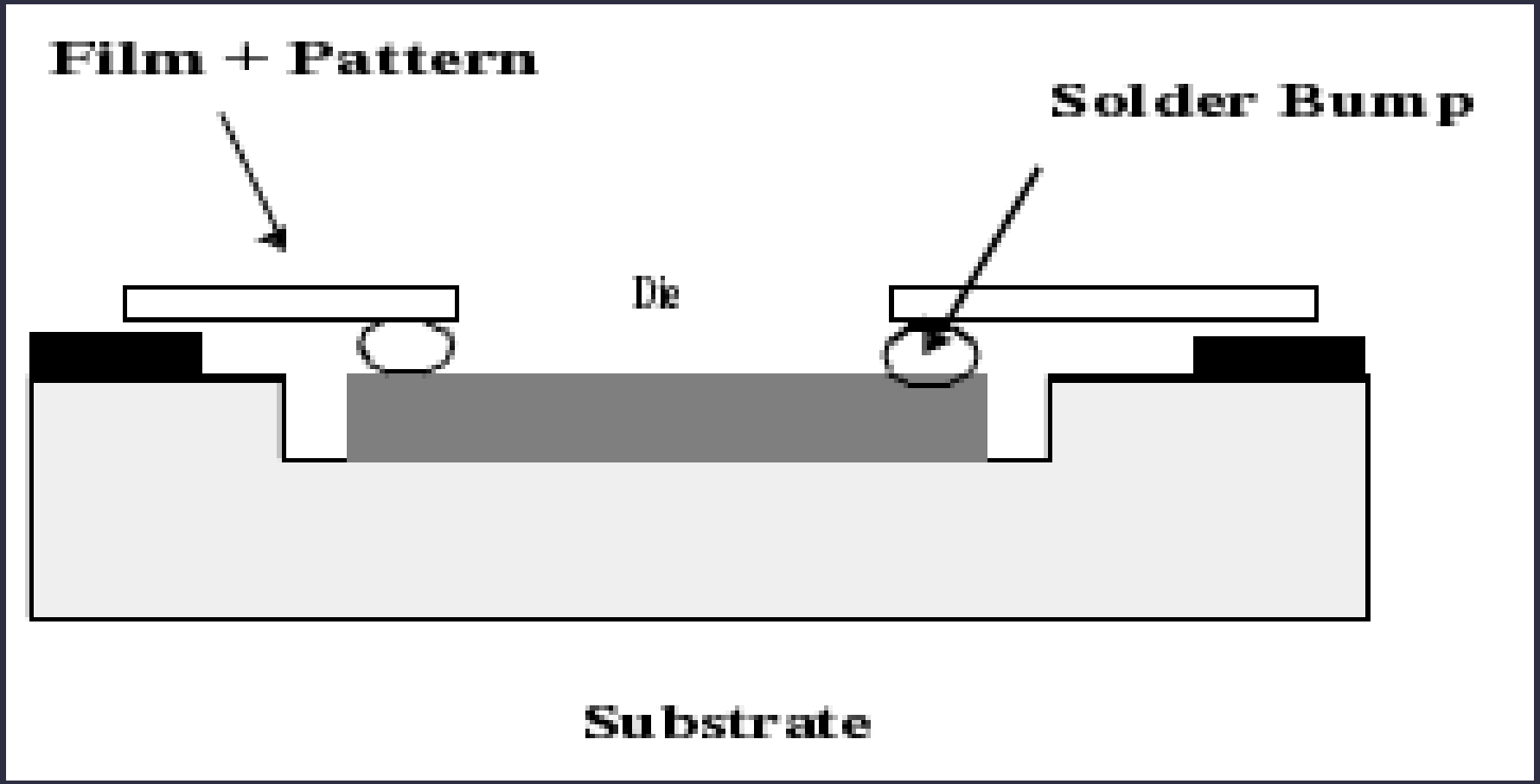
Wire bonding



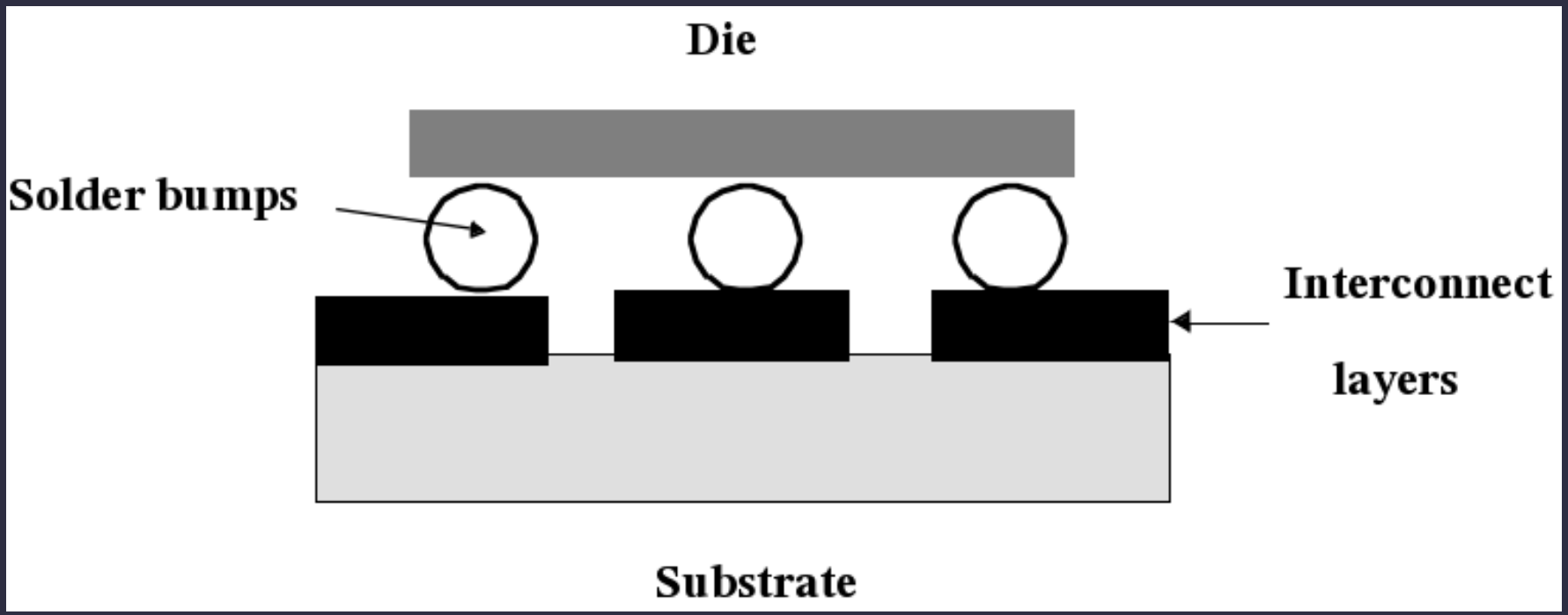
Tape automated bonding



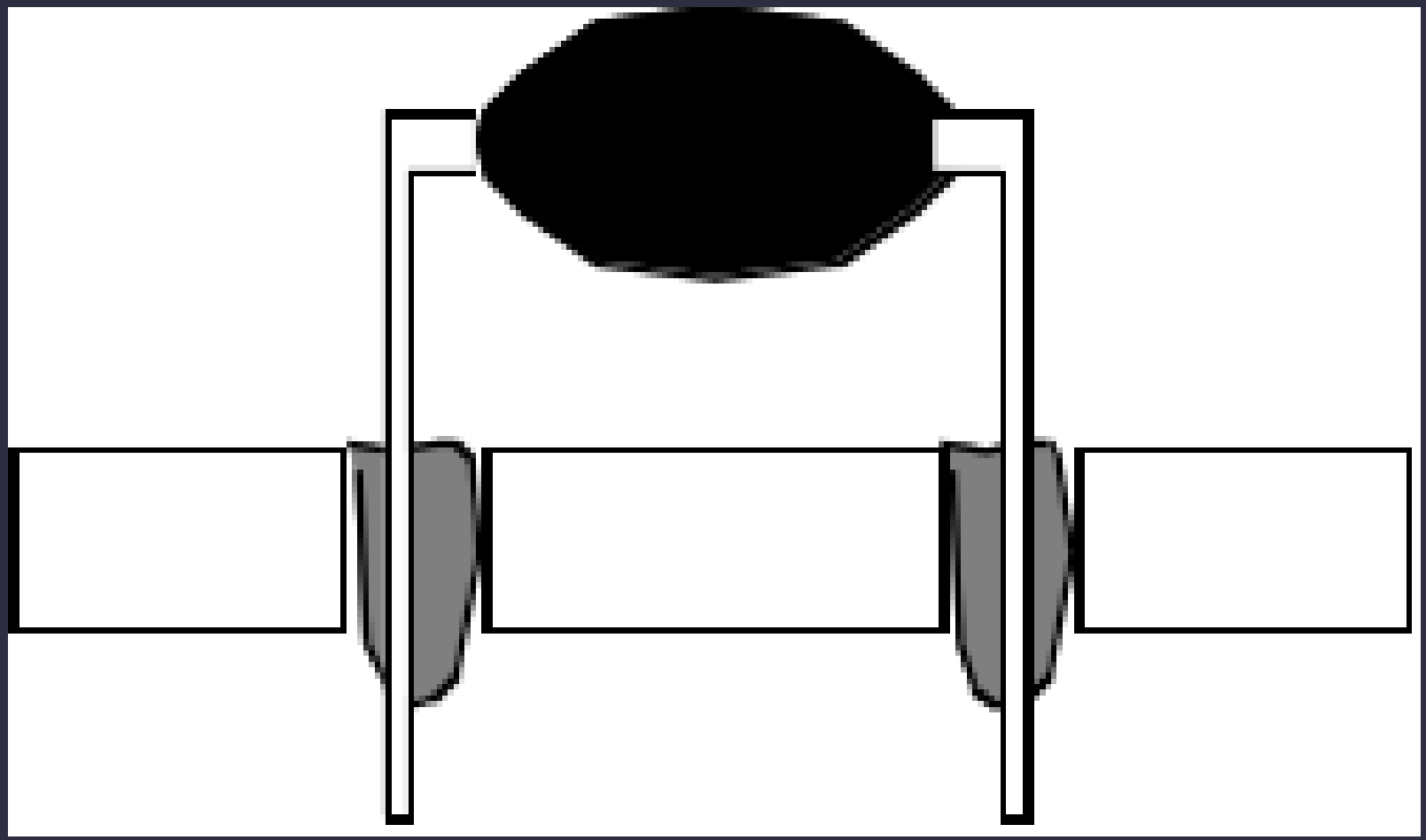
Tape automated bonding die attachment



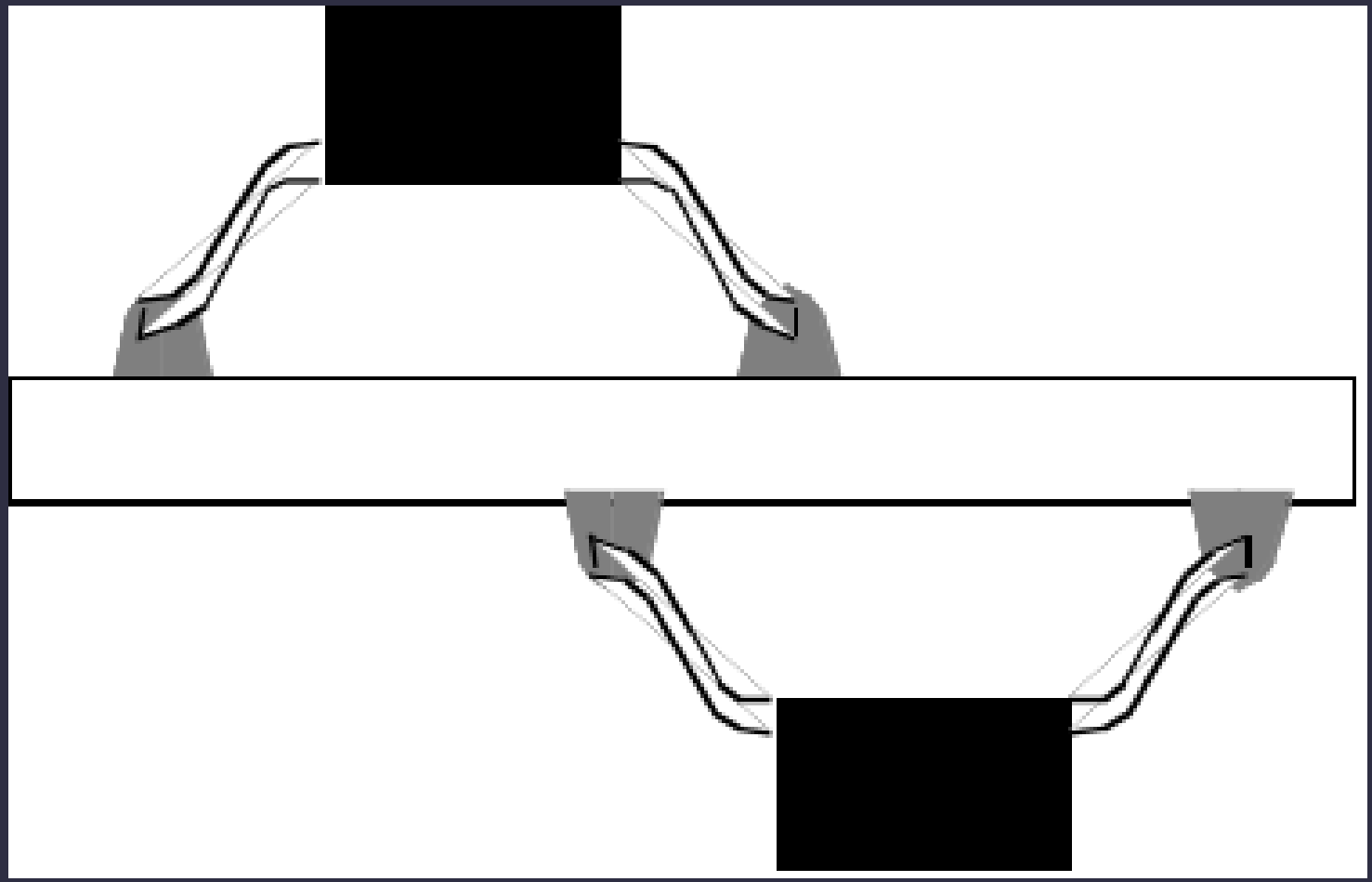
Flip-chip bonding



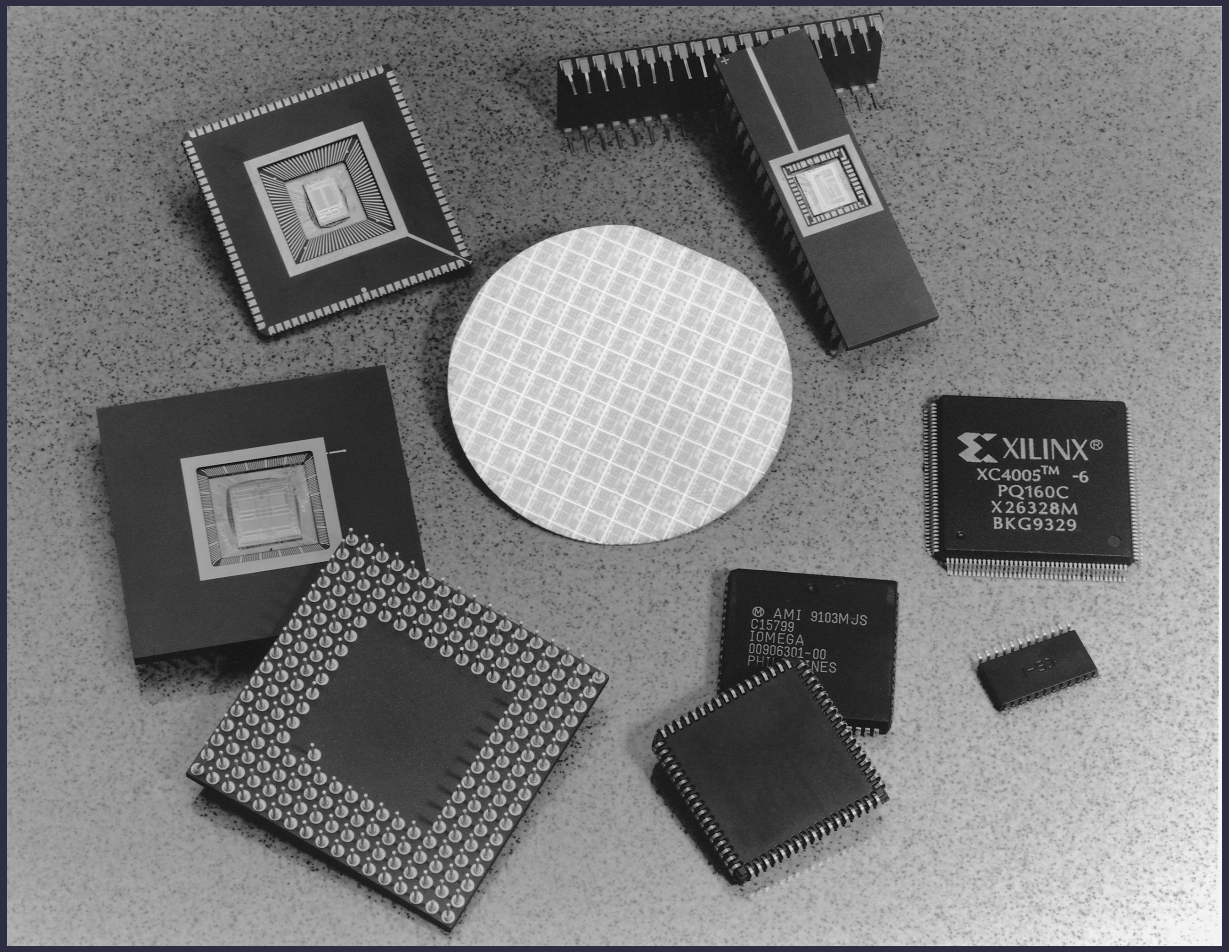
Through-hole PCB mounting



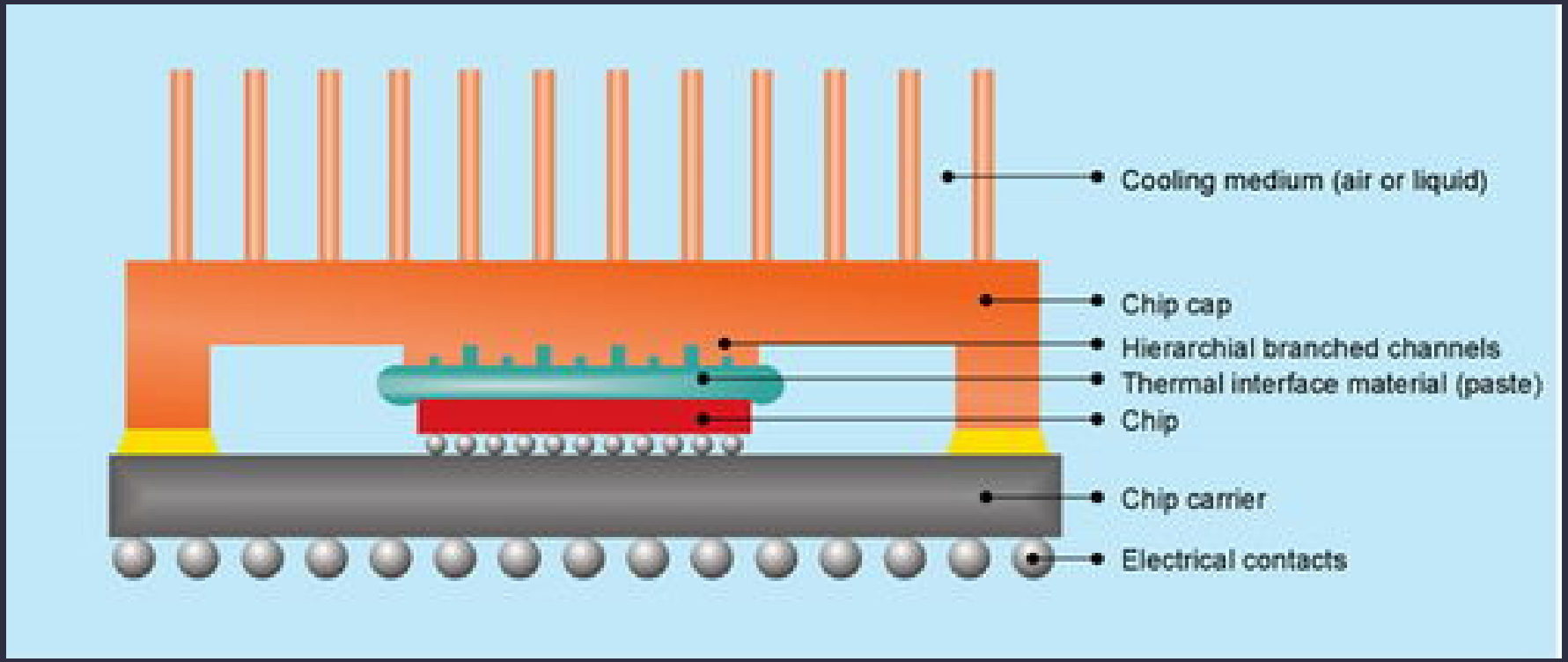
Surface mount



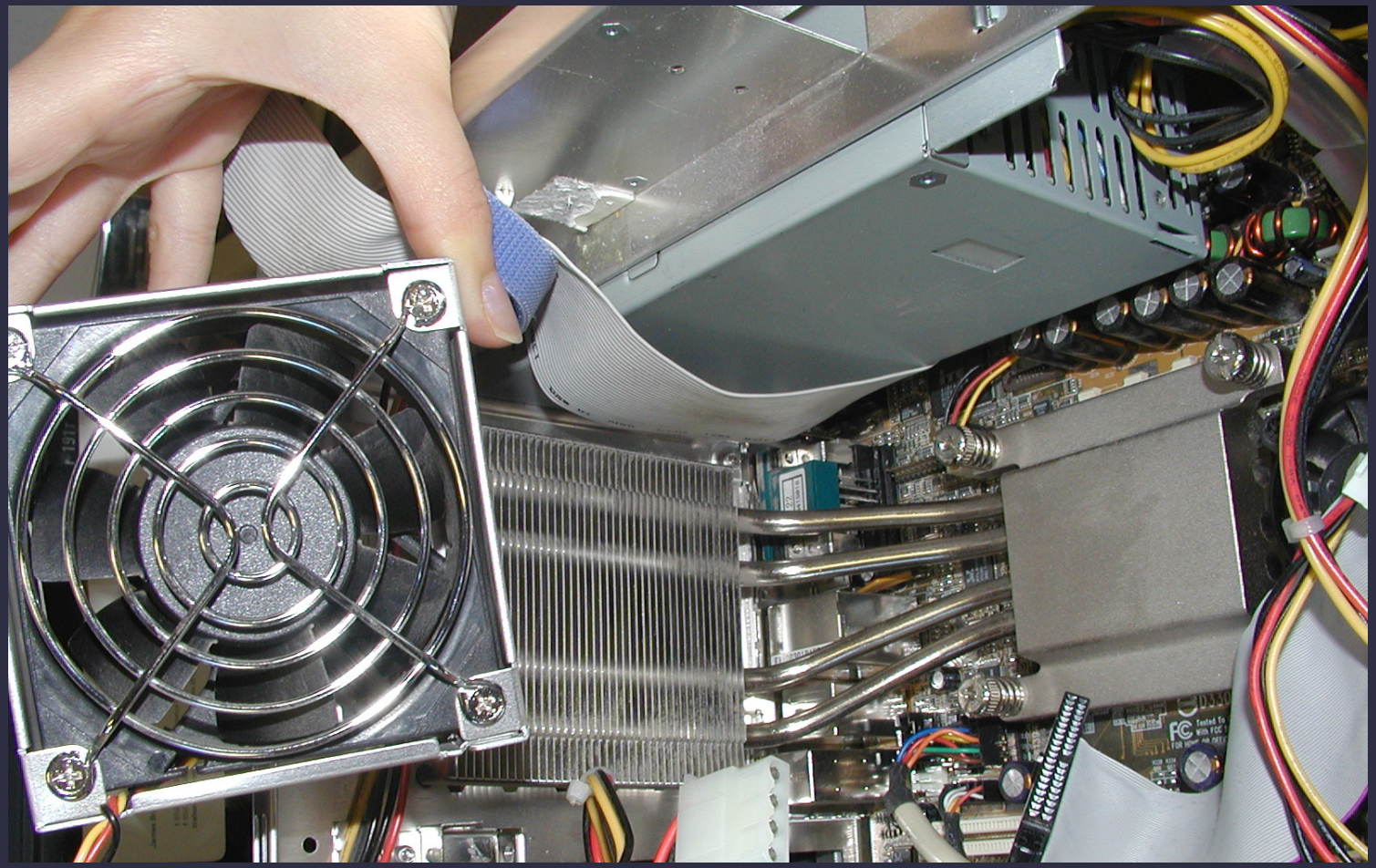
Example package types



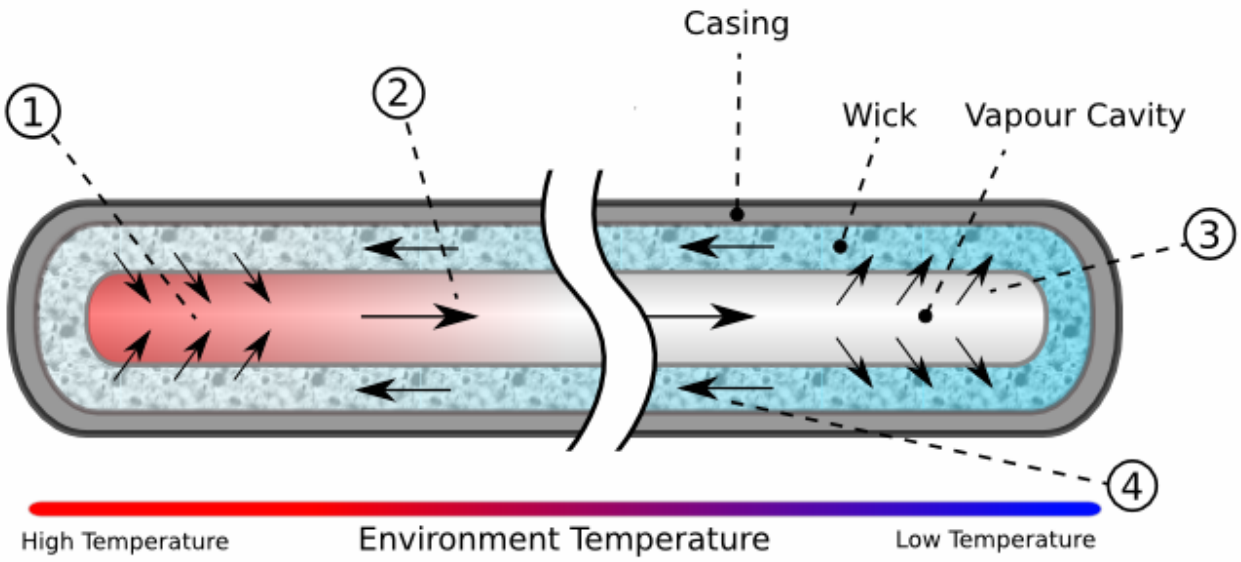
Chip cap


Cooling medium (air or liquid)
Chip cap
Hierarchial branched channels
Thermal interface material (paste)
Chip
Chip carrier
Electrical contacts

Heat pipe



Heat pipe details



Heat pipe thermal cycle

1) Working fluid evaporates to vapour absorbing thermal energy.
2) Vapour migrates along cavity to lower temperature end.
3) Vapour condenses back to fluid and is absorbed by the wick, releasing thermal energy
4) Working fluid flows back to higher temperature end.

Example of variation in package parameters

Type	C (pF)	L (nH)
68-pin plastic DIP	4	35
68-pin ceramic DIP	7	20
256-pin PGA	5	15
Wire bond	1	1
Solder bump	0.5	0.1

System-on-chip

- Instead of integrating more ICs, put more on an IC.
- Advantages: Lower cost per device, compact.
- Disadvantages: Requires integration of devices fabricated with different processes.

Move from lead solder

- Tin–lead solder was commonly used.
- Lead is toxic, accumulates in the body, and is difficult to dispose of.
- Pure tin works in the short term.
- May be acceptable as solder in the long term.
- Problems with plating.

Tin whiskers

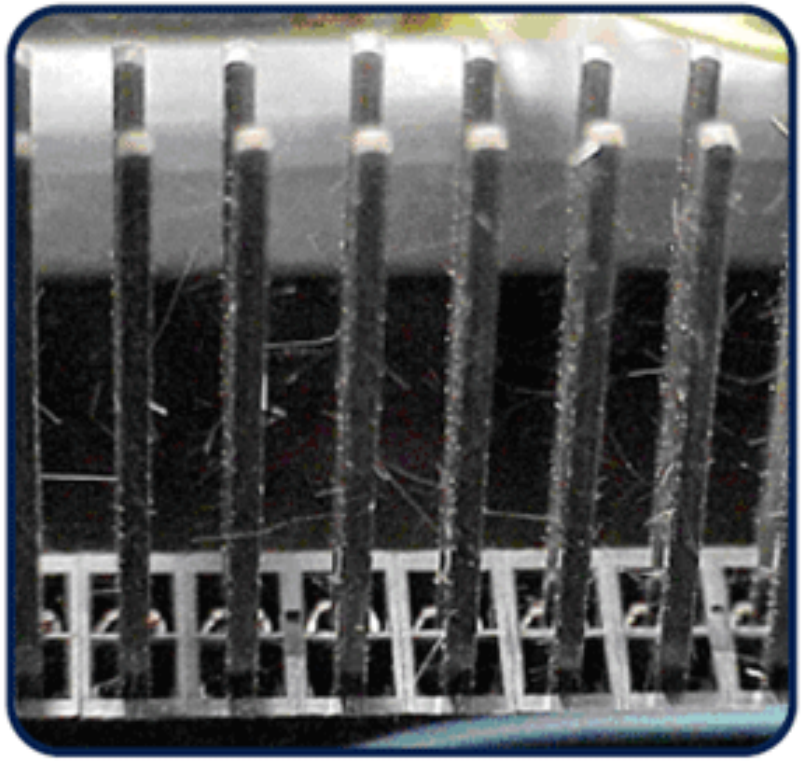
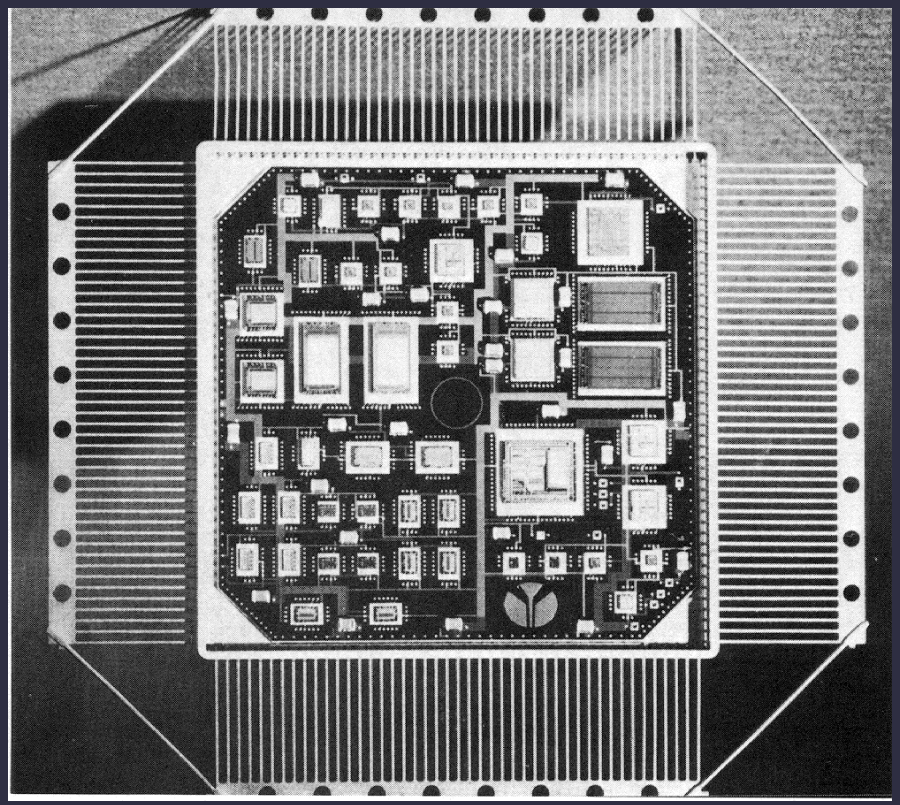


Figure 1-1 – Tin plated connector pins after 10 years
(courtesy of NASA GSFC)

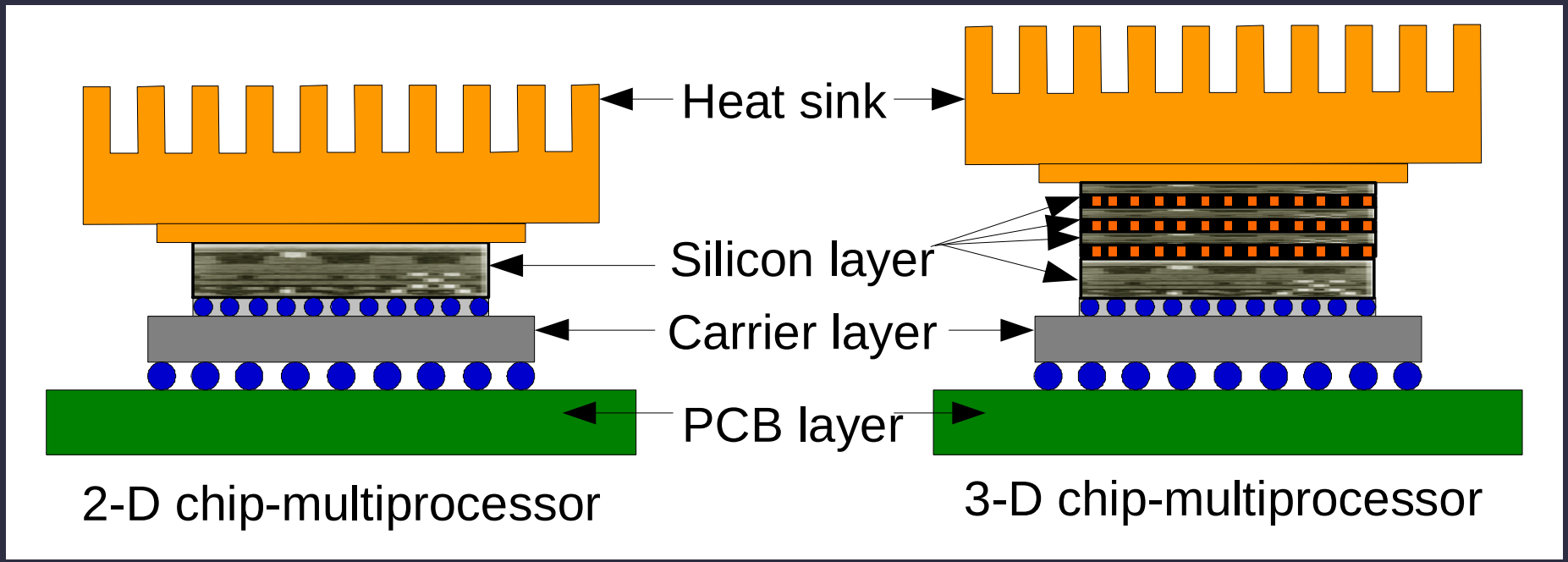
Screw dislocations, primarily caused by plating.

Multi-chip modules



- Better C than board-level integration.
- Integrate multiple processes.
- Somewhat compact.
- Expensive.

Multiple active layer 3-D integration



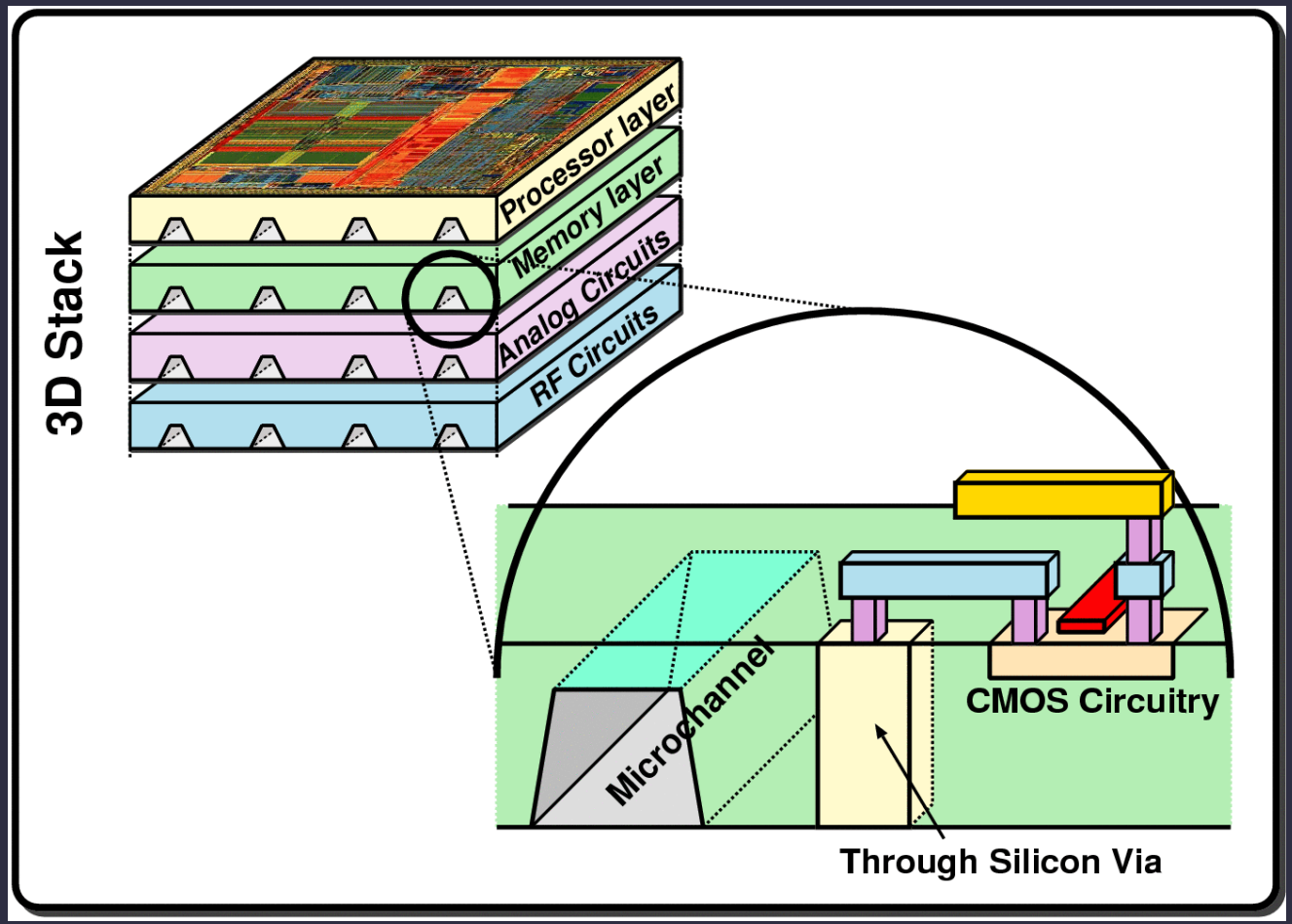
Potential for thermal problems.

Heterogeneous system 3-D integration

Integrate

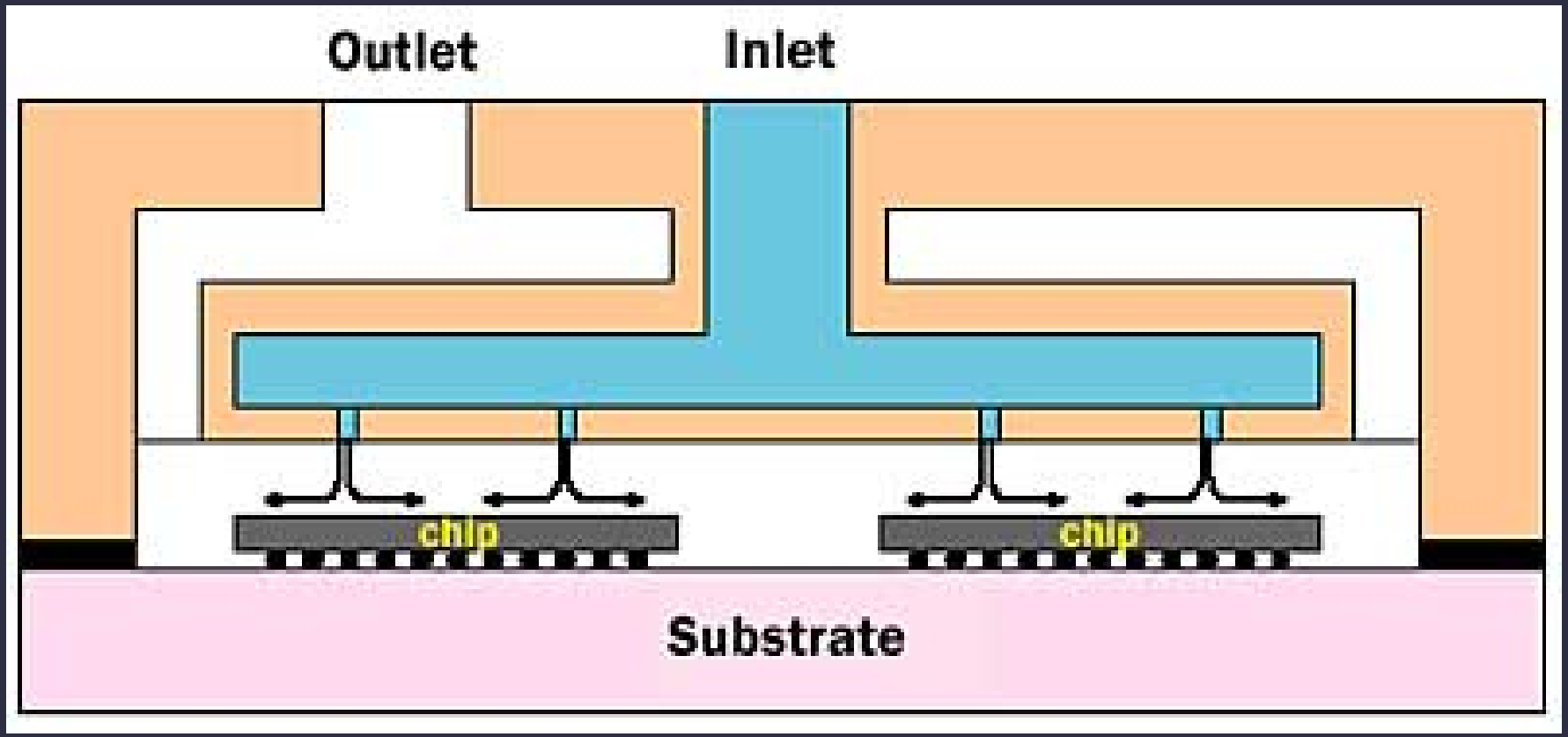
- Logic.
- Memory.
- Analog.
- Research on discrete components (with soldering).

Microchannel cooling



Credit to David Atienza at EPFL.

Vapor-phase cooling



Credit to Michael J. Ellsworth, Jr. and Robert E. Simons at IBM.

Summary

- CMOS is the most economical way to build digital logic now, but potential alternatives being developed.
- Fabrication process is essentially repeated deposition, masking, etching, and polishing steps to dope and build material layers.
- Al$\rightarrow$Cu.
- $SiO_2 \rightarrow$ High-κ and Low-κ.
- Cu interconnects use damascene process.
- Poly-Si$\rightarrow$metal.

Upcoming topics

- MOSFET dynamic behavior.
- Wires.
- CMOS inverters.

Lecture plan

1. Device trends
2. Fabrication
3. Layout and design rules
4. Packaging and board-level integration
5. Homework

Homework assignment

- 24 September: Read Mark T. Bohr, Robert S. Chau, Tahir Ghani, and Kaizad Mistry. The High-k Solution. *IEEE Spectrum*, October 2007.
- 24 September: Homework 1.
- 3 October: Lab 2.