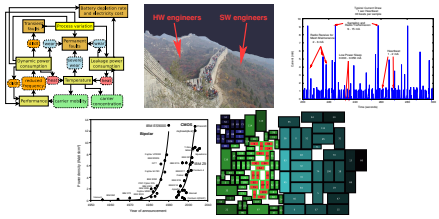
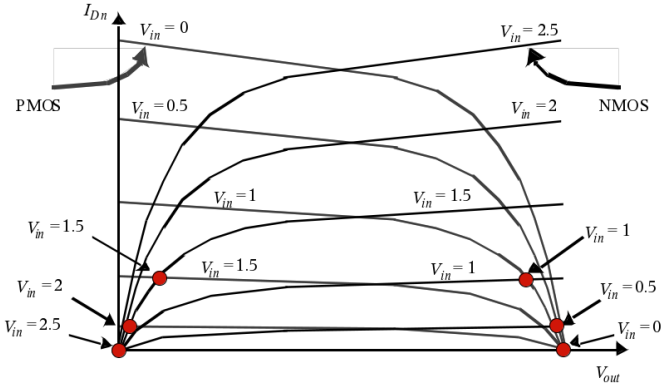
Digital Integrated Circuits – EECS 312

http://robertdick.org/eecs312/

Teacher:	Robert Dick	GSI:	Shengshou Lu
Office:	2417-E EECS	Office:	2725 BBB
Email:	dickrp@umich.edu	Email:	luss@umich.edu
Phone:	734–763–3329		
Cellphone:	847–530–1824		



Review I



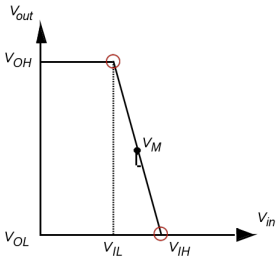
Review II

- How can the transfer curve for an inverter be derived from the I–V curves of the MOSFETs comprising it?
- What useful property relevant to the inverter load curve diagram holds in steady state but not when transients are considered?
- Is the inverter load curve diagram useful for analyzing dynamic systems?

Midterm exam

- May cover anything up to and including 3 October.
- Make sure you did the assigned reading.
- Look though all the on-line slides for anything surprising.
- Review lab and homework assignments.
- If you want to study with other students, please use mailing list to find partners.
- Posted old exams to website.
- No class on Tuesday.

V_{IH} and V_{IL}



$$V_{IH} - V_{IL} = -\frac{V_{OH} - V_{OL}}{g} = \frac{-V_{DD}}{g} \quad (1)$$

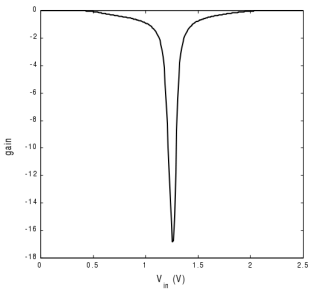
$$V_{IH} = V_M - \frac{V_M}{g} \quad (2)$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} \quad (3)$$

$$NM_H = V_{DD} - V_{IH} \quad (4)$$

$$NM_L = V_{IL} \quad (5)$$

Inverter gain

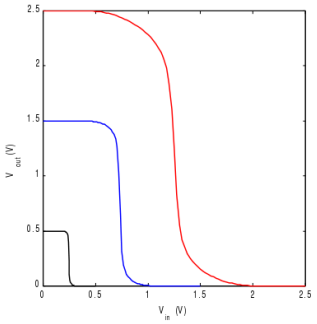


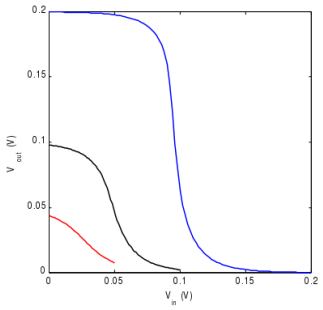
Can find gain by taking $\sigma V_{out}/\sigma V_{in}$ at V_M.

$$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \quad (1)$$

$$g \approx \frac{1 + r}{\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right)(\lambda_n - \lambda_p)} \quad (2)$$

Change in transfer curve (and gain) with V_{DD}

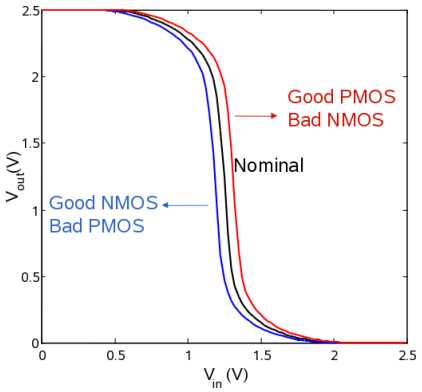




Subthreshold operation

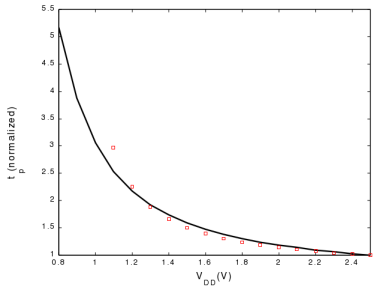
- Higher gain.
- Lower current.
- Increased sensitivity to intrinsic noise.
- Increased sensitivity to fixed external noise.
  - $\frac{xkT}{q}$

Impact of process variation on inverter transfer function



Inverter performance

- Recall inverter propagation delay expression: $t_p = 0.69RC$.
- Either decrease R or decrease C.
- Effective R depends on V_{DD}.



Dependence of inverter delay on V_{DD} I

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}}$$

$$t_{pHL} = 0.52\frac{L_n}{W_n}\frac{C_L V_{DD}}{k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

If $V_{DD} \gg V_{Tn} + V_{DSATn}/2$

$$t_{pHL} \approx 0.52\frac{L_n}{W_n}\frac{C_L}{k'_n V_{DSATn}}.$$

Why?

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

Dependence of inverter delay on V_{DD} II

where

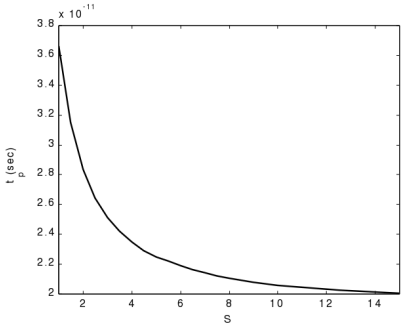
$$I_{DSAT} = k'\frac{W}{L}\left((V_{DD} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right).$$

Ignore channel length modulation factor λ.

Review

- Define noise margin and explain why it is a useful concept.
- What is V_M?
- What influence does an asymmetric change in inverter MOSFET resistance have on the V_{out}–V_{in} curve?
- What is inverter gain and how does it depend on V_{DD}?
- What happens to inverter delay with decreasing V_{DD}?

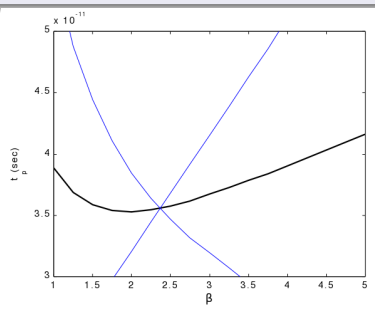
Dependence of delay on width (R)



- Fix $R_L C_L$ and vary W.
- Eventually, self-loading dominates.

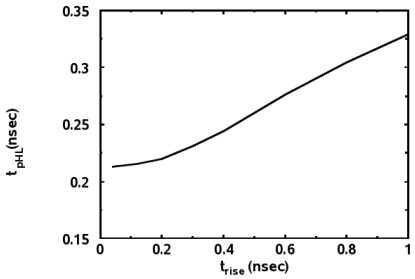
Impact of W_p/W_n ratio

Warning: Broken concept, especially for short-chain analysis.



- $\beta = W_p/W_n$.
- $t_p = \frac{t_{pLH}+t_{pHL}}{2}$.

Impact of rise time on delay



Modeling rise time effects in inverter chains

$$t_p^i = t_{step}^i + \eta t_{step}^{i-1}$$

- t_{step}^i: Delay of gate i in response to step input function.
- η: Technology-dependent constant, generally near 0.25.

Midterm exam I

1. Uses of digital systems.
2. History of digital computing devices. Impact of technology improvements on performance, power consumption, size, and reliability. Bipolar to CMOS move.
3. Power consumption equation and components of total power consumption. Check Slide 19 in lecture notes packet 2.
4. Requirements for devices to permit use in digital system. Regeneration/restoration.
5. MOSFET structure and layout.
6. Schematic capture, e.g., using Cadence software.
7. Resistance basics, and their application to MOSFET channels and metal wires.

Midterm exam II

8. Basic logic gate and transmission gate structures.
9. NMOS, PMOS, and CMOS inverters.
10. Diode structure and operation. Drift and diffusion. Difference between charge carriers and stationary ions. Doping.
11. MOSFET operation. Change in conditions (especially I_D) with changing V_{GS}, V_{DS}, and V_{SB}. MOSFET models. Cutoff, pinch-off, and velocity saturation.
12. Subthreshold leakage and subthreshold operation.
13. Process variation definition and influence on circuit behavior.
14. High-level understanding of FinFET structure and reason for improved k.
15. Steps in fabrication process. Dual damascene process.
16. Understanding what design rules are.

Midterm exam III

17. Packaging, MCMs, and board-level design. Implications of packaging and interconnect for performance.
18. Gate leakage. High-κ dielectric. See assigned article.
19. Transient diode and MOSFET behavior. Computing capacitances based on MOSFET structure and operating region.
20. Derivation from inverter transfer curve from MOSFET I–V curves. Impact of inverter asymmetry on V_M.
21. Noise margin definitions and purpose. Gain definition.

Upcoming topics

- Inverter chains for driving large loads.
- Complex behavior in logic gate.

Homework assignment

- 3 October: Read sections 5.3, 5.4.1, and 5.4.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 3 October: Lab 2.
- 10 October: Homework 2 (which will help in your preparation for the midterm exam).
- 10 October: Read sections 5.4, 5.5, 5.6, and 3.5 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.