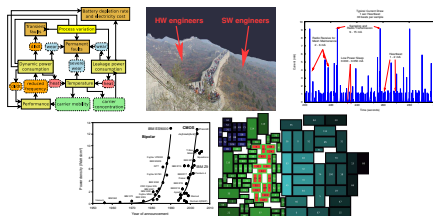


Digital Integrated Circuits – EECS 312

<http://robertdick.org/eecs312/>

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Review

- Design a non-trivial logic gate.
- What happens to inverter delay as the driving MOSFET widths are increased?
- What happens to inverter delay as the driven MOSFET widths are increased?
- What impact does non-instantaneous rise/fall time have on the propagation delay for the subsequent logic stage?

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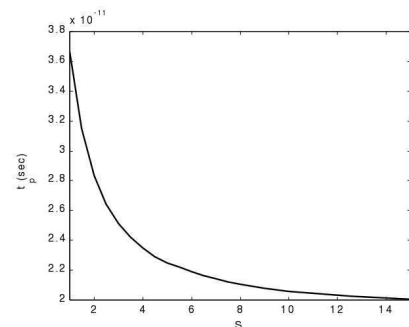
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Lab 3

- Input inverters.
- Implications of sizing on energy consumption.

Derive and explain.

Dependence of delay on width (R)



- Fix $R_L C_L$ and vary W .
- Eventually, self-loading dominates.

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Inverter chain delay optimization

Given

- Size (width) of first inverter in chain,
- Driven load,
- Transistors are minimal length, and
- $W_p/W_n = 2$ approximately balances t_{pHL} and t_{pLH} .

Find

- Optimal number of inverters in chain and
 - Optimal size (width) of each inverter
- to minimize chain delay.

Intuition

- Given two inverters (first fixed) and a large load (C_L), how should the second be sized to minimize delay?
- $C_{G2} = C_{G1}$ (minimal)?
- $C_{G2} > C_L$?
- $C_{G2} = C_L$?
- Some other setting?
- Why?

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Derivation I

$$\begin{aligned} \text{Let } W &= W_n = W_p/2 \\ R &= R_p = R_n \\ T_{pHL} &= T_{pLH} = 0.69RC_L \\ C_i &= 3 \frac{W_{i+1}}{W_{unit}} C_{unit} \\ t_p &= 0.69R(C_{int} + C_L) \end{aligned}$$

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Derivation II

Consider the impact of scaling factor S .

$$\begin{aligned} t_p &= 0.69 \left(\frac{R}{S} SC_{int} \left(1 + \frac{C_L}{SC_{int}} \right) \right) \\ t_p &= 0.69RC_{int} \left(1 + \frac{C_L}{SC_{int}} \right) \\ t_p &= t_{p0} \left(1 + \frac{C_L}{SC_{int}} \right) \end{aligned}$$

t_{p0} : Intrinsic delay.

- Scaling doesn't impact intrinsic delay.
- Scaling does impact total delay.
- $t_p \rightarrow t_{p0}$ as $S \rightarrow \infty$.
- Diminishing returns with increasing S .

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Consider chain of inverters I

$$\begin{aligned} t_{p,chain} &= t_{p1} + t_{p2} + \dots + t_{pn} \\ t_{pi} &\approx t_{p0} \left(1 + \frac{C_{g,i+1}}{\gamma C_{g,i}} \right) \\ t_{p,chain} &= \sum_{i=1}^N t_{pi} \\ t_{p,chain} &= t_{p0} \sum_{i=1}^N \left(1 + \frac{C_{g,i+1}}{\gamma C_{g,i}} \right) \end{aligned}$$

Given that

$$C_{g,N+1} = C_L$$

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Consider chain of inverters II

and

$$\gamma = \frac{C_{int}}{C_g} \approx 1 \text{ (technology-dependent constant).}$$

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Sketch of derivation

- For each i , find $\sigma^{t_{p,chain}/\sigma C_{g,i}}$.
- Solve for $\sigma^{t_{p,chain}/\sigma C_{g,i}} = 0, \forall i=1..N$.
- Result is $\frac{C_{g,i+1}}{C_{g,i}} = \frac{C_{g,i}}{C_{g,i-1}}$.
- Each stage size geometric mean of previous and next:
 $C_{g,i} = \sqrt{C_{g,i-1}C_{g,i+1}}$.
- Constant factor relates sizing of all adjacent gate pairs.
- Each stage has same delay.

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Sizing for optimal inverter chain delay

- Optimal stage-wise sizing factor: $\sqrt[N]{\frac{C_L}{C_{g,1}}}$.
- Minimum path delay: $t_{p,chain} = Nt_{p0} \left(1 + \sqrt[N]{\frac{C_L}{C_{g,1}}}/\gamma \right)$

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Example of inverter sizing

Given

- $C_L = 16C_1$.
- $N = 4$.

Per-stage scaling factor: $\sqrt[4]{16C_1/C_1} = 2$

Optimizing N I

Let

$$\phi = \frac{C_L}{C_{g,1}}$$

$$t_{p,chain} = Nt_{p0} \left(1 + \frac{\sqrt[N]{\Phi}}{\gamma} \right)$$

$$t_{p,chain} \frac{d}{dN} = \gamma + \sqrt[N]{\Phi} - \frac{\sqrt[N]{\Phi} \ln(\Phi)}{N}$$

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Optimizing N II

Set this to zero.

$$\text{Let } \phi = \sqrt[N]{\Phi}$$

$$0 = \gamma + \phi - \frac{\phi \ln(\phi^N)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \frac{\ln(\phi^N)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \frac{N \ln(\phi)}{N}$$

$$0 = \frac{\gamma}{\phi} + 1 - \ln(\phi)$$

$$\ln(\phi) = \frac{\gamma}{\phi} + 1$$

Optimizing N III

$$\phi = e^{\gamma/\phi+1}$$

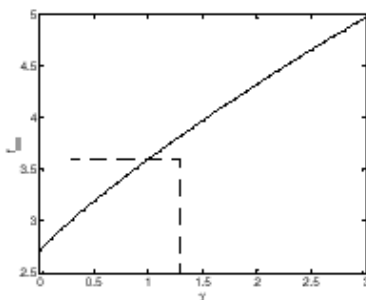
Hard to deal with this for $\gamma \neq 0$. Consider implications for $\gamma = 0$.

$$\phi = e$$

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Optimal stage sizing factor



- Optimal tapering factor for $\gamma = 0$: $e \approx 2.7$.
- 3.6 for $\gamma = 1$.


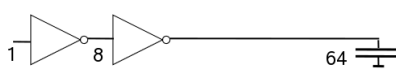
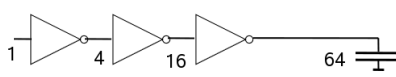
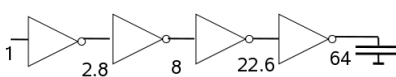
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$t_{p,chain}(\Phi)$

Φ	Unbuffered	$N = 2$	Optimal N
10	11	8.3	8.3
100	101	22	16.5
1,000	1,001	65	24.8
10,000	10,001	202	33.1

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Buffering example

	N	f	t _p
	1	64	65
	2	8	18
	3	4	15
	4	2.8	15.3

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Upcoming topics

- Interconnect.
- Alternative logic design styles.

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Review

- How can the optimal number of inverters in a load-driving chain be determined?
- How can the optimal size of each inverter in the chain be decided?
- How do determine optimal sizes of logic gates in arbitrary structures?
 - May cover this near end of course.
- Do example problem.

Derive and explain.

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Power consumption in synchronous CMOS

$$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$$

$$P_{SWITCH} = C \cdot V_{DD}^2 \cdot f \cdot A$$

$$\dagger P_{SHORT} = \frac{b}{12} (V_{DD} - 2 \cdot V_T)^3 \cdot f \cdot A \cdot t$$

$$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$$

C : total switched capacitance V_{DD} : high voltage
f : switching frequency A : switching activity
b : MOS transistor gain V_T : threshold voltage
t : rise/fall time of inputs

$$\dagger P_{SHORT} \text{ usually } \leq 10\% \text{ of } P_{SWITCH}$$

Smaller as V_{DD} → V_T
A < 0.5 for combinational nodes, 1 for clocked nodes.

Reasons for power consumption

- Dynamic
 - Charging and discharging RC loads.
 - $E_{dyn} = C_L V_{DD}^2$.
 - $P_{dyn} = C_L V_{DD}^2 f$.
 - But $f \propto V_{DD}$.
 - So $P_{dyn} = C_L V_{DD}^3$.
- Static
 - Sub-threshold leakage.
 - Gate leakage.
- Short-circuit: Pull-up and pull-down networks briefly both on.

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Fixed voltage charging

$$E_R^{step} = \int_{t=0}^{\infty} V_R(t) I_R(t) dt$$

$$E_R^{step} = \int_{t=0}^{\infty} V_R(t) \frac{V_R(t)}{R} dt$$

$$E_R^{step} = \int_{t=0}^{\infty} V_{DD} e^{-t/RC} \frac{V_{DD} e^{-t/RC}}{R} dt$$

$$E_R^{step} = \frac{V_{DD}^2}{R} \int_{t=0}^{\infty} e^{-2t/RC} dt$$

$$E_R^{step} = \frac{V_{DD}^2}{R} \left(-\frac{RC}{2} \right) \left(e^{-2t/RC} \right)_{t=0}^{\infty}$$

$$E_R^{step} = \frac{-V_{DD}^2 C}{2} (0 - 1)$$

$$E_R^{step} = \frac{V_{DD}^2 C}{2}$$

Fixed current charging I

$$E_R^{ramp} = \int_{t=0}^{\infty} V_R(t) I_R(t) dt$$

Let T be the voltage ramp duration, I_R is fixed. V_R is fixed.

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Fixed current charging III

$$E_R^{ramp} = \frac{V_{DD}^2 C^2 R}{T^2} T$$

$$E_R^{ramp} = \frac{V_{DD}^2 C^2 R}{T}$$

$$E_R^{ramp} = \frac{V_{DD}^2 C 2RC}{2 T}$$

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Charging methods summary

- $I(t)$ influences energy consumption for same change in V .
- In theory, keeping voltage differences very small can permit extremely low-power operation.
- Leakage, current control, and preserving reversibility make this challenging.

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Fixed current charging II

$$\Delta V = \frac{\Delta q}{C}$$

$$V_{DD} = \frac{I_R T}{C}$$

$$I_R = \frac{C V_{DD}}{T}$$

$$V_R = R I_R$$

$$E_R^{ramp} = \int_{t=0}^T I_R(t) V_R(t) dt$$

$$E_R^{ramp} = \int_{t=0}^T \frac{C V_{DD}}{T} \frac{R C V_{DD}}{T} dt$$

$$E_R^{ramp} = \frac{R V_{DD}^2 C^2}{T^2} \int_{t=0}^T 1 dt$$

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Break-even point

$$E_R^{step} = E_R^{ramp}$$

$$\frac{V_{DD}^2 C}{2} = \frac{V_{DD}^2 C 2RC}{2 T}$$

$$1 = \frac{2RC}{T}$$

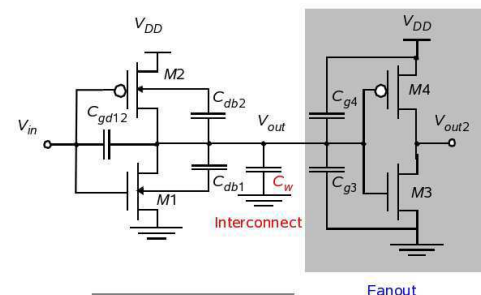
$$T = 2RC$$

- Properly controlling $V_R(t)$.
- Performance.
- In limit, permits reversible computation with low/no power consumption during charging and discharging.

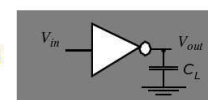
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Charging methods summary

Capacitive load modeling



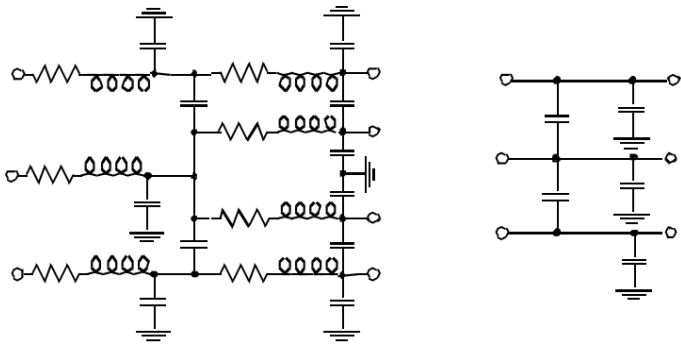
Simplified Model



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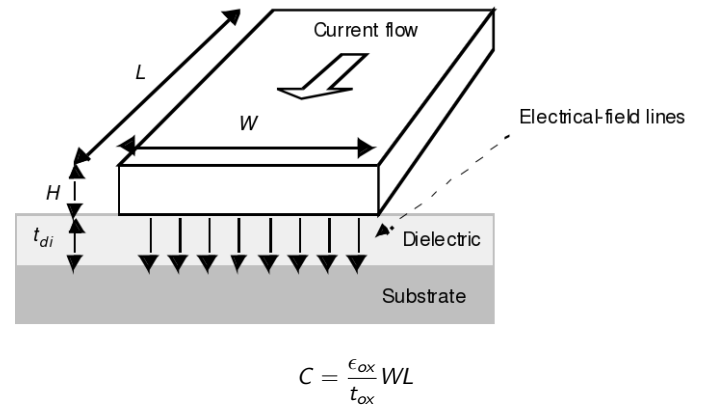
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Interconnect modeling



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Interconnect capacitance



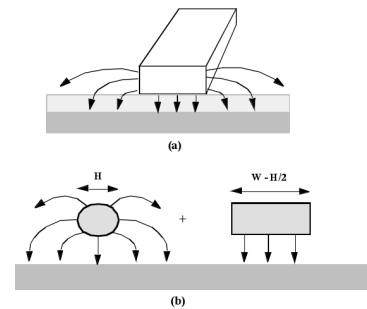
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Permittivity (k)

Material	ϵ
Vacuum	1
Aerogels	~ 1.5
Polyimides	3-4
SiO ₂	3.9
Glass-epoxy	5
Si ₃ N ₄	7.5
Alumina	9.5
Silicon	11.7

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Fringing



$$C_{wire} = C_{pp} + C_{fringe} = W \frac{\epsilon_{ox}}{t_{ox}} + \frac{2\pi\epsilon_{ox}}{\log(t_{ox}/H)}$$

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Trends in interconnect design

- More metal layers.
- Lower aspect ratios.
 - More coupling.
- Smaller transistors, but similar-length global interconnect.

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Upcoming topics

- Alternative logic design styles.
- Latches and flip-flops.
- Memories.

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Homework assignment

- 10 October: Homework 2.
- 10 October: Read sections 5.4, 5.5, 5.6, and 3.5 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 17 October: Read sections 6.2.1, 4.1, and 4.3.2 in J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.
- 22 October: Lab 3.