Fundamental Limitations to CMOS Scaling

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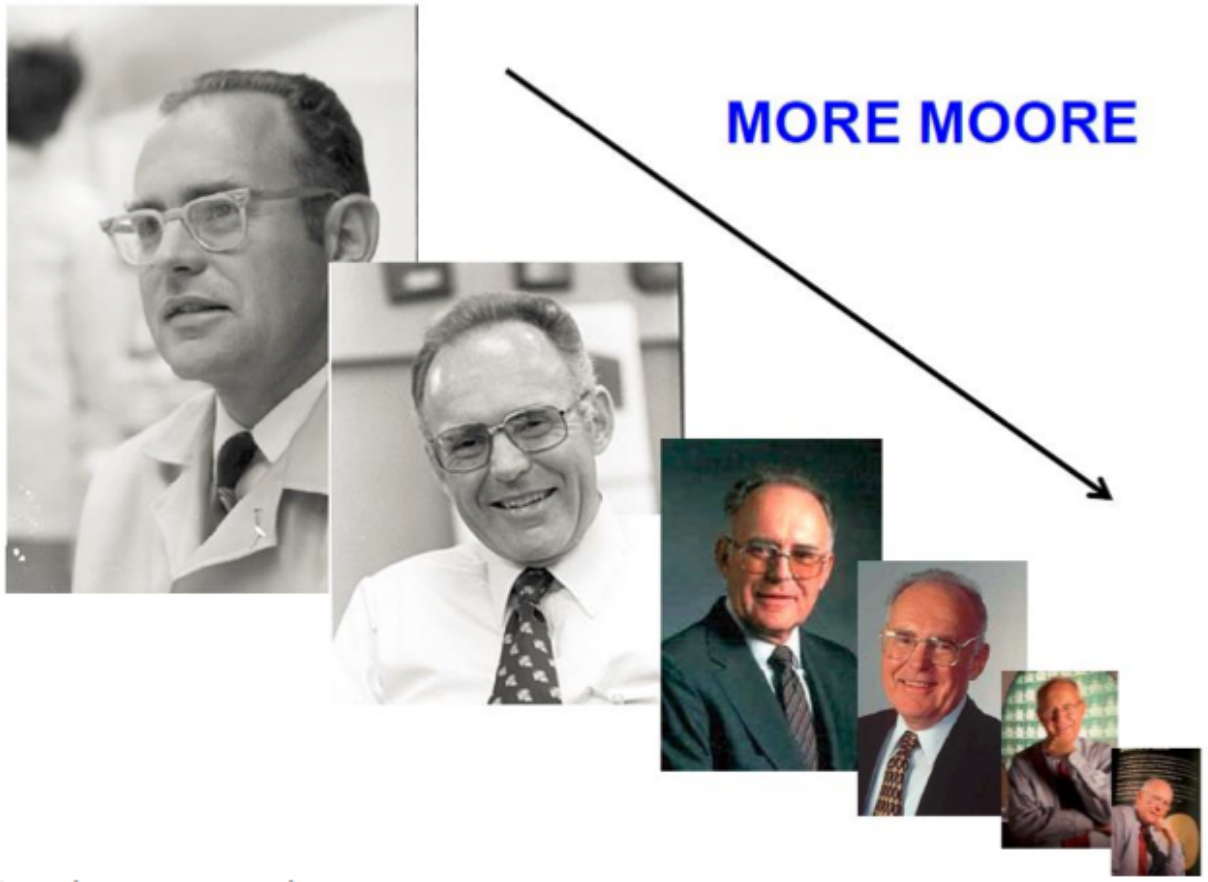
Outline

- Motivation for scaling
- Fabrication difficulties
- High leakage current
- Possible solutions

Motivation for Scaling

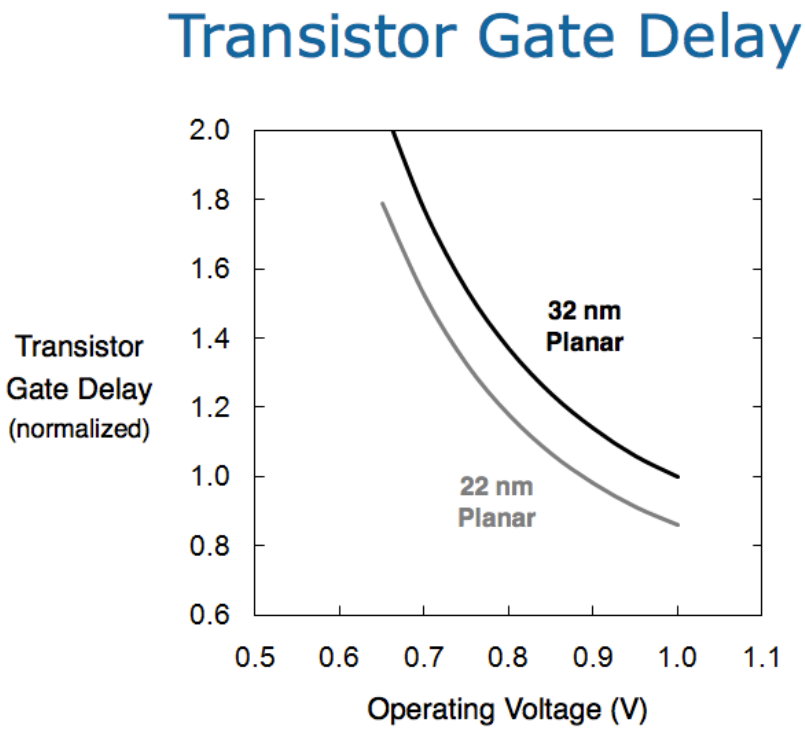
- Scaling = Improving performance

Moore's Law



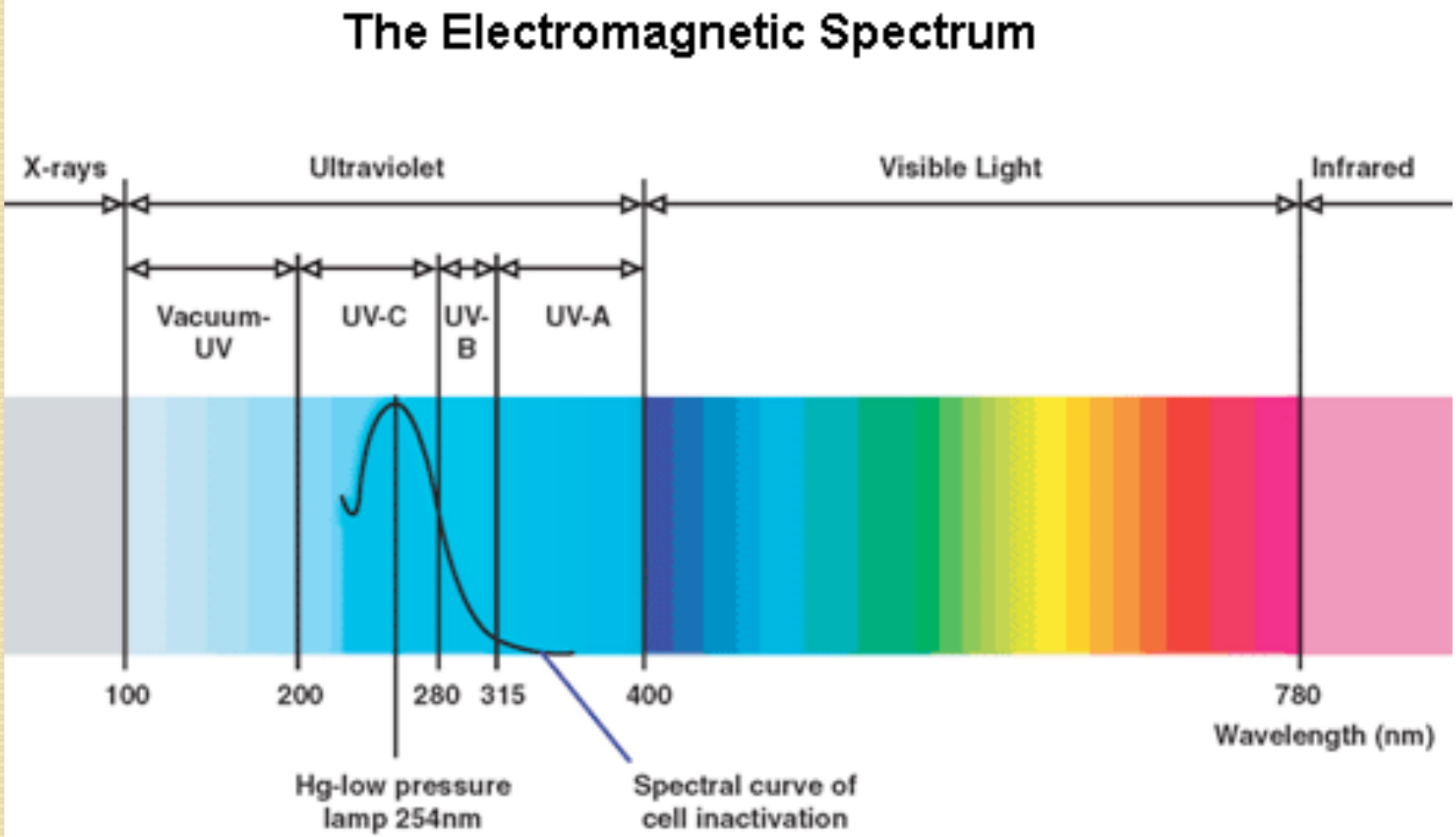
Motivation for Scaling

- More transistors --> Higher performance
- Less delay time --> Higher frequency
- Less V_{DD} --> Lower power consumption



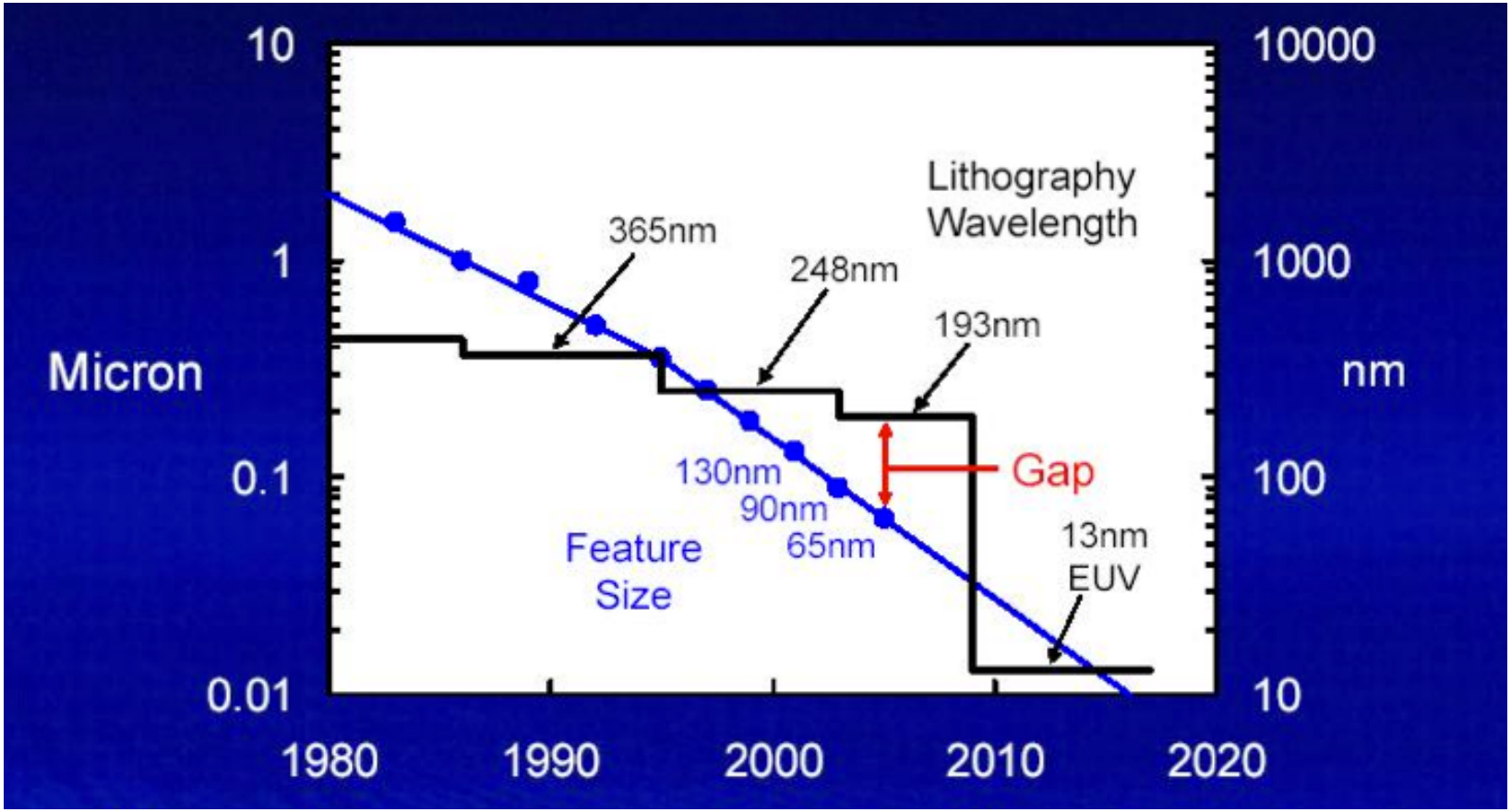
Fabrication Difficulties

- Problems in lithography



Fabrication Difficulties

- State-of-the-art lithography: 193nm UV
- Next Generation: 13.5nm EUV

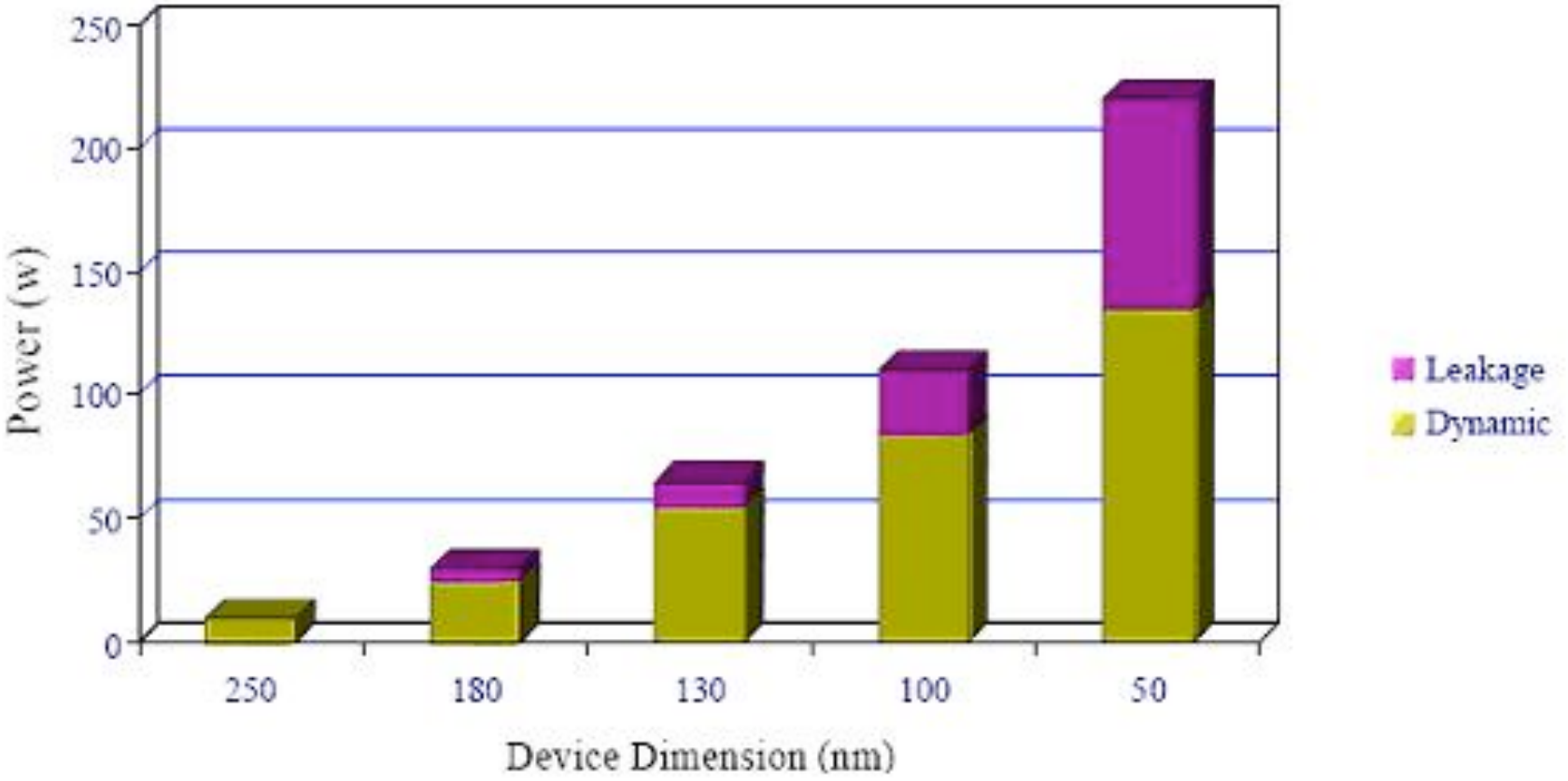


Fabrication Difficulties

- Problems of 13.5nm EUV: **Cost!**
  - Need to change the entire lithography equipment
  - Still take some time to reach 14-nm technology or lower.
  - As a result: Cost overwhelms benefits.

High Leakage Current

- $P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$



High Leakage Current

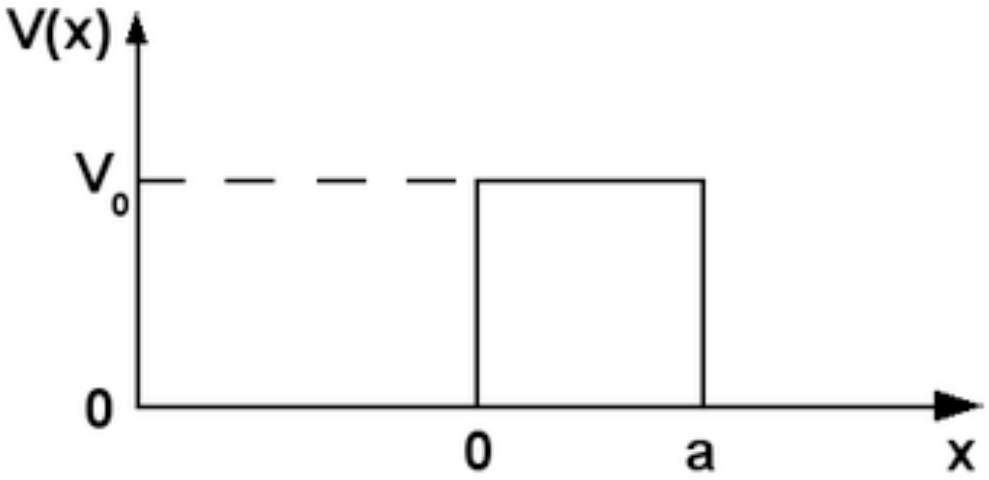
- Five major sources of leakage current:
  - **Gate oxide tunneling leakage**
  - **Subthreshold leakage**
  - Reverse-bias junction leakage
  - Gate induced drain leakage
  - Gate current due to hot-carrier injection

Gate Oxide Tunneling Leakage

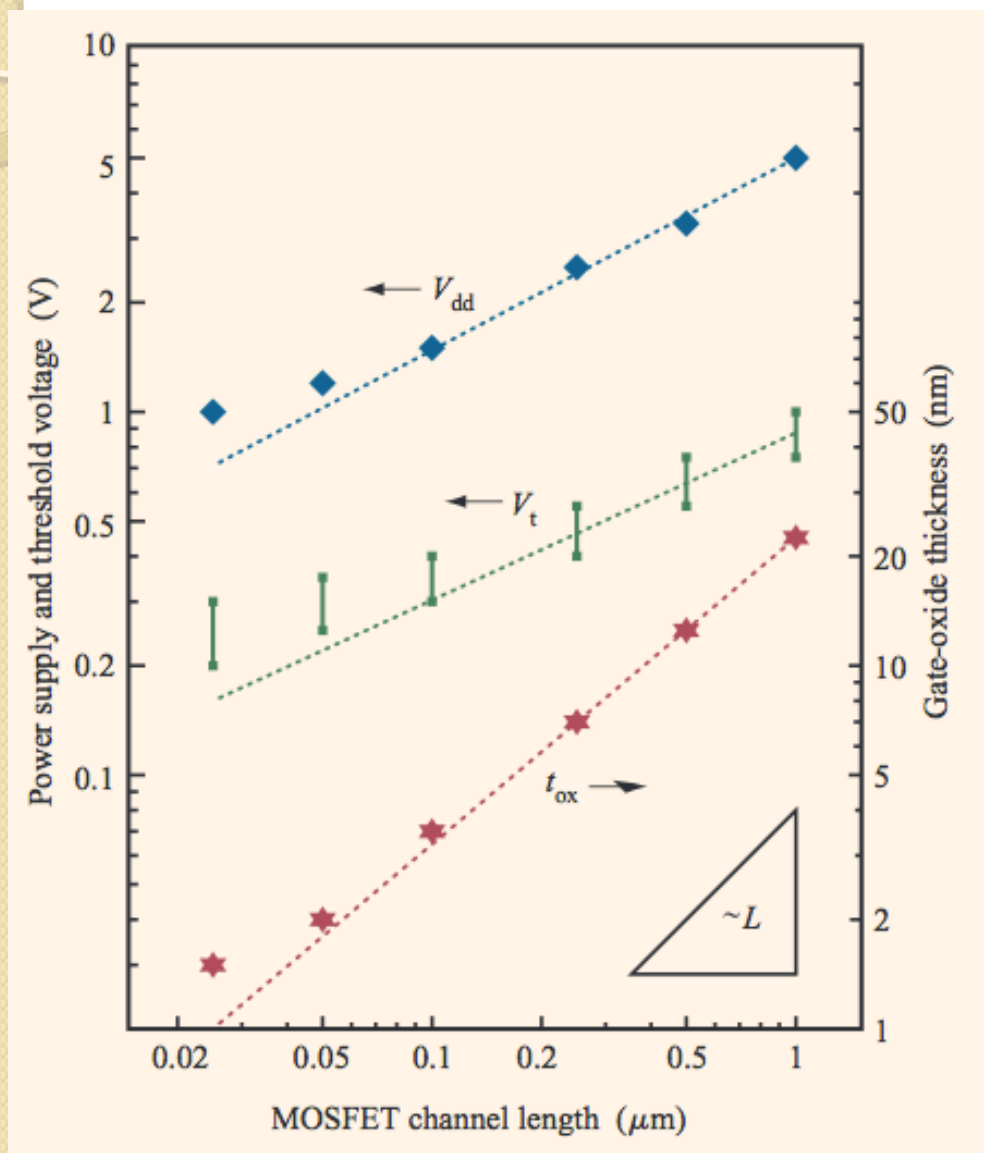
- Quantum tunneling

  --Phenomenon where a particle tunnels through a barrier that it classically could not surmount

- More significant as t_{ox} goes down



Gate Oxide Tunneling Leakage



Scaling

Thinner gate oxide

High gate oxide tunneling leakage

Subthreshold Leakage

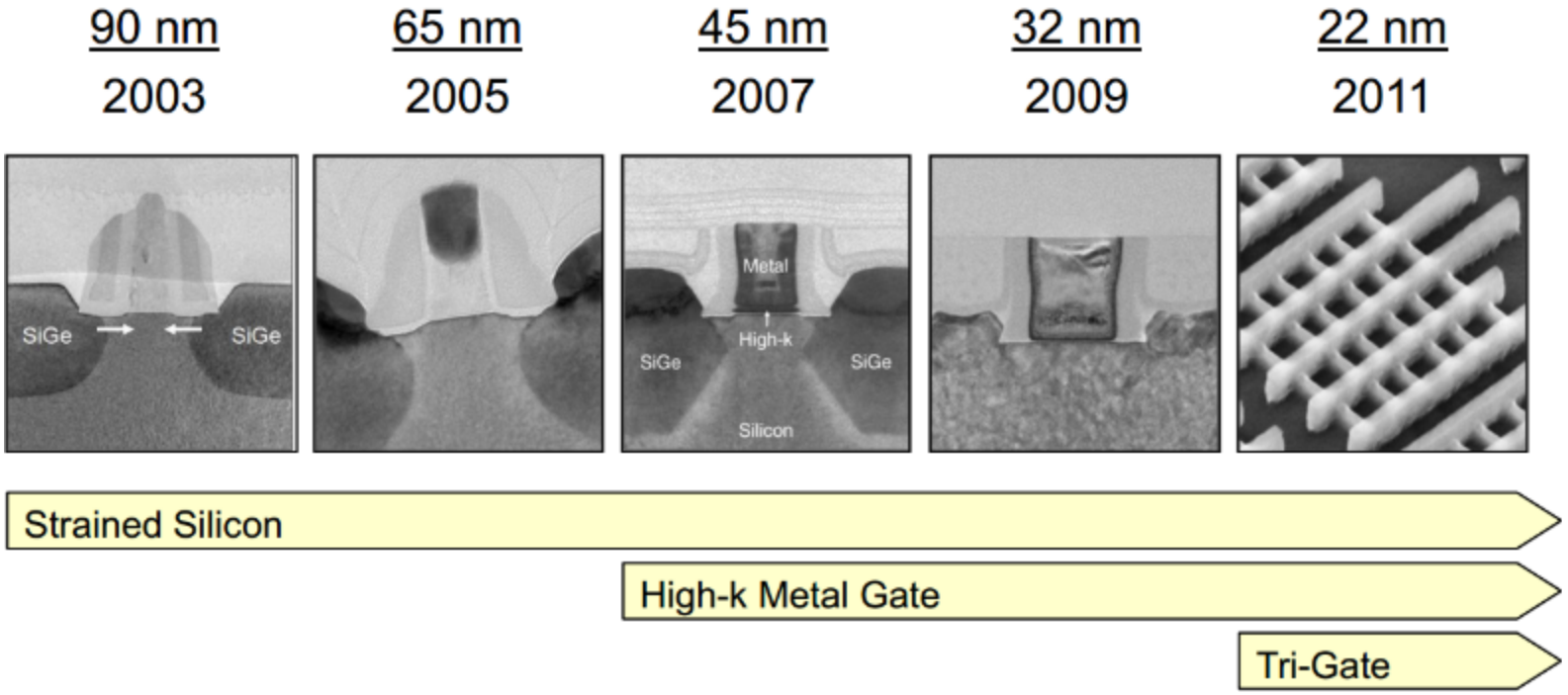
- Current is not 0 when the transistor is off
- From lecture slides 5, we have equation

$$S=n(kT/q)\ln(10)$$

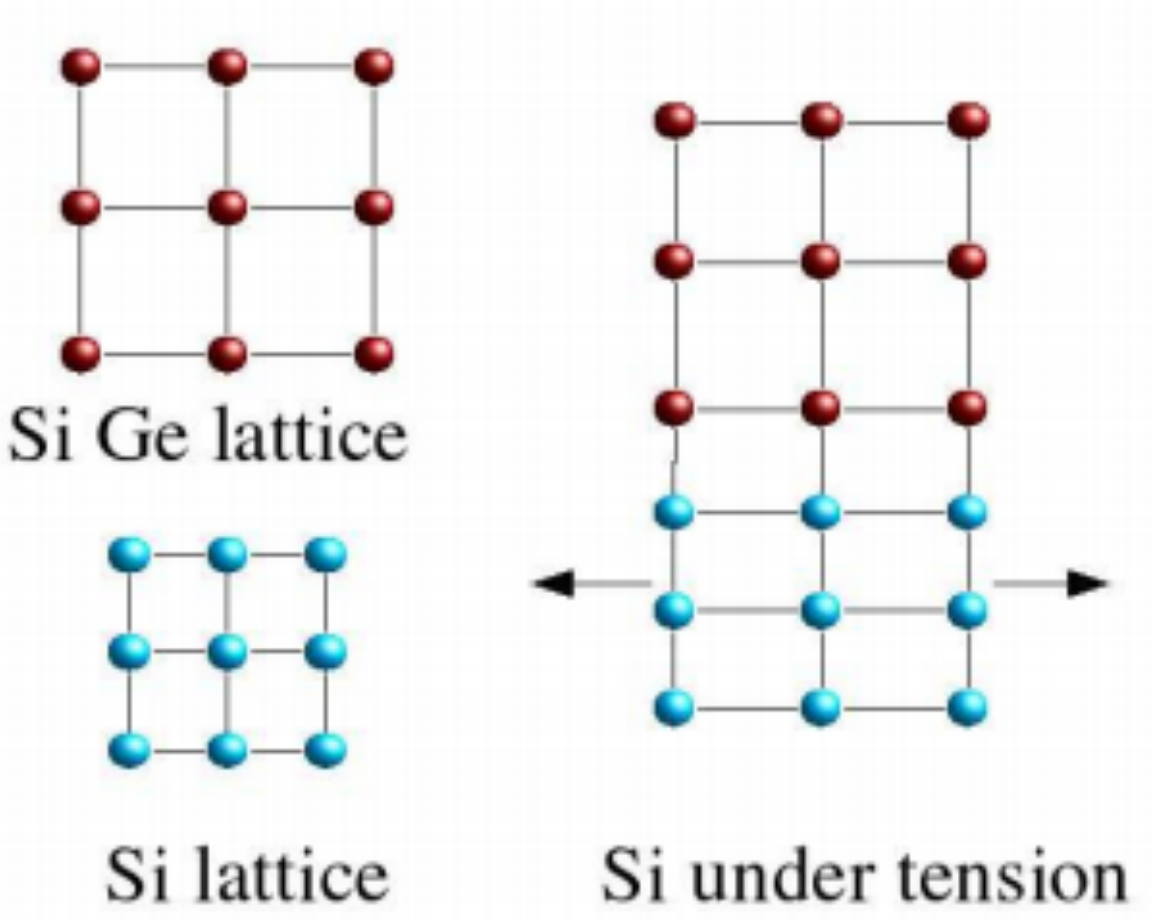
S: Change in V_{GS} for I_D to change 10x

- Scaling -> Smaller threshold voltage -> Nearer to the V_{GS} = 0 -> Higher subthreshold leakage

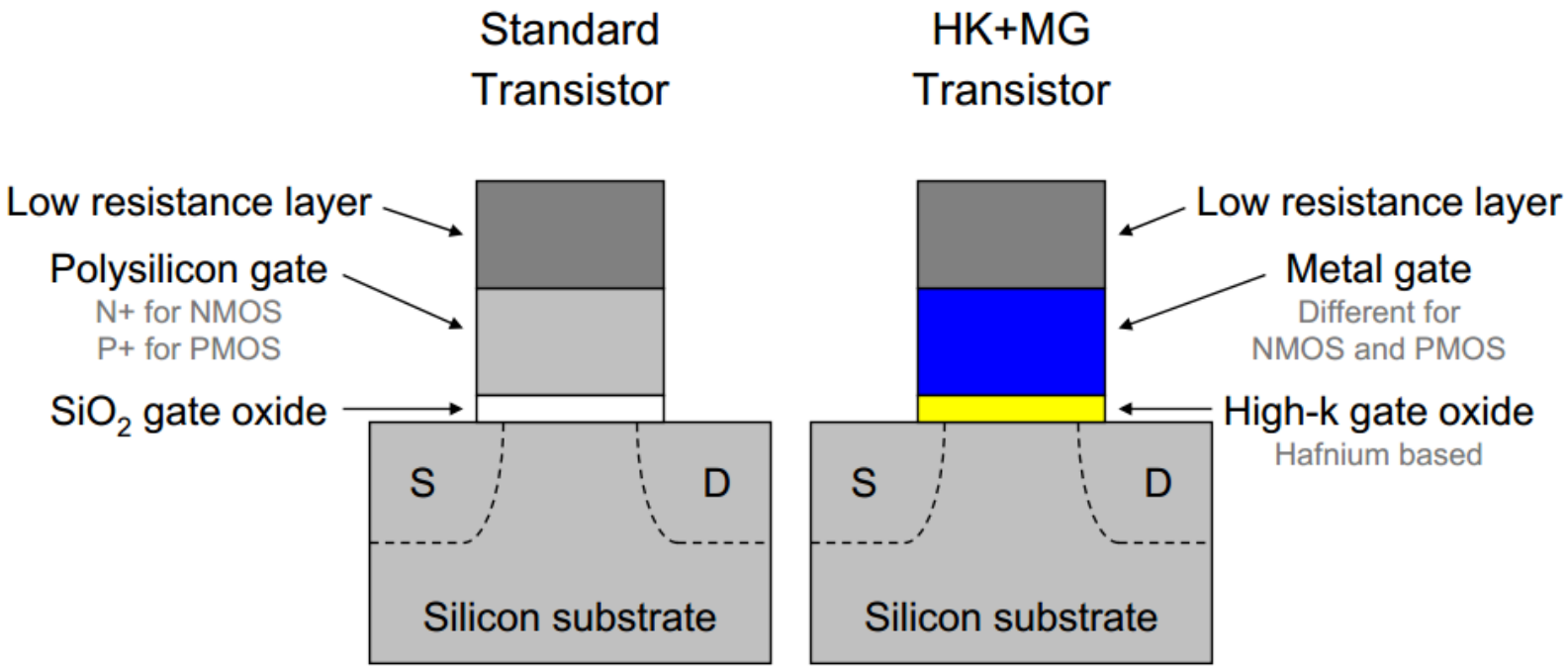
Possible solutions



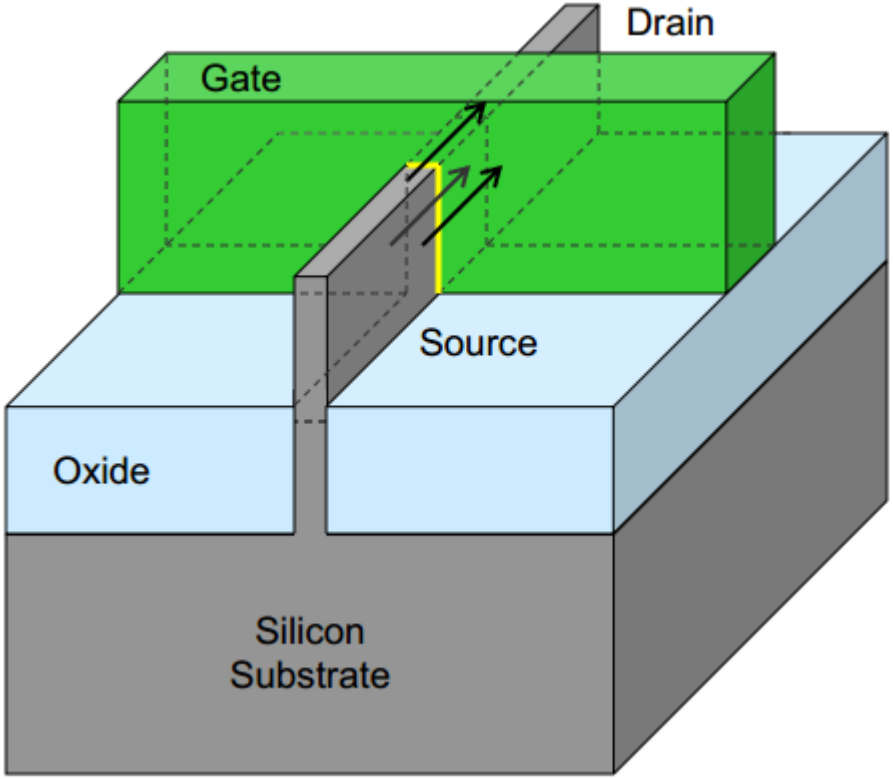
Strained Silicon



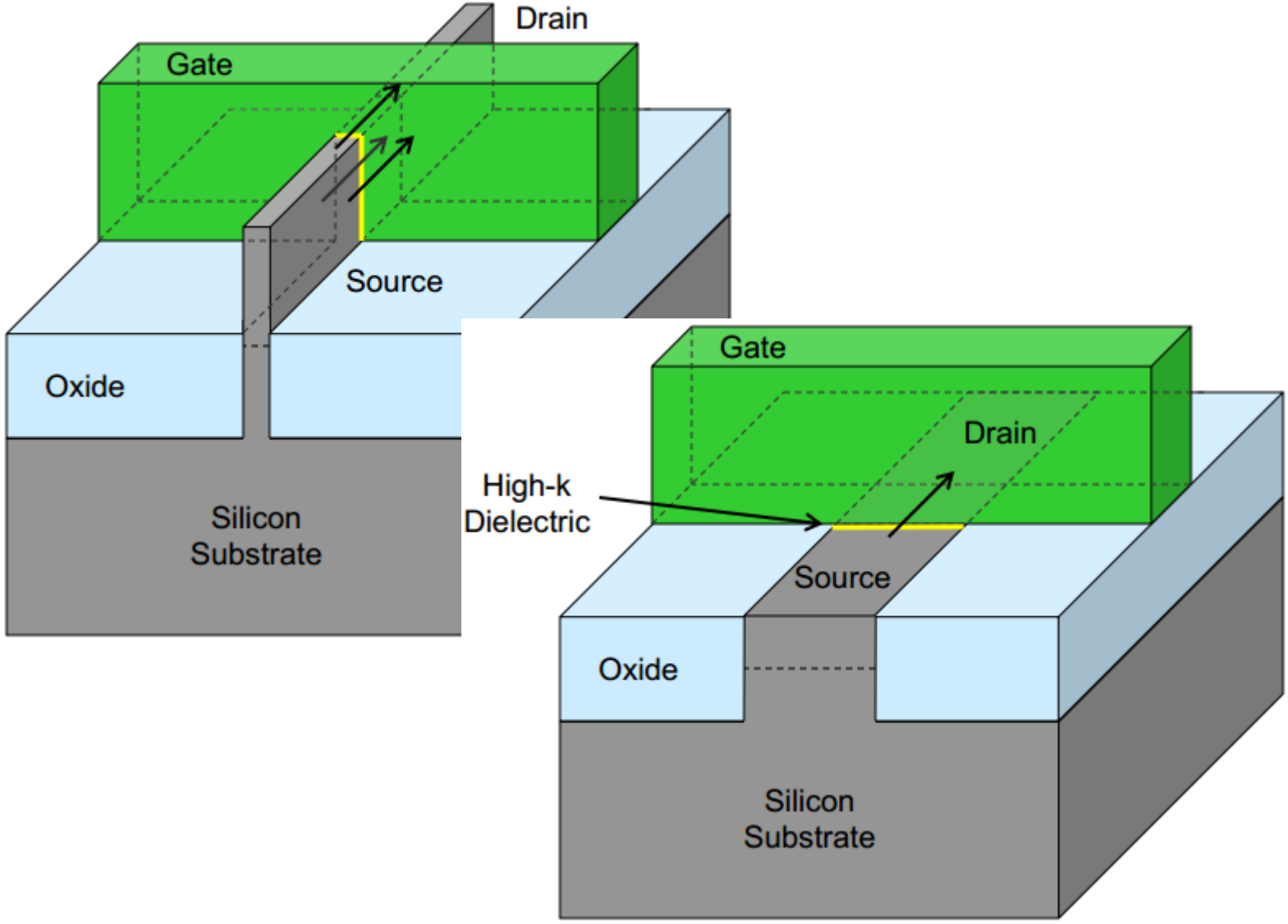
High-k Metal Gate



Tri-Gate



Tri-Gate


Drain
Gate
Source
Oxide
Silicon
Substrate
Gate
Drain
High-k
Dielectric
Source
Oxide
Silicon
Substrate

Reference:

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