EECS 312: Digital Integrated Circuits
http://ziyang.eecs.umich.edu/~dickrp/eecs312/

Robert Dick

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Instructor	Robert Dick http://robertdick.org/ dickrp@umich.edu
Lecture	1010 DOW Tuesdays and Thursdays, 14:30–16:00
Office hours:	2417-E EECS Tuesdays and Thursdays, 16:00–17:00 (plan to extend when demand is high)
Teaching assistant	Shengshuo Lu Email: luss@umich.edu
Discussion	1303 EECS Fridays, 12:30–13:30
Office Hours	2725 BBB Mondays, 10:30–12:30 Thursdays, 17:30–19:30
Midterm exam	19:00–20:30 8 October in 1670 BBB
Final exam	13:30–15:30 20 December

1 References

Textbook

J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.

Supplementary Texts

- Ben G. Streetman. *Solid State Electronic Devices*. Prentice-Hall, NJ, fifth edition, 2005.
- Andrei Vladimirescu. *The SPICE Book*. John Wiley & Sons, second edition, 1994.
- Adel S. Sedra and Kenneth C. Smith. *Spice for Microelectronic Circuits*. Harcourt School, third edition, 1991.
- Ivan Sutherland, Robert F. Sproull, and David Harris. *Logical Effort: Designing Fast CMOS Circuits*. Morgan Kaufmann, first edition, 1999.

2 Purpose of Course and Course Objectives

Digital Integrated Circuits is a junior-level digital circuits course designed for electrical and computer engineering majors. Serious students in other majors are welcome. Building upon pre-existing knowledge of MOSFET device operation, students will learn to analyze and design combinational and sequential digital circuits in various logic families, with an emphasis on CMOS. Tradeoffs among logic families will be explained (e.g., noise immunity vs. speed and density vs. static power), allowing students to make informed decisions on when to use each style. Students will be introduced to SPICE simulation and will use SPICE in designing various blocks of logic in lab assignments as well as a design project. Common memory structures (ROM, SRAM, and DRAM) will be described. This class will prepare students for EECS 427. EECS 312 has the following objectives.

1. Teach students the analysis and design of static CMOS digital circuits.
2. Develop a thorough understanding of the static and dynamic characteristics (delay, power, noise immunity, and density) of various MOS based logic families (CMOS, pseudo-NMOS, pass transistor, and domino).
3. Introduce and familiarize students with circuit simulation tools (SPICE) that will be valuable to them in later courses (e.g., EECS 427) and industry as circuit designers.
4. Provide students the chance to work on small design projects where they attempt to minimize certain objective functions while meeting other design constraints for a functional unit. Collaborative discussion during the design process will be encouraged.
5. Teach the operation and importance of memory structures (ROM, SRAM, and DRAM) in large digital systems.
6. Provide students with the required knowledge to make informed decisions on when to use different logic styles and the tradeoffs inherent in those decisions.
7. Teach students to analyze the effect of interconnect parasitics on circuit performance.
8. Introduce students to important future trends in large-scale digital circuit design, including manufacturability issues and barriers to device scaling.

3 Grading Philosophy

There is not a fixed number of As, Bs, etc. for the class. If the class performs well, there will be more As than average. The converse is also true. Therefore, when you help classmates, you needn't be concerned that you are undermining your own course grade.

4 The Line Between Collaboration and Copying

Students are encouraged to discuss problems and design ideas with others. However, students are individually responsible for preparing, evaluating, and reporting on their designs. You are encouraged to share ideas and discuss assignments, but are not permitted to copy the schematics, simulation results, or reports of other students. If you feel that you must do this, report it openly so credit can be appropriately adjusted (reduced). Continued participation in the course implies that you understand that discussion is fine but that claiming credit for copied work is cheating.

5 Homework Assignments and Projects

Homework assignments are due at the beginning of lecture. There will be a 5% penalty for assignments that are less than a day late and a 10% penalty per day for late assignments. After two days, no credit will be given; this allows us to hand out solutions soon after assignments are handed in. Note that the penalty for late assignments is gradual. If you neglect to leave some slack and something unexpected comes up, you have the option of handing in the assignment a day late instead of staying up all night.

There will be a four laboratory assignments and a final project. Laboratory assignments are subject to a 10% per day late penalty. There will be little if any slack in the final project due date so that deadline is hard, but you will have four weeks for the project.

Our grader will provide very limited feedback on assignments. The GSI and I will provide more detailed feedback in discussions and lectures. We will also provide solutions and be available for help with assignments and projects during office hours.

6 Topics

We will endeavor to cover the following topics. References to relevant book chapters or supplements will be provided for each topic.

- Course overview and administrative details
- Context for digital integrated circuit design
- Scaling and process variation
- Transistor static behavior
- Transistor dynamic behavior
- Fabrication
- SPICE models
- CMOS inverters
- Inverter dynamic behavior
- Inverter power consumption
- CMOS gates
- Pass transistor logic
- Transmission gates
- Transistor and logic gate sizing
- Dynamic logic
- Domino logic
- np-CMOS
- Interconnect behavior
- Interconnect design
- Latches

- Flip-flops
- Other sequential elements
- ROM
- SRAM
- DRAM
- Future technology and architecture trends

7 Special Topics

Groups of 2–3 students will give brief (5–10 minute) presentations on course-related special topics of special interest to them, with one such presentation per lecture.

8 Grade Weightings

Midterm exam:	15%
Final exam:	30%
Laboratory assignments:	20%
Final project:	20%
Homework:	10%
Presentation on special topic:	5%