Study Helper for EECS 312

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1. Uses of digital systems.
2. History of digital computing devices. Impact of technology improvements on performance, power consumption, size, and reliability. Bipolar to CMOS move.
3. Power consumption equation and components of total power consumption.
4. Requirements for devices to permit use in digital system. Regeneration/restoration.
5. MOSFET structure and layout.
6. Schematic capture, e.g., using Cadence software.
7. Resistance basics, and their application to MOSFET channels and metal wires.
8. Logic gate and transmission gate structures.
9. Ratioed vs. ratioless logic.
10. NMOS, PMOS, and CMOS inverters.
11. Doping. Intrinsic vs. extrinsic semiconductors. N-type vs. P-type semiconductors. Stationary ions and mobile charge carriers.
12. Diode structure and operation. Drift and diffusion.
13. MOSFET operation. Operating regions and reasons for their existence. Change in conditions (especially I_D) with changing V_{GS}, V_{DS}, and V_{SB}. MOSFET models. Cutoff, pinch-off, and velocity saturation. Long-channel vs. short-channel MOSFETs.
14. Impact of threshold voltages upon appropriate uses of NMOSFETs and PMOSFETs, e.g., why not use NMOSFETs for pull-up networks?
15. Body effect.
16. Subthreshold leakage and subthreshold operation.
17. Process variation definition and influence on circuit behavior.
18. High-level understanding of FinFET structure and reason for improved k.
19. Steps in fabrication process. Dual damascene process. CMP.
20. Ability to read layouts.
21. Understanding what design rules are.

22. Packaging, MCMs, and board-level design. Implications of packaging and interconnect for performance. Low-k dielectric.

23. Gate leakage. High-k dielectric. See assigned article.

24. Transient diode and MOSFET behavior. Computing capacitances based on MOSFET structure and operating region.

25. Derivation from inverter transfer curve from MOSFET I–V curves. Impact of inverter asymmetry on V_M.

26. Noise margin definitions and purpose. Gain definition.

27. Ability to solve RC delay, power, and energy problems.

28. Inverter chain sizing for driving large loads.

29. Types of power consumption, dependence on V, f, and C.

30. Energy consumption implications of fixed-voltage and fixed-current charging.

31. Appropriate interconnect models for different types of interconnect.

32. Reasons for interconnect parasitic capacitances.

33. Trends in integrated circuit interconnect structure.

34. Rent's rule. Know what it is.

35. Sheet resistance concept.

36. Impact of material resistivities. Al and Cu in particular.

37. Silicides. Know what they are and why they are used.

38. Elmore delay modeling. Understand it and be able to use it proficiently.

39. Know what happens to the shape of a voltage step function as it propagates along a wire, i.e., a distributed RC network.

40. Transistor sizing. Know how to balance worst-case pull-up and pull-down resistances for complex logic gates. Don't forget impact of mobility.

41. TG-based design and pass transistor based design using 2^{n-1} MUX as a starting point.

42. Miller effect. What is it? How can it be modeled?

43. Stack effect. What is it? What impact does it have on leakage current?

44. Hazards. What are they? What problems can they cause? What is their fundamental cause? How can they be eliminated?

45. DCVSL design.

46. Dynamic logic design.

47. Charge sharing. How to calculate its impact? How to compensate for it?

48. Leakage in dynamic logic. Use of keepers.

49. Role of combinational and sequential logic.

50. Latches and flip-flops. Meaning of symbols and behavior. Setup and hold time. Level-sensitive vs. edge-triggered. Static vs. dynamic.

51. Analysis of simple circuits with feedback, for which the RS latch provided an example.

52. Bistability.

53. Schmitt triggers.

54. Knowledge of different types of ROM at the schematic/functionality level. SRAM and DRAM cell design. Memory organization. Roles played by sense amplifiers and detailed understanding of latch-based sense amplifier.

55. Logical effort.

Please also review the lecture notes and assigned reading. You will find the assigned reading at the end of nearly every lecture will help understand the material in the following lecture. Please also review your work on the lab and homework assignments.