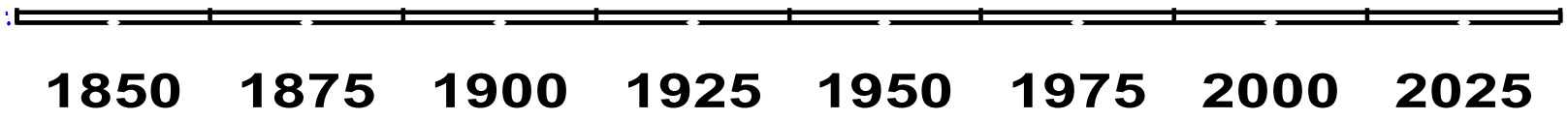
Novel device technologies

- Slides largely based on presentation Li Shang and I gave at Tsinghua University
- Some of the images might be copyrighted by others: don't charge or distribute

Overview

- Historic overview of technology scaling
- CMOS: current status and challenges
- Nanotechnologies: An introduction
- Nano circuit and architecture design
  - Carbon nanotube technology
  - Single electron tunneling transistor
- Open questions

Evolution of electronics



Mechanical

Electro-Mechanical

Electronic-VT

Bipolar

NMOS

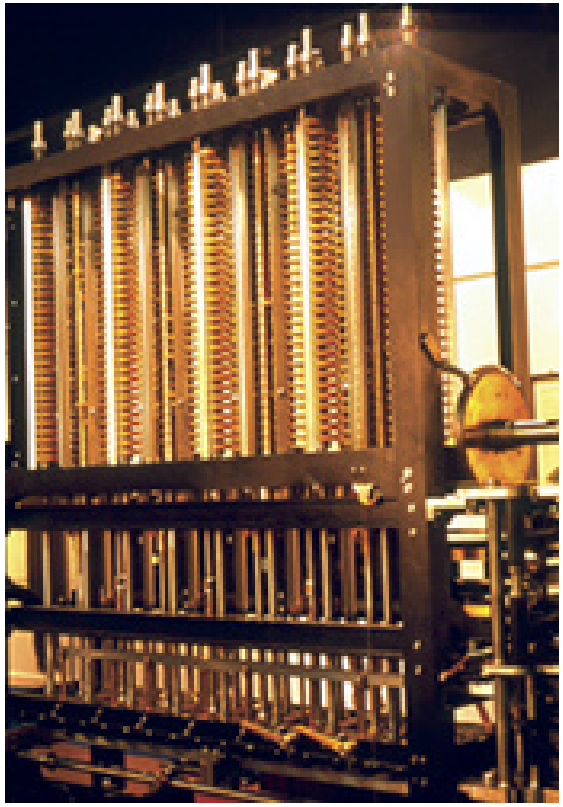
CMOS…….焙？

The first computer

Babbage difference Engine (1822)

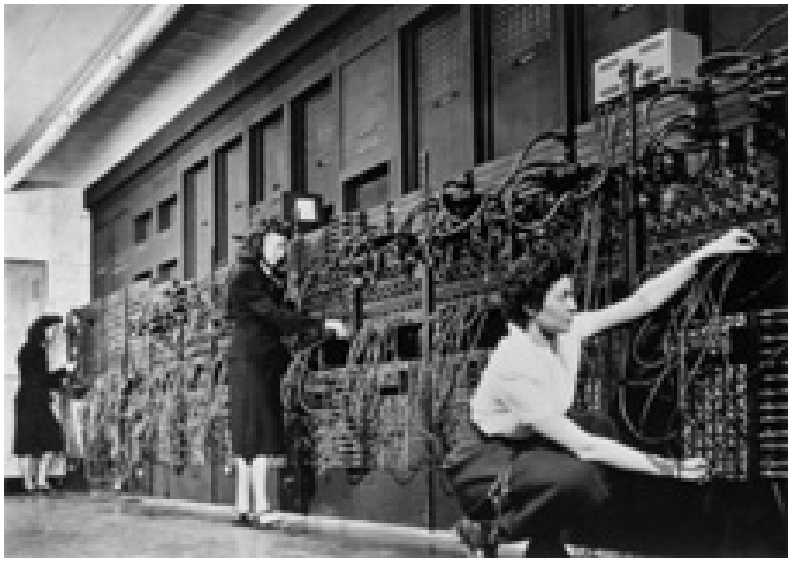
- 4000 components
- Three tons
- 31 digits

- Pros – automatic
- Cons – slow, expensive, not flexible



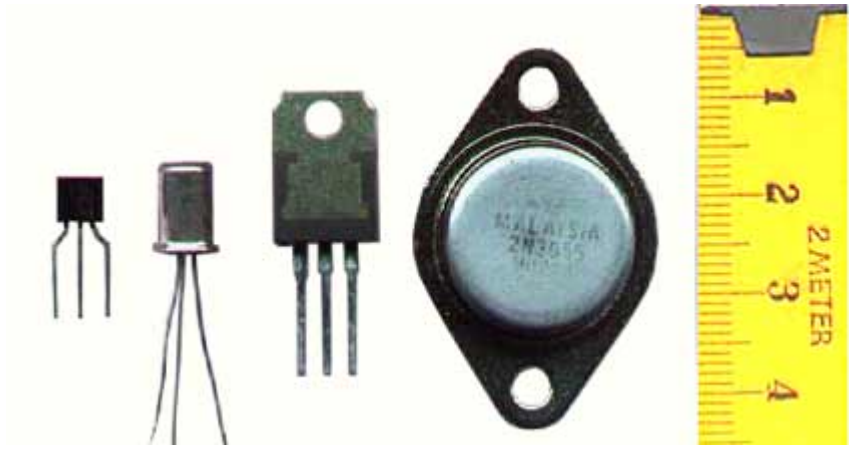
The first electronic computer

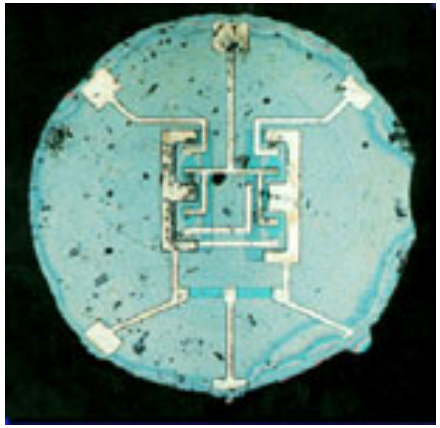
- Electrical numerical integrator and computer ENIAC (1946)
  - 18,000 vacuum tubes
  - 30 tons
  - 100,000 calculations per second
- Pro – faster, flexible
- Con – too big, not reliable



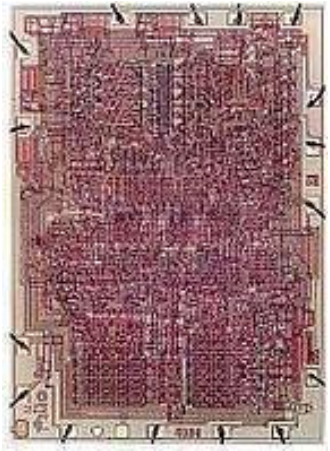
Semiconductors

The first transistor





The first integrated circuit



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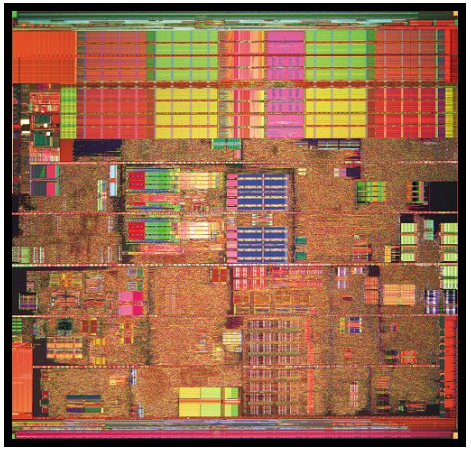
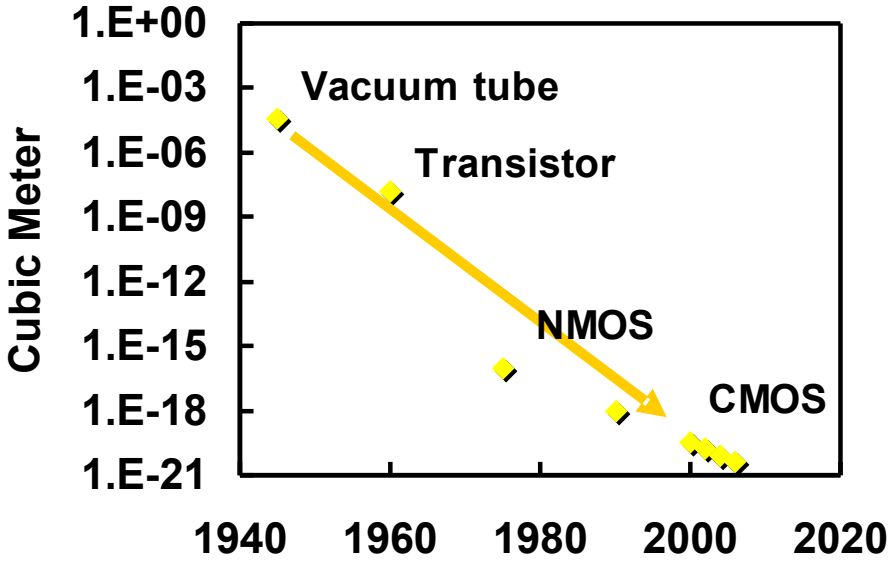
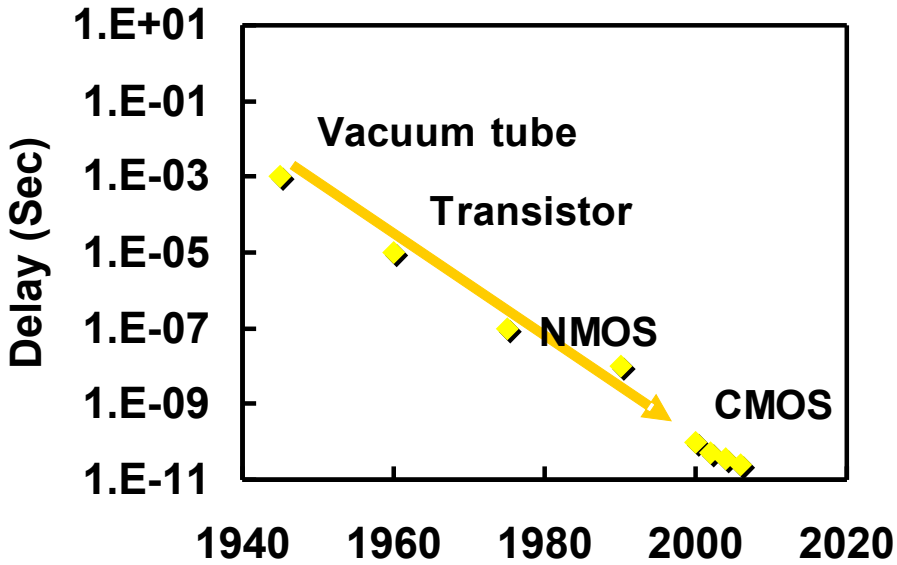
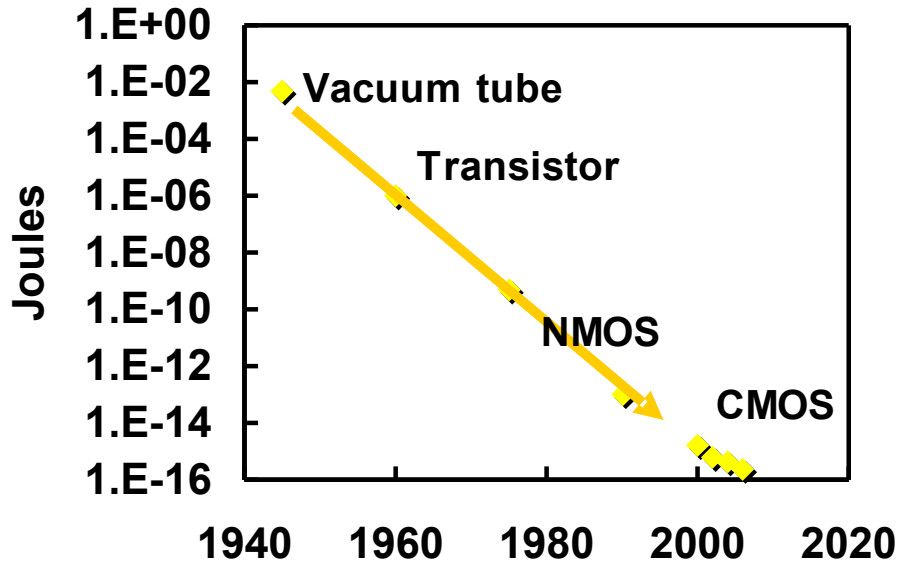


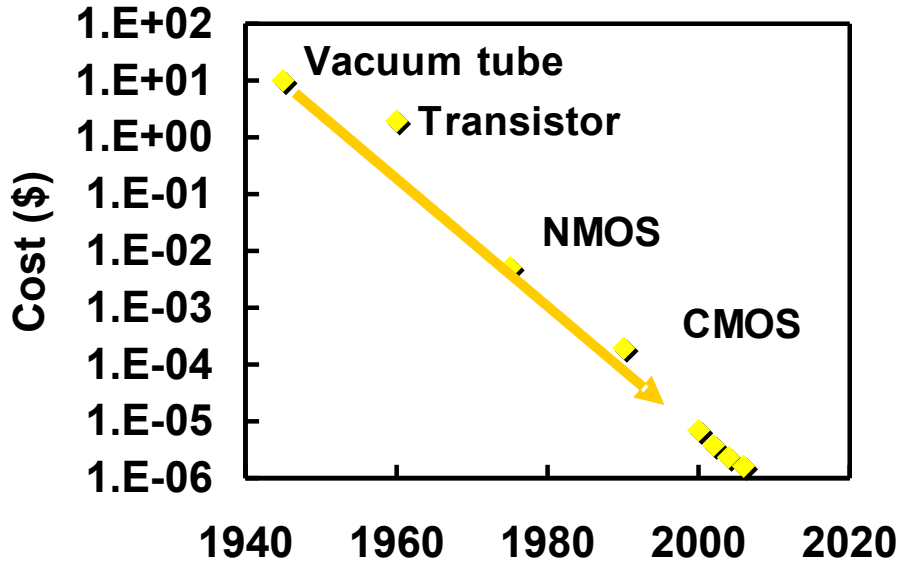
Pentium® 4

Benefits of scaling



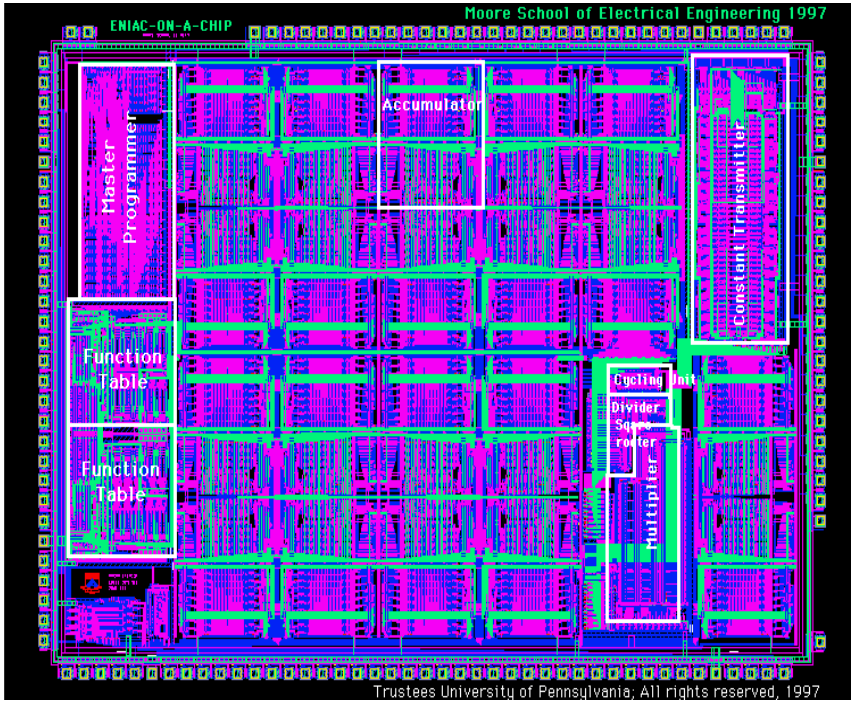






ENIAC-on-a-chip

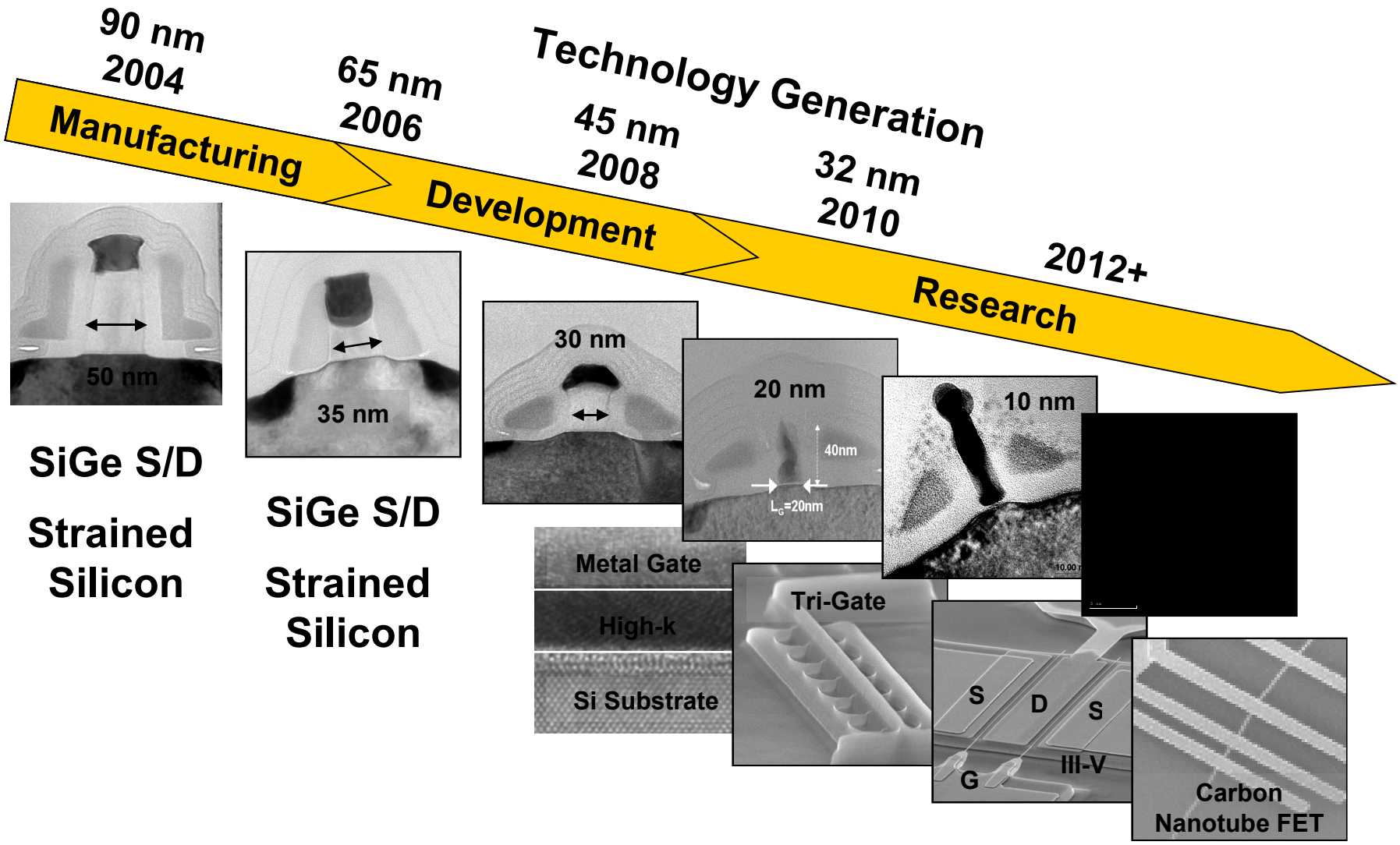
- 40 mm²
  - 174,000 transistors
- 0.5 W
- 20 MHz



Technology outlook

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Technology Node (nm)	90	65	45	32	22	16	11	8
Integration Capacity (BT)	2	4	8	16	32	64	128	256
Delay = CV/I scaling	0.7	~0.7	>0.7	Delay scaling will slow down				
Energy/Logic Op scaling	>0.35	>0.5	>0.5	Energy scaling will slow down				
Bulk Planar CMOS	High Probability						Low Probability	
Alternate, 3G etc	Low Probability						High Probability	
Variability	Medium			High			Very High	
ILD (K)	~3	<3	Reduce slowly towards 2-2.5					
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	6-7	7-8	8-9	0.5 to 1 layer per generation				

CMOS research continues…



SiGe S/D

Strained Silicon

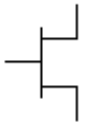
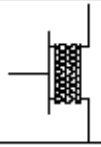
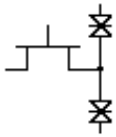
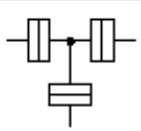
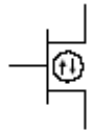
SiGe S/D

Strained Silicon

Nanotechnology outlook

- Why CMOS technology?
  - Performance
    - Gain, low noise
  - Area
    - Massive integration
  - Power
  - Reliability
  - Fabrication difficulty & cost
- Status & challenges
  - 65 nm Intel, IBM, TSMC, etc.
  - Power challenge
    - Energy, thermal issues
  - Fabrication cost
    - Photolithograph masks are expensive
  - Reliability
    - Soft errors
    - Electromigration, dielectric breakdown, etc.
  - Process variation
- Why nanotechnology?
  - To continue technology scaling to further scale integration, reduce cost, improve performance, and minimize power consumption
- Candidates
  - Carbon nanotube
  - Nanowire
  - Single electron device

Emerging nano devices

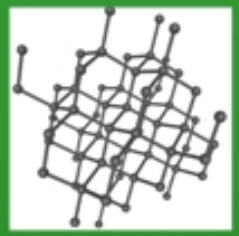
Device								
		FET [B]	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*Ferromagnetic logic*	*Spin transistor*
Types		*Si CMOS*	*CNT FET* *NW FET* *NW hetero-structures* *Crossbar nanostructure*	*RTD-FET* *RTT*	*SET*	*Crossbar latch* *Molecular transistor* *Molecular QCA*	*Moving domain wall* *M: QCA*	*Spin transistor*
Supported Architectures		*Conventional*	*Conventional and Cross-bar*	*Conventional and CNN*	*CNN*	*Cross-bar and QCA*	*CNN Reconfigure logic and QCA*	*Conventional*
Cell Size (spatial pitch)	*Projected*	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [D]	3μm [H]	~700 nm [M]	~2μm [R]	250 nm [V, W]	100 μm [X]
Density (device/cm^2)	*Projected*	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	*Projected*	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	*Projected*	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	*Projected*	3E-18	3E-18	>3E-18	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	3E-7 [R]	6E-18 [W]	Not known
Binary Throughput, GBit/ns/cm^2	*Projected*	238	238 [C]	238 [C]	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	0.1	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	4.2 – 300 K	20 K [L]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	III-V Si-Ge	III-V Si	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research activity [A]			171	88	65	204	25	102

Carbon nanotube

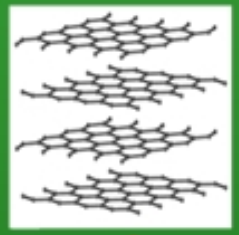
Forms of carbon…

Carbon atom can form several distinct types of valence bonds….

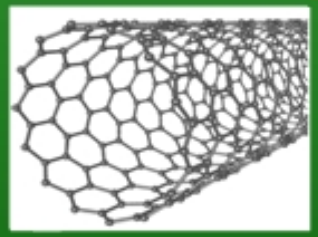
allotropes



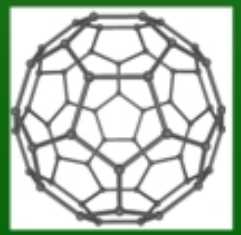
diamond



graphite

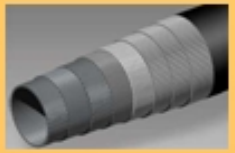


carbon nanotube

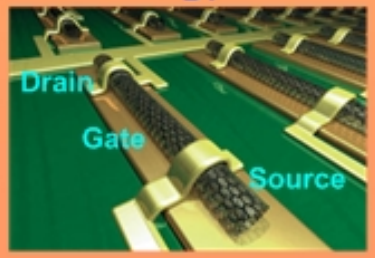


Fullerene

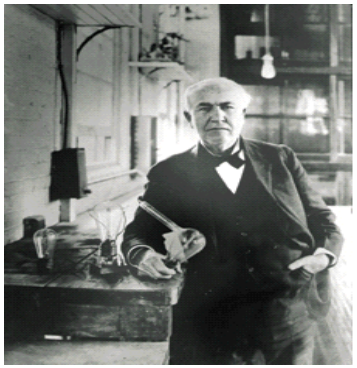
applications



nanotechnology

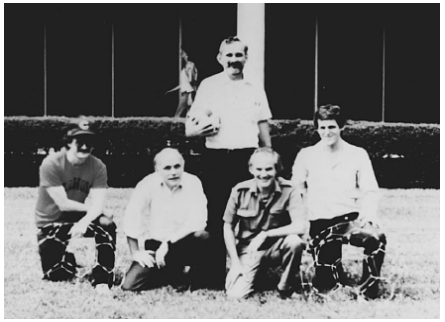


A bit of history….



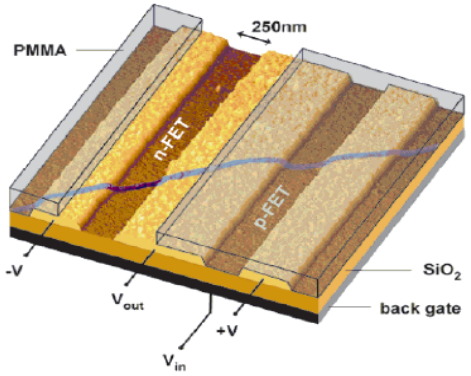
Edison's original carbon-filament lamp
US Patent 223898

1880



Discovery of Fullerenes (Smalley)

1985



Carbon nanotube transistor based logic-performing ICs (IBM)

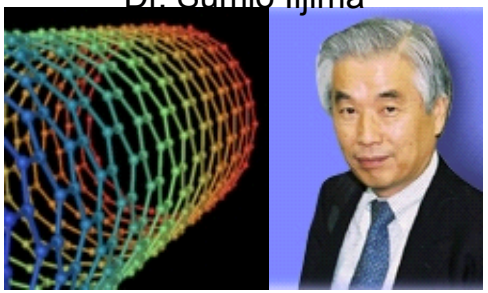
2001

1978

F/A-18 Hornet
The first aircraft with carbon fiber wings

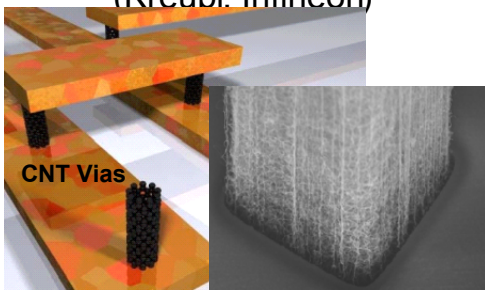
1991

Nanotubes discovered at NEC, by Japanese researcher Dr. Sumio Iijima

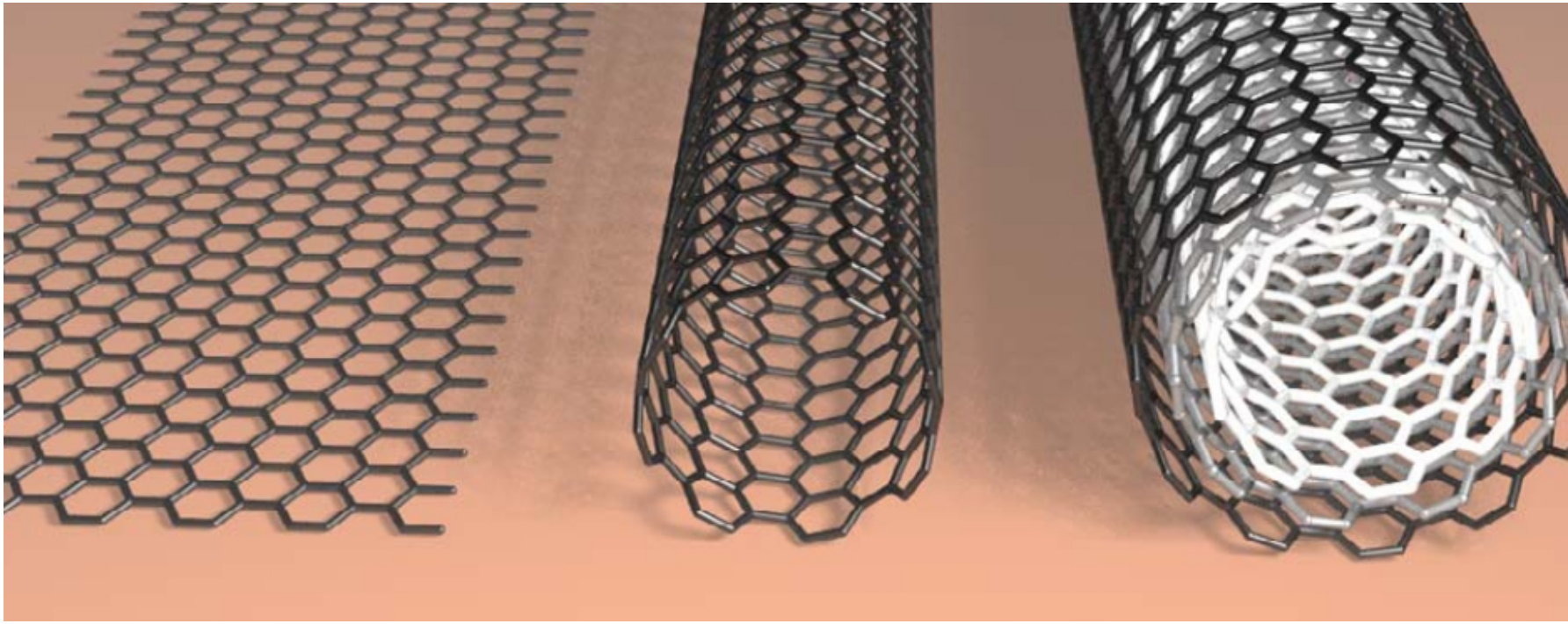


2002

Carbon nanotubes in interconnet applications (Kreupl, Infineon)



What are carbon nanotubes?



Graphene

Single-Walled Nanotube (SWCNT)

Multi-Walled Nanotube (MWCNT)

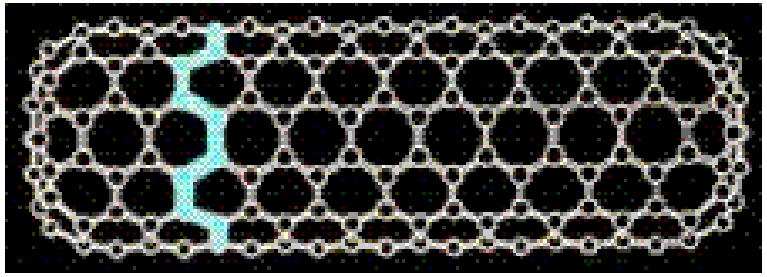
Eg ~1/d: Thick (>5nm) MWCNTs have a vanishing band gap at 300K, hence metallic…..

Courtesy: F. Kreupl, Infineon

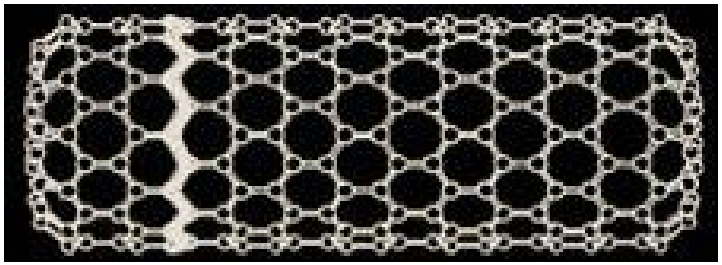
What are carbon nanotubes?

SWCNTs

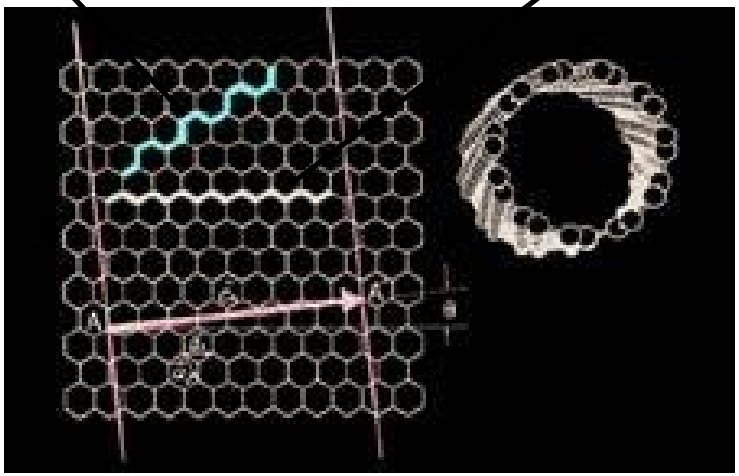
Armchair Nanotube (metallic)



Zigzag Nanotube (semi-conducting)



Various roll-ups possible depending on chirality



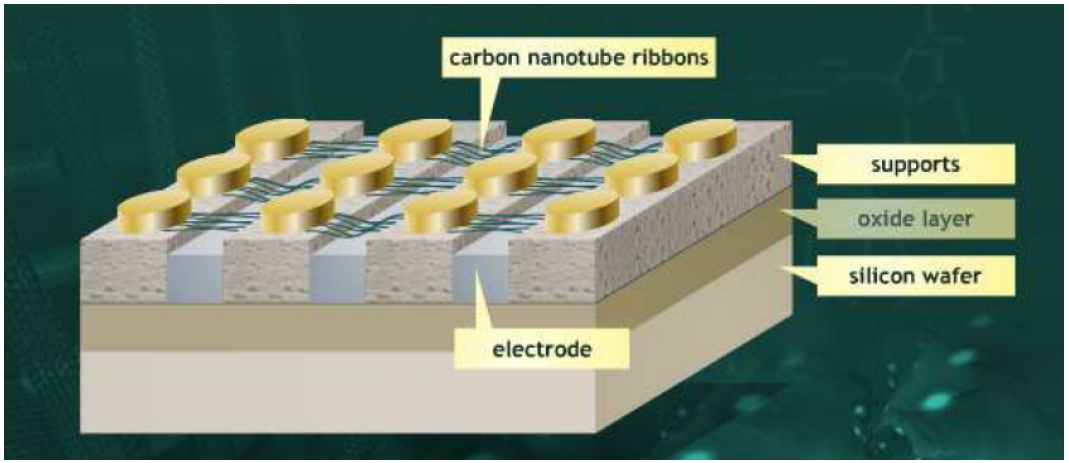
Chiral nanotube

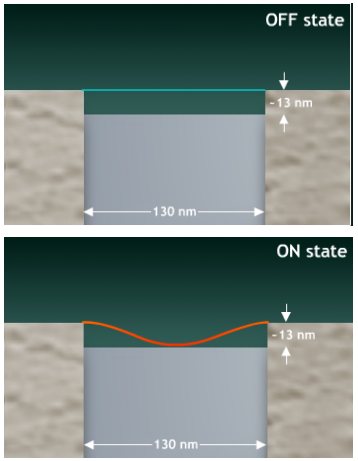
Properties

- Carbon nanotube
  - Single-wall or multi-wall
  - Diameter: 0.4-100nm
  - Length: up to millimeters
  - Ballistic transport
  - Excellent thermal conductivity
  - Very high current density
  - High chemical stability
  - Robust to environment
  - Tensile strength: 45 TPa! (high strength steel ~ 2TPa)
  - Temperature Stability: up to 2800 ^{o}C in vacuum and up to 700 ^{o}C in air

	CNT	Cu
Max current density (A/cm^2)	**>1x10^9** Wei, et al., *APL*, 2001	**<1x10^7**
Thermal conductivity (W/mK)	**5800** Hone, et al., *Phys. Rev. B*, 1999	**385**
Mean free path (nm) @ room temp	**>1000** McEuen, et al., *Trans. Nano.*, 2002	**40**

NRAM





Source: Nantero

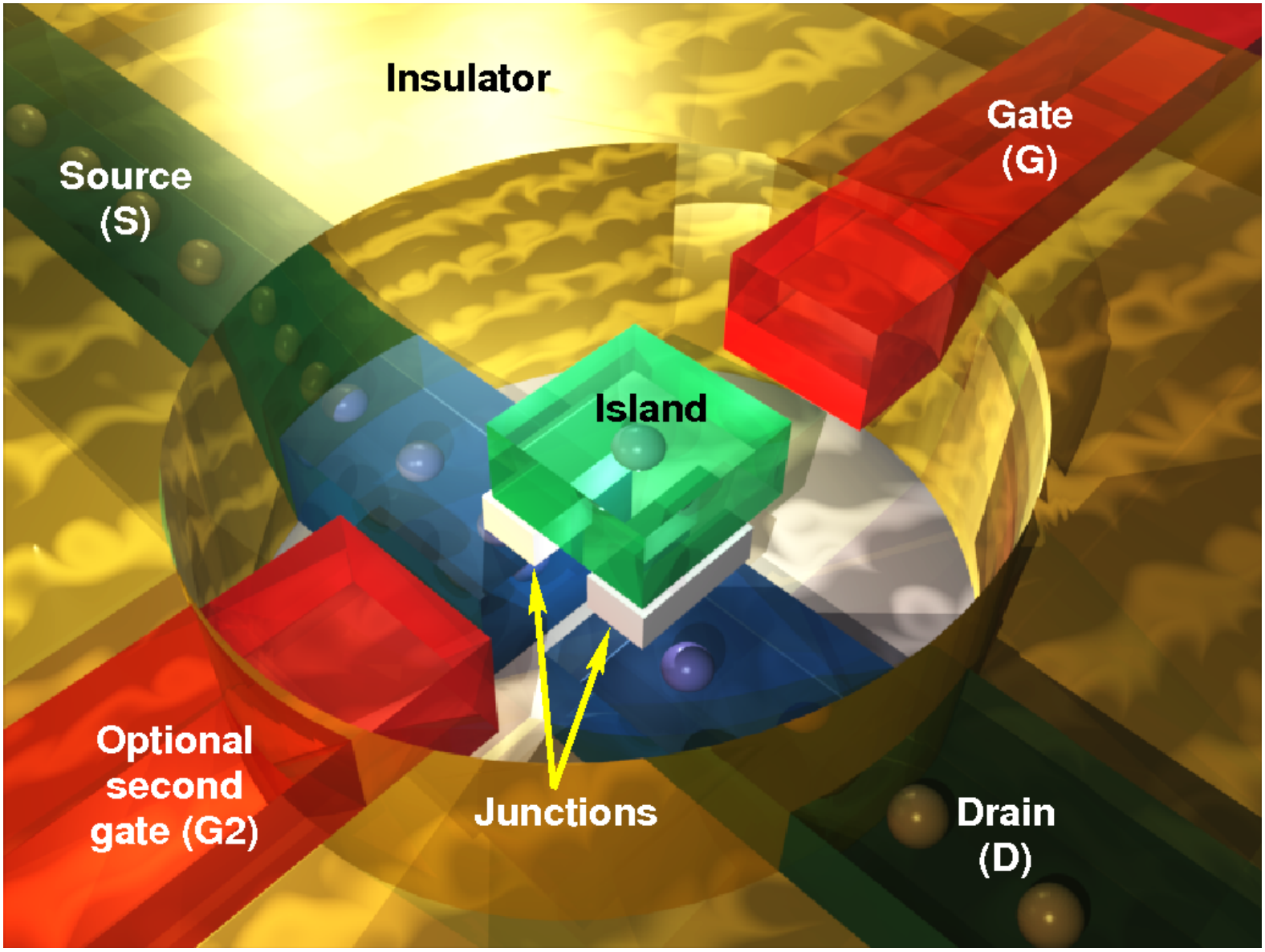
- Non-volatile nanotube random-access memory (NRAM)
  - Mechanically bent or not: determines bistable on/off states
  - Fully CMOS-compatible manufacturing process
  - Prototype chip: 10 Gbit NRAM
  - Will be ready for the market in the near future

NRAM

- Properties of NRAM
  - Non-volatile
  - Similar speed to SRAM
  - Similar density to DRAM
  - Chemically and mechanically stable

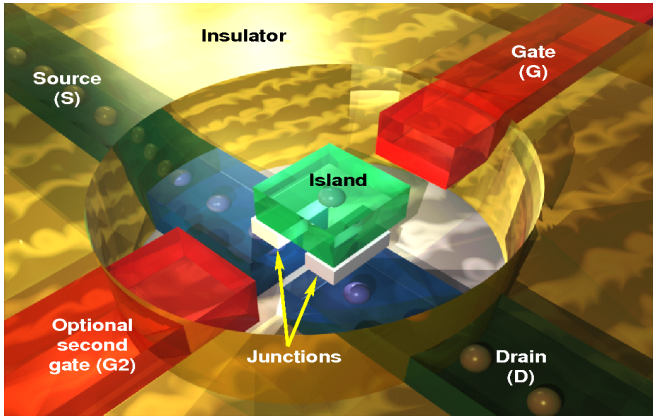
Single-electron tunneling transistor (SET)

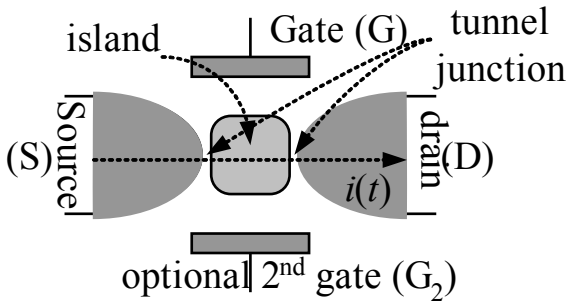
SET structure

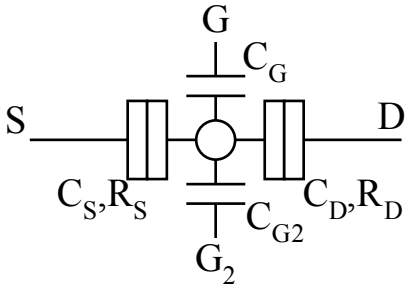


SET background

- Device structure
  - A nanometer-scale conductive island embedded in an insulating material
  - Electrons travel between the island and electrodes through tunneling junctions







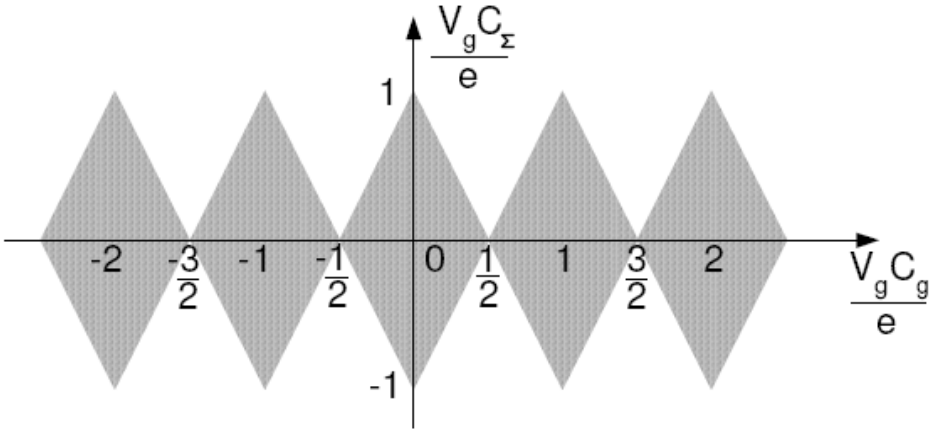
C_G	:gate capacitance	C_D	:drain tunnel junction capacitance
C_{G2}	:optional 2 nd gate capacitance	R_S	:source tunnel junction resistance
C_S	:source tunnel junction capacitance	R_D	:drain tunnel junction resistance

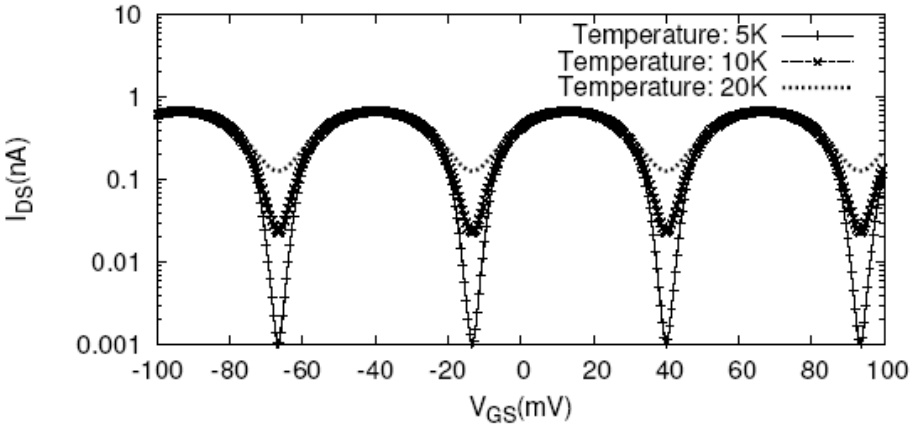
SET background

- Coulomb blockade effect
  - Electrostatic charge: e^2/C
  - Island has a minimal-energy number of electrons
  - When integer, tunneling in and out blocked
  - When ½ integer, tunneling permitted
  - Can tune with applied gate voltage, V_G

SET characteristics

- Periodic I-V characteristics
- This is not due to de Broglie wavelength!





SET characteristics

- Ultra-low power consumption
- Strong temperature dependency

$$e^2 / C \geq K_B T$$

- Fabrication challenge
- Reliability concern
  - Random background charge noise
- Low drive strength

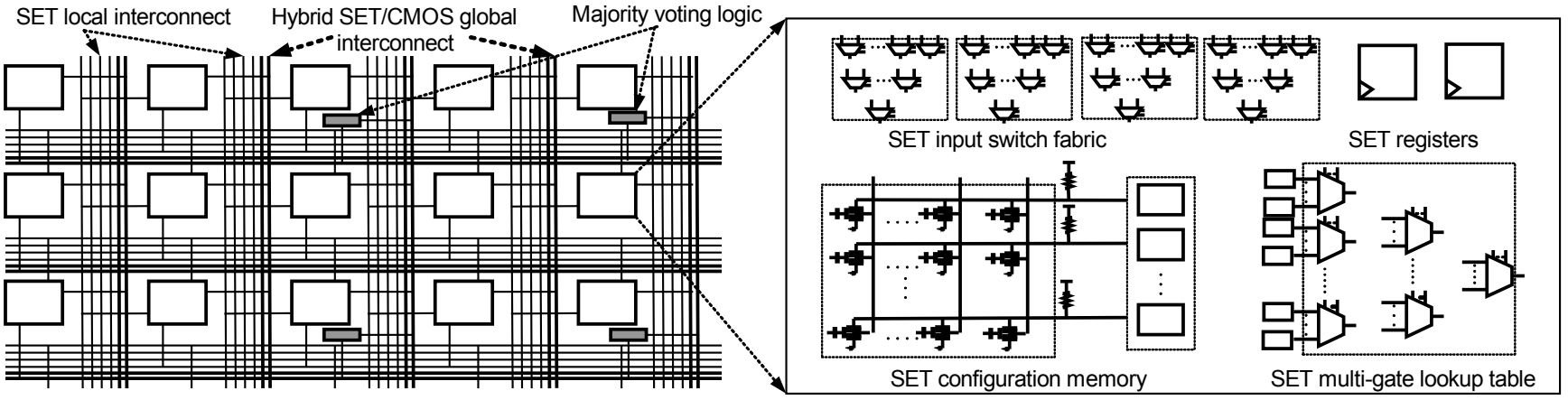
$$R \geq h / e^2 \approx 26\,K\,\Omega$$

- Low circuit gain

$$g = C_G / (C_S + C_D)$$

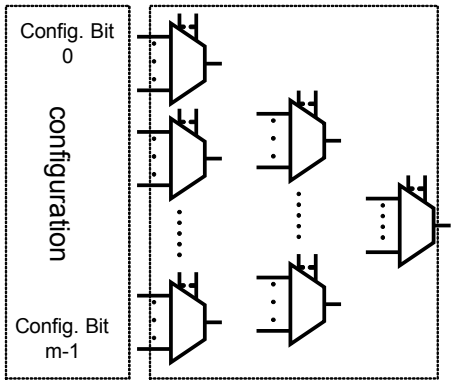
ICE-FLEX: hybrid SET/CMOS reconfigurable architecture design

- Design space
  - Power consumption
  - Performance
  - Fabrication challenge
  - Room-temperature operation
  - Reliability concerns
- Reconfigurable Architecture
  - SET logic block
  - SET/CMOS interconnect
  - SET configuration memory
  - SET/CMOS majority voting logic

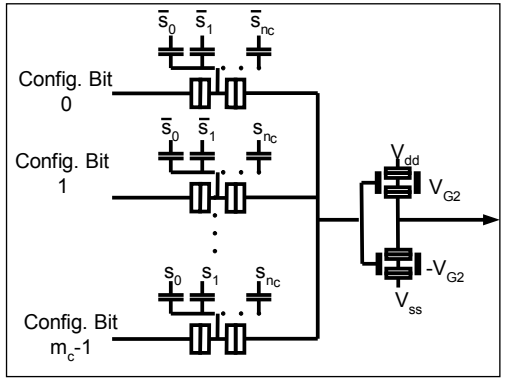


SET reconfigurable logic

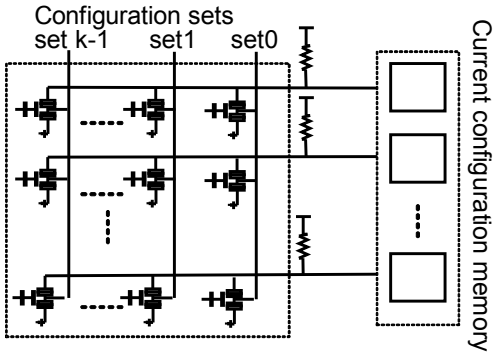
- SET multi-gate look-up table
  - Multi-gate structure
  - Strong temperature dependence
- SET configuration memory
  - Phase shifting controlled by Coulomb charge



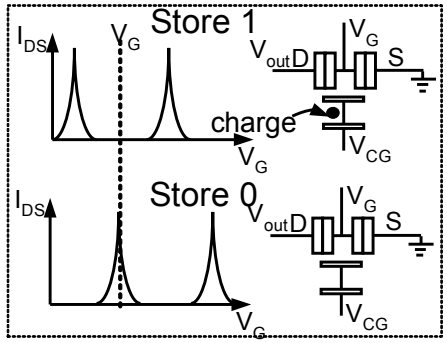
m-to-1 multi-gate multiplexer SET tree



m_c-to-1 multi-gate SET multiplexer



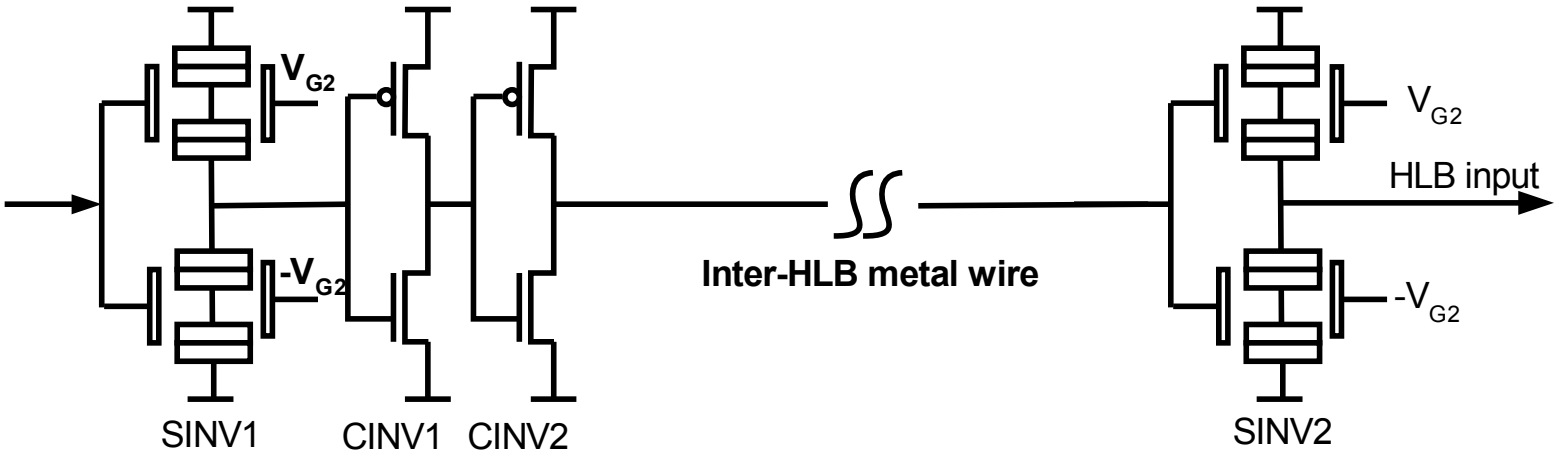
SET configuration cache



SET configuration cache

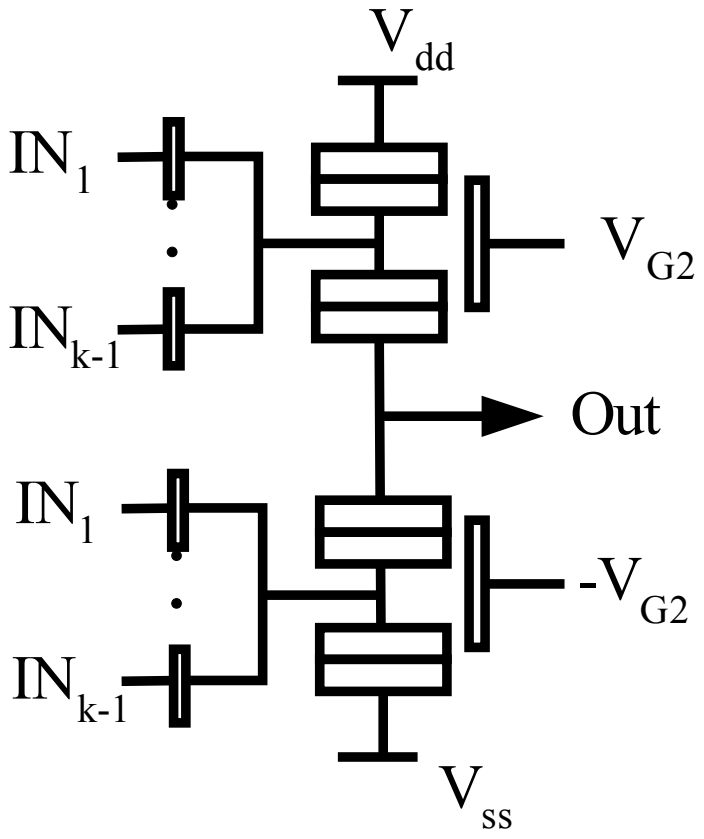
SET interconnect

- SET local interconnect
  - Static power dominant
- Hybrid SET/CMOS global interconnect
  - Dynamic power dominant



Majority voting & arithmetic logic

- SET MVL
  - Efficient implementation
  - Suffer from random background charge effect itself
- SET arithmetic logic
  - Threshold logic
  - Non-unate functions



Characterization

Benchmarks	FPGA			IceFlex					
	Xilinx Vertex-II XC2V2000			Non-Redundant Low Power			Non-Redundant High Performance		
	Freq (MHz)	Power (mW)	Energy req. (J/cycle)	Freq (MHz)	Power (mW)	Energy req. (J/cycle)	Freq (MHz)	Power (mW)	Energy Eff. (J/cycle)
ARM7	20.32	424	2.09e-08	1.00	0.13	1.33e-10	109.35	12.47	1.14e-10
ASPIDA DLX	97.09	611	6.29e-09	5.88	0.09	1.51e-11	645.16	8.37	1.30e-11
Jam RISC	74.05	469	6.33e-09	6.54	0.06	8.83e-12	716.85	5.44	7.59e-12
LEON2 SPARC	66.33	886	1.34e-08	4.52	0.27	5.87e-11	496.28	25.01	5.04e-11
Microblaze RISC	88.94	460	5.17e-09	8.40	0.04	4.61e-12	921.66	3.65	3.96e-12
miniMIPS	67.96	235	3.46e-09	4.90	0.11	2.33e-11	537.63	10.78	2.00e-11
MIPS	62.12	449	7.23e-09	5.35	0.06	1.04e-11	586.51	5.22	8.89e-12
Plasma	58.21	468	8.04e-09	4.52	0.08	1.72e-11	496.28	7.33	1.48e-11
UCore	105.34	613	5.82e-09	6.54	0.09	1.31e-11	716.85	8.06	1.12e-11
YACC	55.68	466	8.37e-09	9.80	0.07	7.38e-12	1075.27	6.81	6.34e-12
AES	158.63	387	2.44e-09	14.71	0.08	5.62e-12	1612.90	7.79	4.83e-12
AVR	55.55	105	1.89e-09	4.90	0.06	1.29e-11	537.63	5.94	1.11e-11
CORDIC	209.95	205	9.76e-10	58.82	0.03	4.44e-13	6451.61	2.46	3.81e-13
ECC	30.24	105	3.47e-09	5.88	0.09	1.46e-11	645.16	8.07	1.25e-11
FPU	21.96	155	7.06e-09	1.31	0.26	2.00e-10	143.37	24.60	1.72e-10
RS	383.73	35	9.12e-11	29.41	0.00	1.05e-13	3225.81	0.29	9.04e-14
USB	132.57	305	2.30e-09	19.61	0.07	3.53e-12	2150.54	6.52	3.03e-12
VC	88.19	775	8.79e-09	11.76	0.29	2.50e-11	1290.32	27.75	2.15e-11
Avg Energy Imp.						201.38×			234.60×

Characterization

Benchmarks	FPGA			IceFlex					
	Xilinx Vertex-II XC2V2000			Redundant Low Power			Redundant High Performance		
	Freq (MHz)	Power (mW)	Energy Eff. (J/cycle)	Freq (MHz)	Power (mW)	Energy req. (J/cycle)	Freq (MHz)	Power (mW)	Energy req. (J/cycle)
ARM7	20.32	424	2.09e-08	0.96	0.92	9.56e-10	102.72	86.52	8.42e-10
ASPIDA DLX	97.09	611	6.29e-09	5.67	0.61	1.08e-10	606.06	57.69	9.52e-11
Jam RISC	74.05	469	6.33e-09	6.29	0.40	6.36e-11	673.40	37.72	5.60e-11
LEON2 SPARC	66.33	886	1.34e-08	4.36	1.85	4.24e-10	466.20	174.21	3.74e-10
Microblaze RISC	88.94	460	5.17e-09	8.09	0.26	3.26e-11	865.80	24.89	2.87e-11
miniMIPS	67.96	235	3.46e-09	4.72	0.79	1.67e-10	505.05	74.44	1.47e-10
MIPS	62.12	449	7.23e-09	5.15	0.38	7.42e-11	550.96	36.00	6.53e-11
Plasma	58.21	468	8.04e-09	4.36	0.54	1.25e-10	466.20	51.29	1.10e-10
UCore	105.34	613	5.82e-09	6.29	0.59	9.39e-11	673.40	55.71	8.27e-11
YACC	55.68	466	8.37e-09	9.44	0.50	5.30e-11	1010.10	47.12	4.67e-11
AES	158.63	387	2.44e-09	14.16	0.57	4.04e-11	1515.15	53.86	3.55e-11
AVR	55.55	105	1.89e-09	4.72	0.44	9.26e-11	505.05	41.18	8.15e-11
CORDIC	209.95	205	9.76e-10	56.65	0.17	3.08e-12	6060.61	16.46	2.72e-12
ECC	30.24	105	3.47e-09	5.67	0.57	1.00e-10	606.06	53.45	8.82e-11
FPU	21.96	155	7.06e-09	1.26	1.83	1.45e-09	134.68	172.10	1.28e-09
RS	383.73	35	9.12e-11	28.33	0.02	7.39e-13	3030.30	1.97	6.52e-13
USB	132.57	305	2.30e-09	18.88	0.47	2.50e-11	2020.20	44.48	2.20e-11
VC	88.19	775	8.79e-09	11.33	2.04	1.80e-10	1212.12	192.19	1.59e-10
Avg Energy Imp.						27.05×			30.85×

Characterization

- Ultra-low power sensor applications
  - AVR (4 MHz) can run for 9.7 years on one AA battery
  - Scavenging indoor solar energy is sufficient to power AVR at 1.6 MHz
- Power-efficient high-performance computing
  - LEON2 SPARC: 1.6 Terra IPS at 100 W power budget, 16 Terra IPS under 1 kW power budget

Open questions

- Will nanotechnologies replace CMOS completely?
  - CMOS: high-performance, low cost, mature fabrication, reliable, relatively low power
- When will nanotechnologies be ready?
  - Nanotechnologies: fabrication challenge (10–15 years to mature), reliability challenge, performance concern, etc.
- What can we do?
  - CAD support, circuit design, architecture research

Open questions

- Characterizing impact of new technologies on applications: start with technology library
- Changes to classical problems: buffer insertion
- Nano modeling: Compact fast models validated against reported results and Monte-Carlo
- Reliability models: Correlations, distributions, rates
- Reliability solutions: Markov random fields or modular redundancy